DDR4-3200 Channel Modeling and Signal Integrity Analysis Using an FPGA

Presented by Benjamin Dannan

October 20, 2020

Technical Session

Presenter Bio

Benjamin Dannan has a multi-faceted background that includes a wide range of professional engineering and military experiences. He is a specialist in signal and power integrity concepts, high-speed circuit and multi-layered PCB design, vision systems, robotics, as well as has multiple years of experience with EMC product development and certifications to support global product launches. Benjamin graduated from Purdue University with a BSEE, and from Penn State University with his Masters of Engineering in Electrical Engineering. He also holds a certification in cybersecurity. In addition to being a recent DesignCon 2020 Best Paper Award winner, he is also an IEEE senior member.

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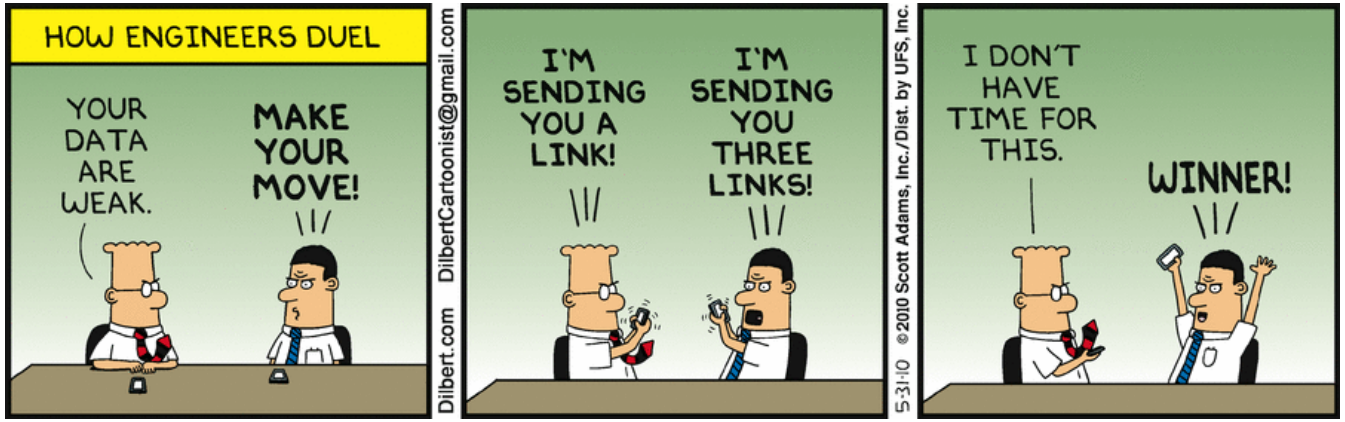
Outline

- Objectives & Background
- Simulation Platform
- DDR4 Interface Background
- UDIMM Channel Model Analysis
- VCK190 PCB Stack-up Analysis
- VCK190 Channel Model Analysis
- Channel Model Setup
- Channel Simulation Initial Results
- Channel Simulation Post-Tuning Results
- Conclusions



Source: dilbert.com

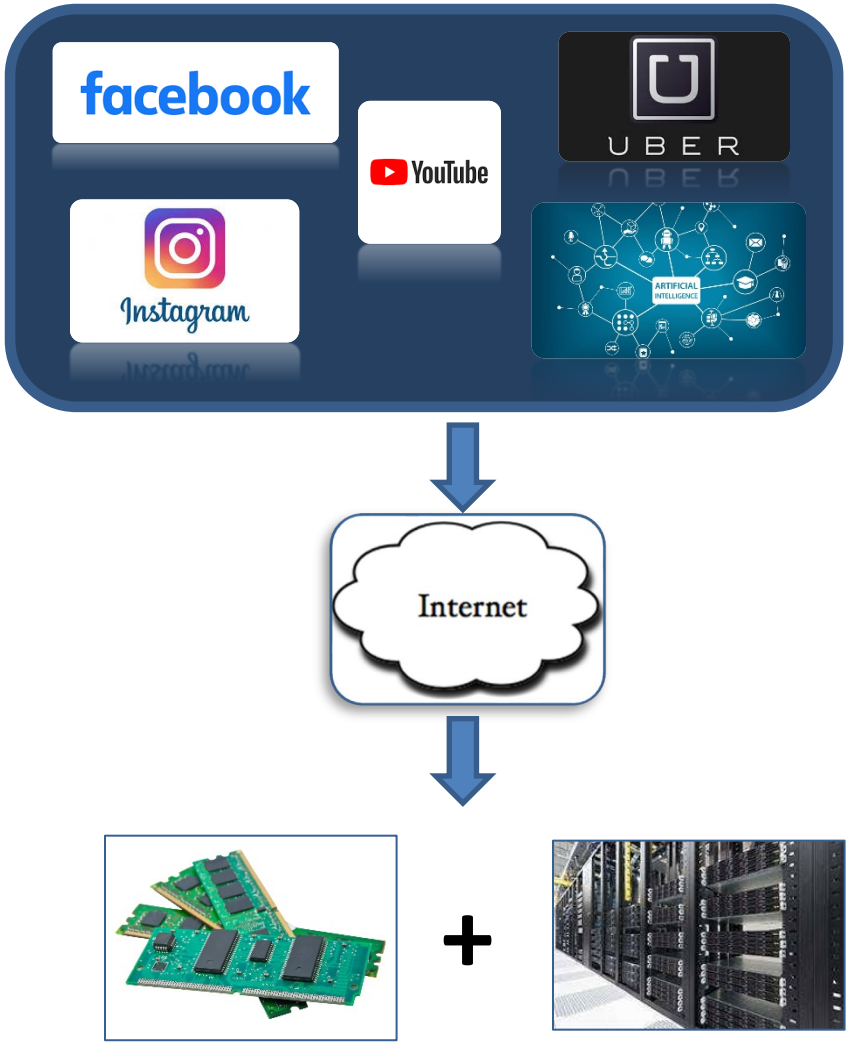
Today's Objectives

- ✓ Understand how to setup DDR4 model
- ✓ Simulate a DDR4 Model
- ✓ Analyze the results

1. Request/acquire all models (DIMM, IBIS, touchstone, etc.)
2. Import Layout file into ADS
3. Verify PCB stack-up, substrate material and properties
4. Use SIPro simulate DDR4 channel model(s)
5. Build DDR4 Channel Model in Memory Designer
6. Simulate Model
7. Analyze Results – Tune Channel and Re-simulate

Background

- **400 hours of video are uploaded to YouTube every minute [1]**
- **1,000,000,000+ hours of videos are watched on YouTube everyday [1]**
- **350 million photos are uploaded to Facebook daily, with 14.5 million photo uploads per hour [2]**
- **AI is quickly becoming part of everyday life**
  - Experts state that ML will require 6X amount of DDR than standard cloud server [3].
- **There is a need to store data and process it quickly**



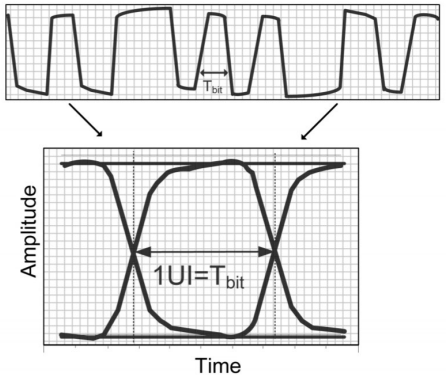
Making memory and fast-storage solutions central to the basic function of computing.

Background

Why do you care about Signal Integrity on DDR4?

> "There is no Black or White for high speed digital signals! Just different levels of grey. It is important to know where a design is located on this grey scale."
>
> – Hermann Ruckerbauer (EyeKnowHow)

- **DDR4-3200 has reduced margin vs. DDR3 => SI and PI become more critical for designs**
- **SHRINKING Unit Interval (UI) -** DDR4-3200 (3200 MT/s) UI = 312.5 ps
- **SK Hynix unveiled the world's *first* 64 GB DDR5-4800 and DDR5-5600 DIMMs** [3]
  - DDR5 UI is much smaller!
  - DDR5-4800 UI = 208.3 ps and DDR5-5600 UI = 178.571 ps
- **DDRx Data valid window & insertion loss targets continue to shrink**
  - Memory bottleneck is coming!

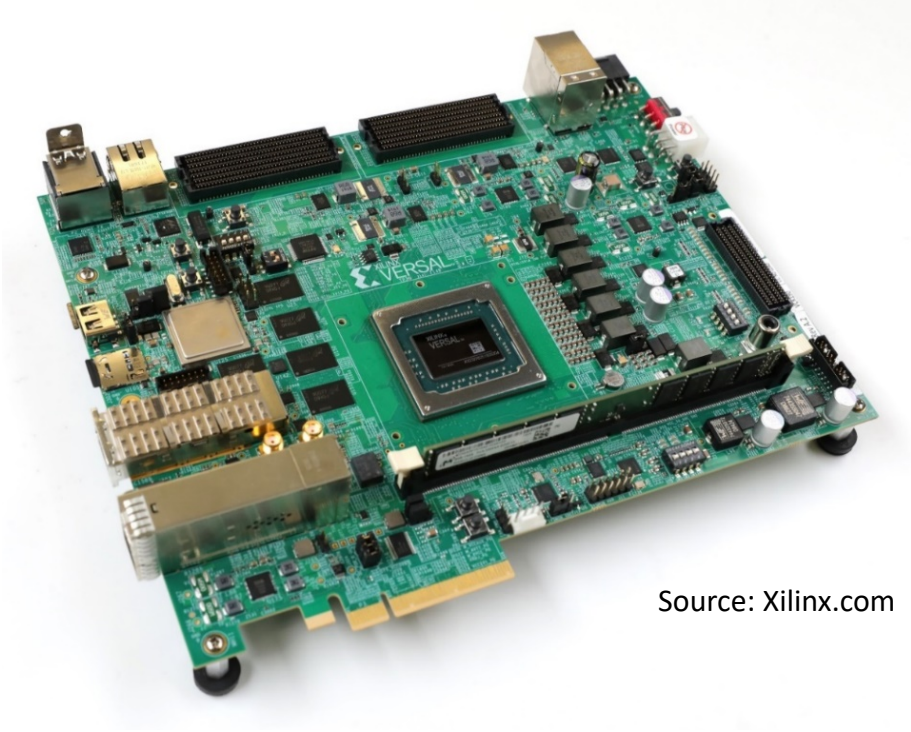


Source: Onsemi.com

Simulation Platform

VCK190 Evaluation Kit with Versal FPGA

- **Multiple high-speed digital interfaces** (PCIe G4, DDR4, LPDDR4, HDMI)
- **Versal FPGA memory controller has many features:**
  - DDR4, DDR4 3DS, LPDDR4/4X support
  - Multi-Rank and Dual-slot configuration support
  - ***1st FPGA with an integrated DDR4-3200 memory controller***

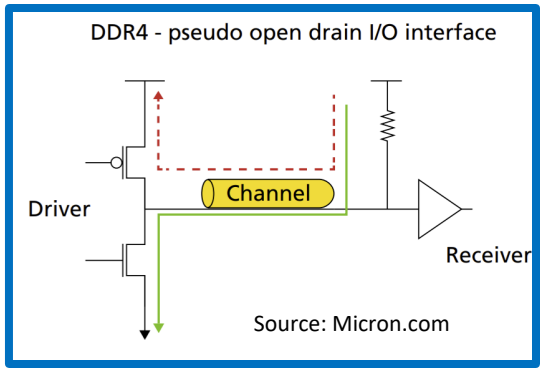


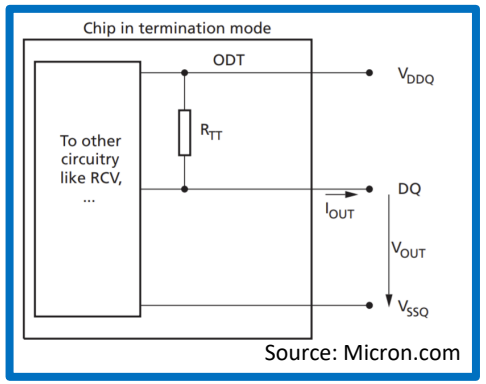
Source: Xilinx.com

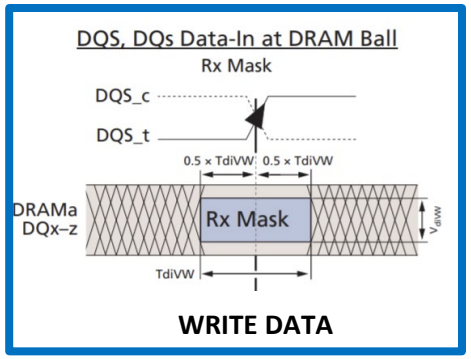
- **UDIMM interface**
  - DDR4 DIMM 288 position connector Amphenol MPN: 10124677 [7]
- **Simulation Models will use Micron *MTA16ATF2G64AZ-3G2E1 (R/C B1) UDIMM***
  - VCK190 Includes Micron UDIMM MPN: MTA9ADF1G72AZ-3G2E1 (R/C ZZ) – desired model unavailable, EBD model available

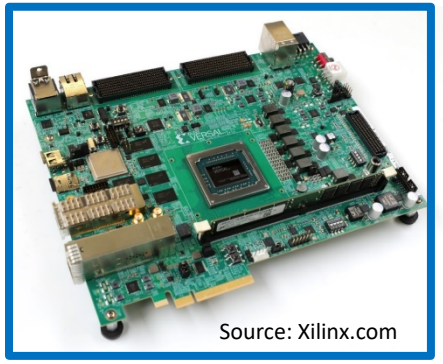
DDR4 Interface Background (basics)

- **Data Signals (DQ)** uses Pseudo Open Drain 1.2V (POD12)
  - Single Ended Signals
- **For channel calibration DDR4 DRAM uses On-Die Termination (ODT)** – *Designed to improve signal integrity*
  - ODT Values: OFF, 34 Ω, 48 Ω, 60 Ω, 80 Ω, 120 Ω, 240 Ω
- **Data Strobe (DQS)** uses Differential POD12
  - Edge-aligned with READ data (DQ)
  - Centered-aligned with WRITE data (DQ)
- **Clock (CK)** differential signal used to sample on positive-edge crossing for all address, command and control input signals



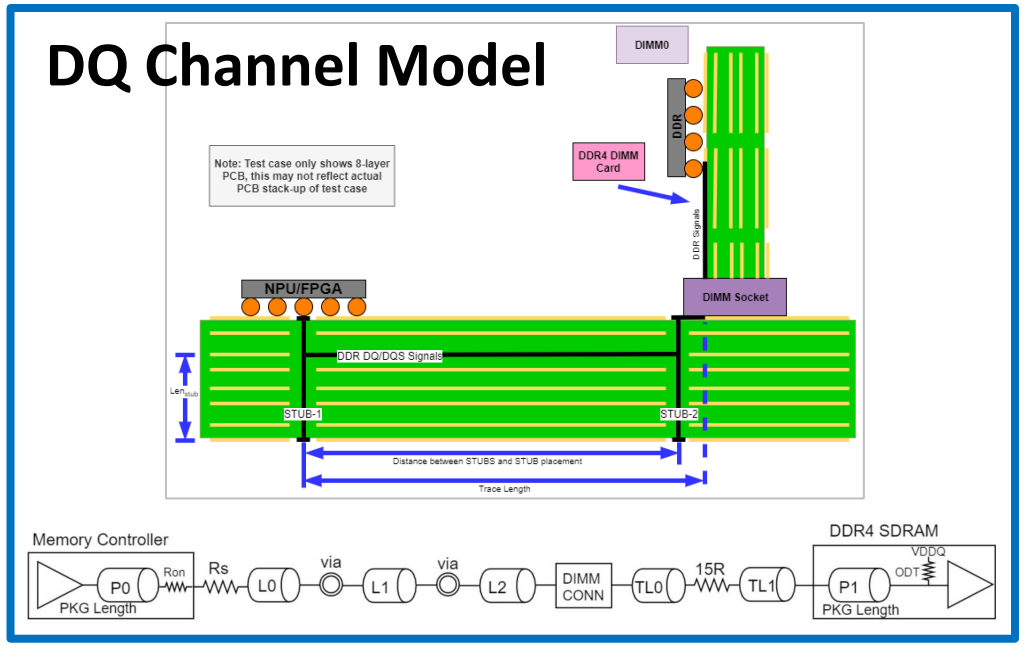






3D to 2D Channel Model

Depiction

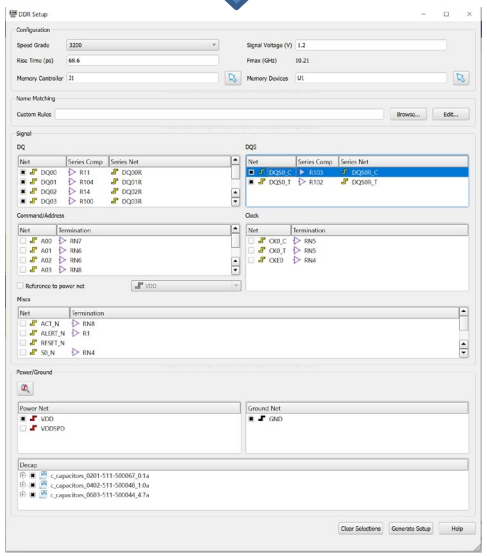


UDIMM (R/C B1) DDR4 Channel Model

Setting up UDIMM Model in SIPro

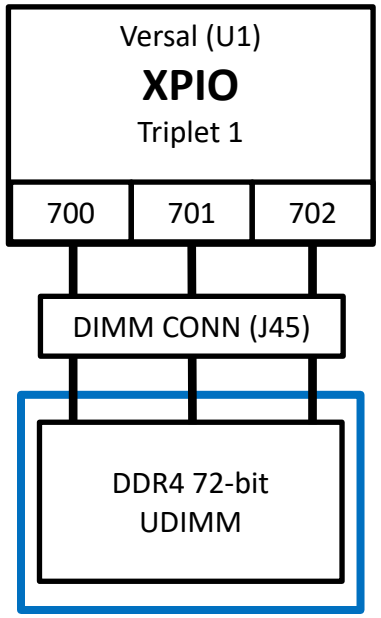
1. Import UDIMM file into SIPro
2. Use DDR setup to select signals
3. Check options and component models
4. Run simulation
5. Export SIO file

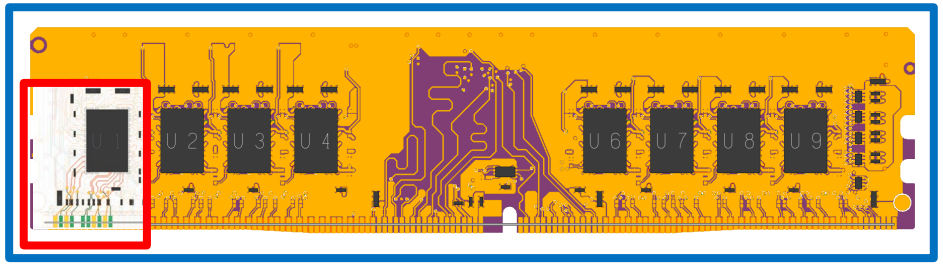
	Net Name	Start Pin	End Pin	Total Delay [ps]	Z0 (longest section)	Length [mm]	Width [mm]	Layer	Via Count
	DQ00	J1.5	R11.1	19.1	47.6	2.1188	0.1000	ETCH_TOP (1000)	0
	DQ00R	U1.D7	R11.2	89.2	49.5	6.2428	0.1000	ETCH_S6 (1005)	2
	DQ01	J1.150	R104.1	19.1	47.6	2.1221	0.1000	ETCH_BOTTOM (1007)	0
	DQ01R	U1.B7	R104.2	91.4	49.5	8.8481	0.1000	ETCH_S6 (1005)	2
	DQ02	J1.12	R14.1	17.6	47.6	1.7984	0.1000	ETCH_TOP (1000)	0
	DQ02R	U1.C2	R14.2	91.0	49.5	7.2269	0.1000	ETCH_S6 (1005)	2
	DQ03	J1.157	R100.1	17.7	47.6	1.8946	0.1000	ETCH_BOTTOM (1007)	0
	DQ03R	U1.D3	R100.2	93.1	49.5	8.4459	0.1000	ETCH_S6 (1005)	2

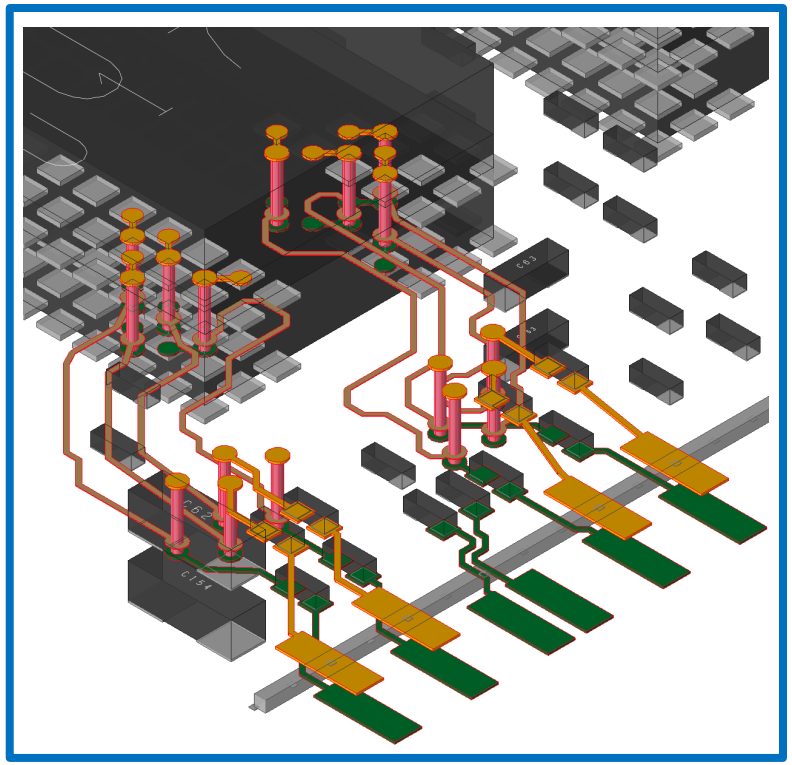


Transmission Line - Rapid Scan Analysis

Perform Design Inspection





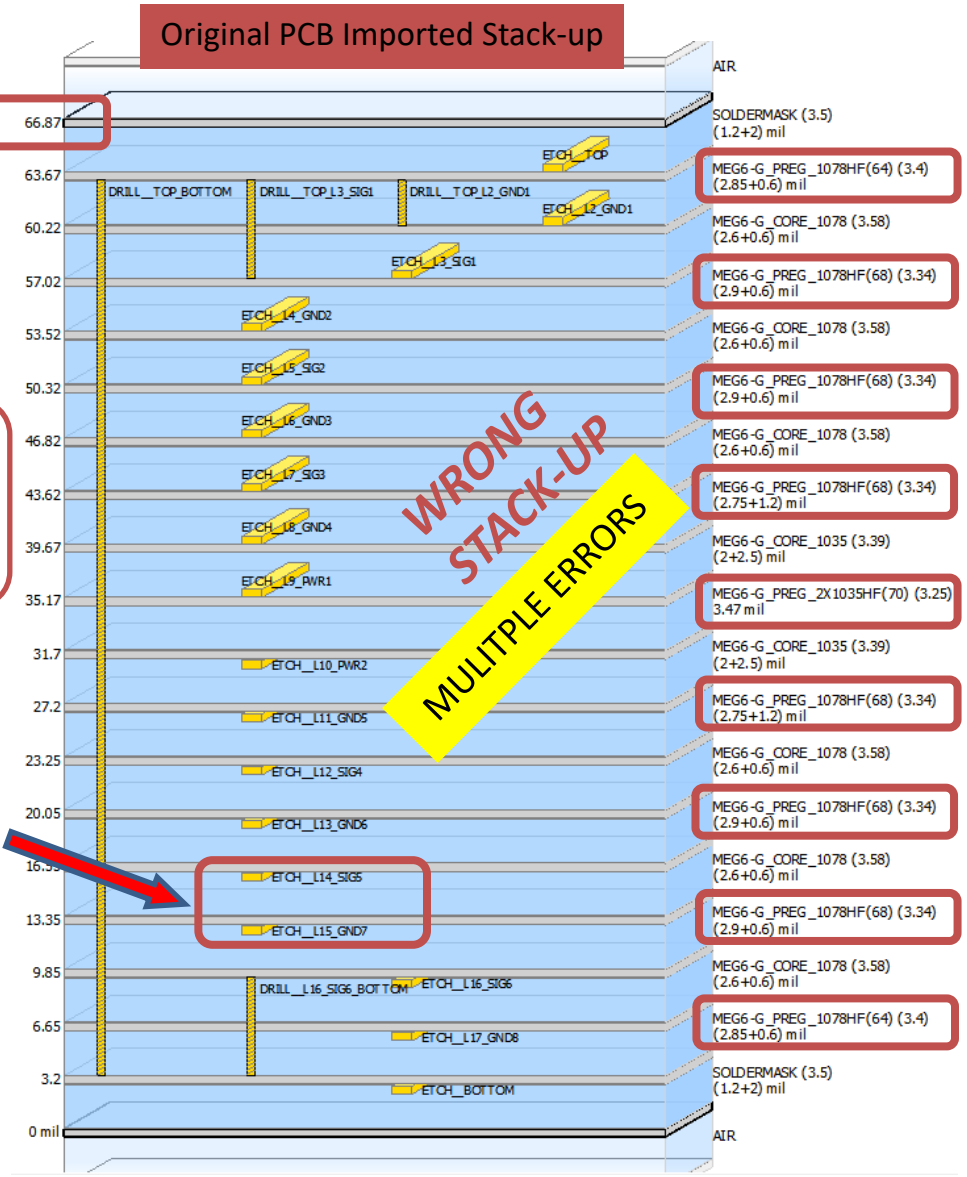


VCK190 18L PCB Stack-up Analysis

Error in total Stack-up thickness: ***66.87 mils***

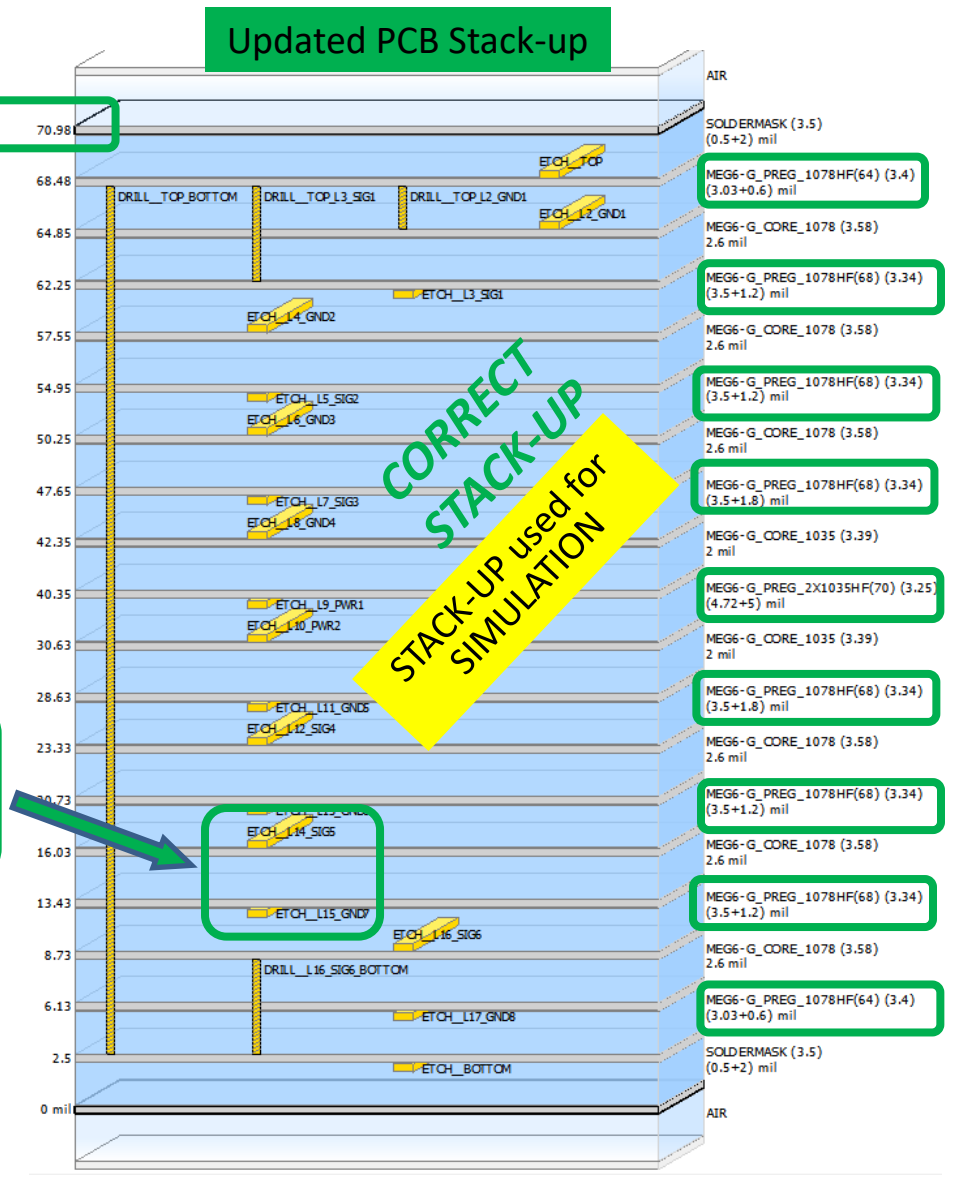
Multiple errors in laminate thickness & in dielectric property

For core material: Copper should reside on top & bottom of core material

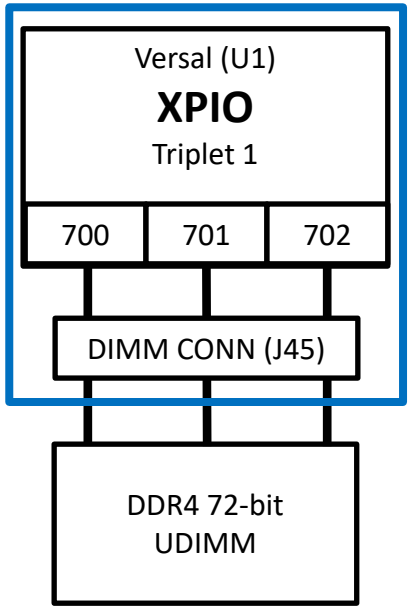


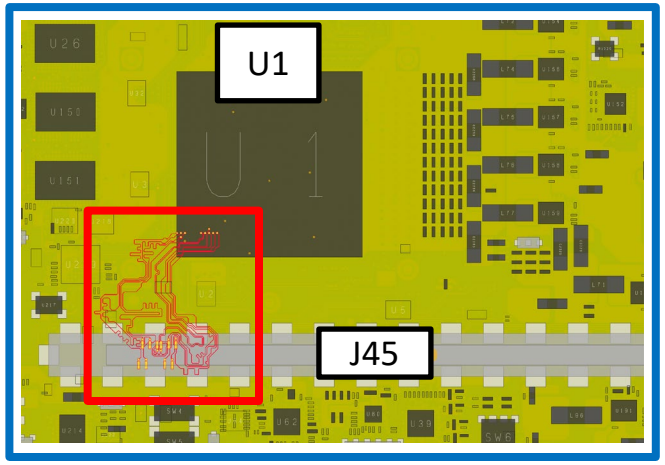
Updated PCB total stack-up thickness: ***70.98 mils***

Correct design for copper on core material in a stack-up

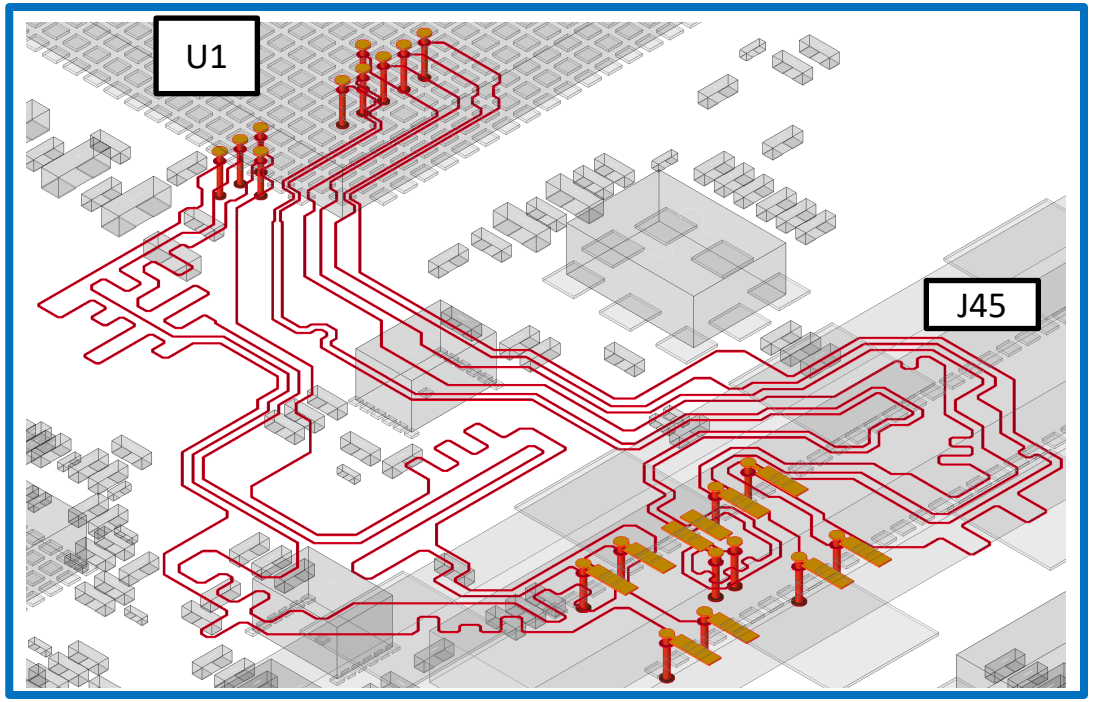


VCK190 DDR4 Channel Model





Depiction of DQ[0:7] and DQS signals between Versal (U1) and DIMM Connector (J45)



Setting up VCK190 Model in SIPro

1. Import VCK190 board file into SIPro
2. Use DDR setup to select signals
3. Check options and component models
4. Run simulation
5. Export SIO file

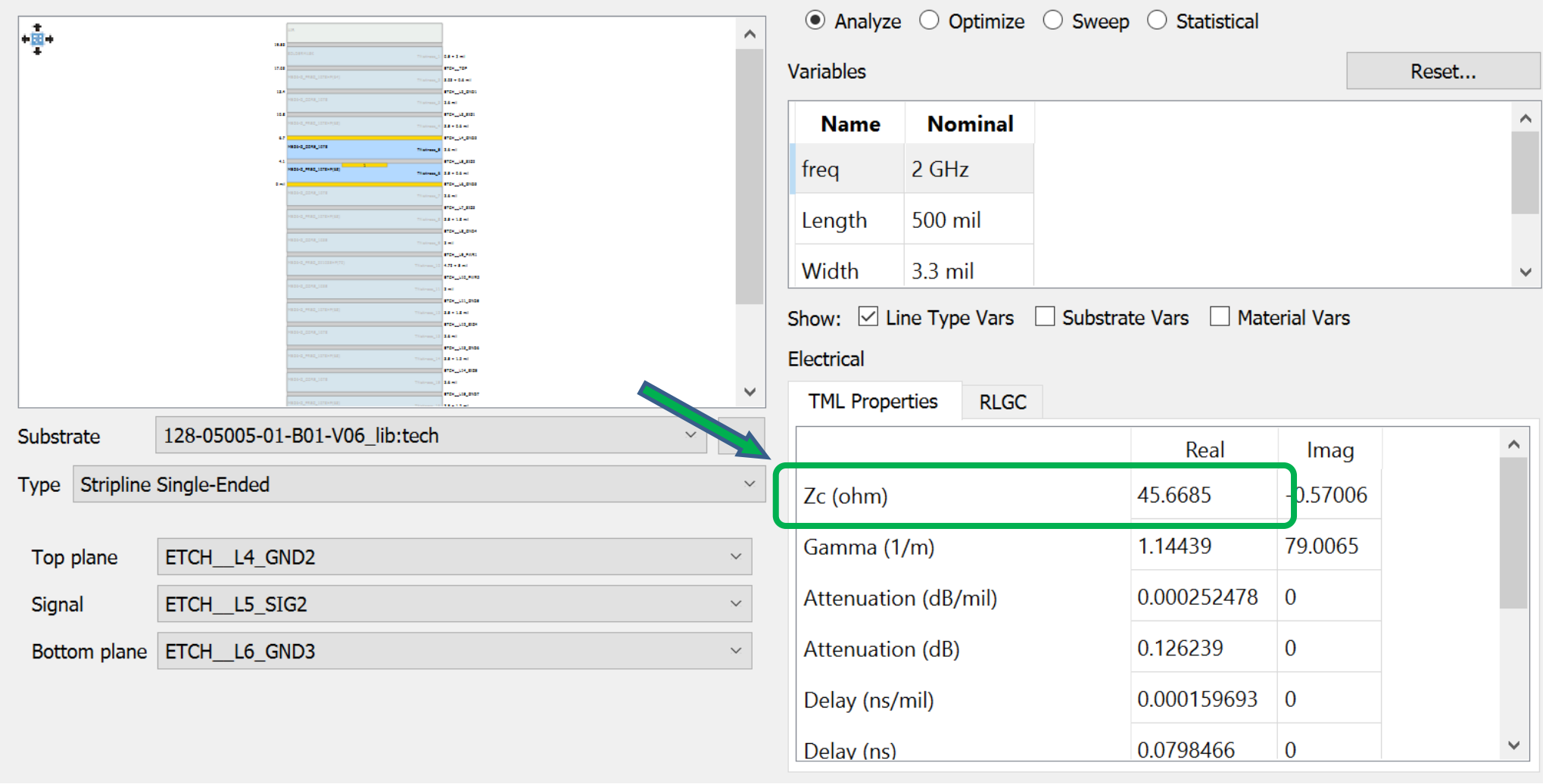
Perform Design Inspection

Net Name	Start Pin	End Pin	Total Delay [ps]	Z0 (longest section)	Length [mil]	Width [mil]	Width2 [mil]	Spacing [mil]	Layer	Via Count
DDR4_DIMM1_DQ0	U1.BE41	J45.5	443.1	45.4	2669.1	3.3			ETCH_L5_SIG2 (1004)	2
DDR4_DIMM1_DQ1	U1.BF41	J45.150	441.6	45.4	2660.3	3.3			ETCH_L5_SIG2 (1004)	2
DDR4_DIMM1_DQ2	U1.AV41	J45.12	442.9	45.4	2668.0	3.3			ETCH_L5_SIG2 (1004)	2
DDR4_DIMM1_DQ3	U1.AU41	J45.157	443.0	45.4	2660.3	3.3			ETCH_L5_SIG2 (1004)	2
DDR4_DIMM1_DQ4	U1.BG41	J45.3	437.0	45.4	2630.9	3.3			ETCH_L5_SIG2 (1004)	2
DDR4_DIMM1_DQ5	U1.BF42	J45.148	432.0	45.4	2599.0	3.3			ETCH_L5_SIG2 (1004)	2
DDR4_DIMM1_DQ6	U1.AW41	J45.10	435.5	45.4	2621.2	3.2			ETCH_L5_SIG2 (1004)	2
DDR4_DIMM1_DQ7	U1.AW40	J45.155	427.8	45.4	2572.1	3.2			ETCH_L5_SIG2 (1004)	2
DDR4_DIMM1_DQS0_C	U1.BA41	J45.152	449.5	45.7	2716.0	3.2			ETCH_L5_SIG2 (1004)	2
DDR4_DIMM1_DQS0_T	U1.AY41	J45.153	450.5	45.7	2722.6	3.2			ETCH_L5_SIG2 (1004)	2

Transmission Line - Rapid Scan Analysis

VCK190 DQ[0:7] Channel Model Impedance

Let’s do a quick check of impedance for DQ signals on Layer 5 to determine the target impedance……



VCK190 DQ[0:7] Channel Insertion Loss Results

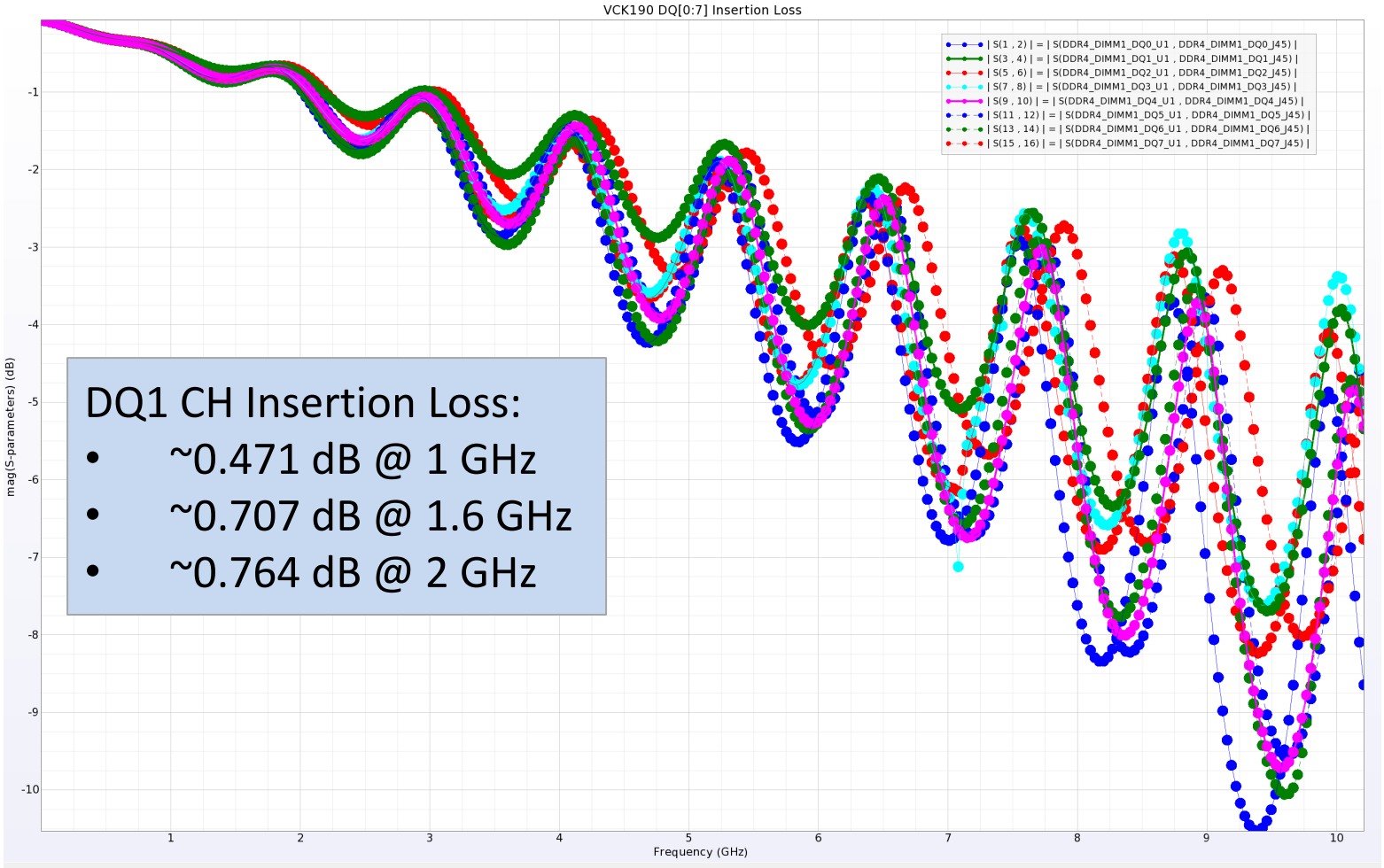
$$atten\,[dB/inch] \approx \frac{31.6}{(W[mils]+T[mils])*Z_0}\sqrt{f[GHz]} + 2.32 \times f[GHz] \times Df \times \sqrt{Dk} \quad [11]$$

Where for MEG6 R-5670(G) Prepreg 1078, 68% resin content:

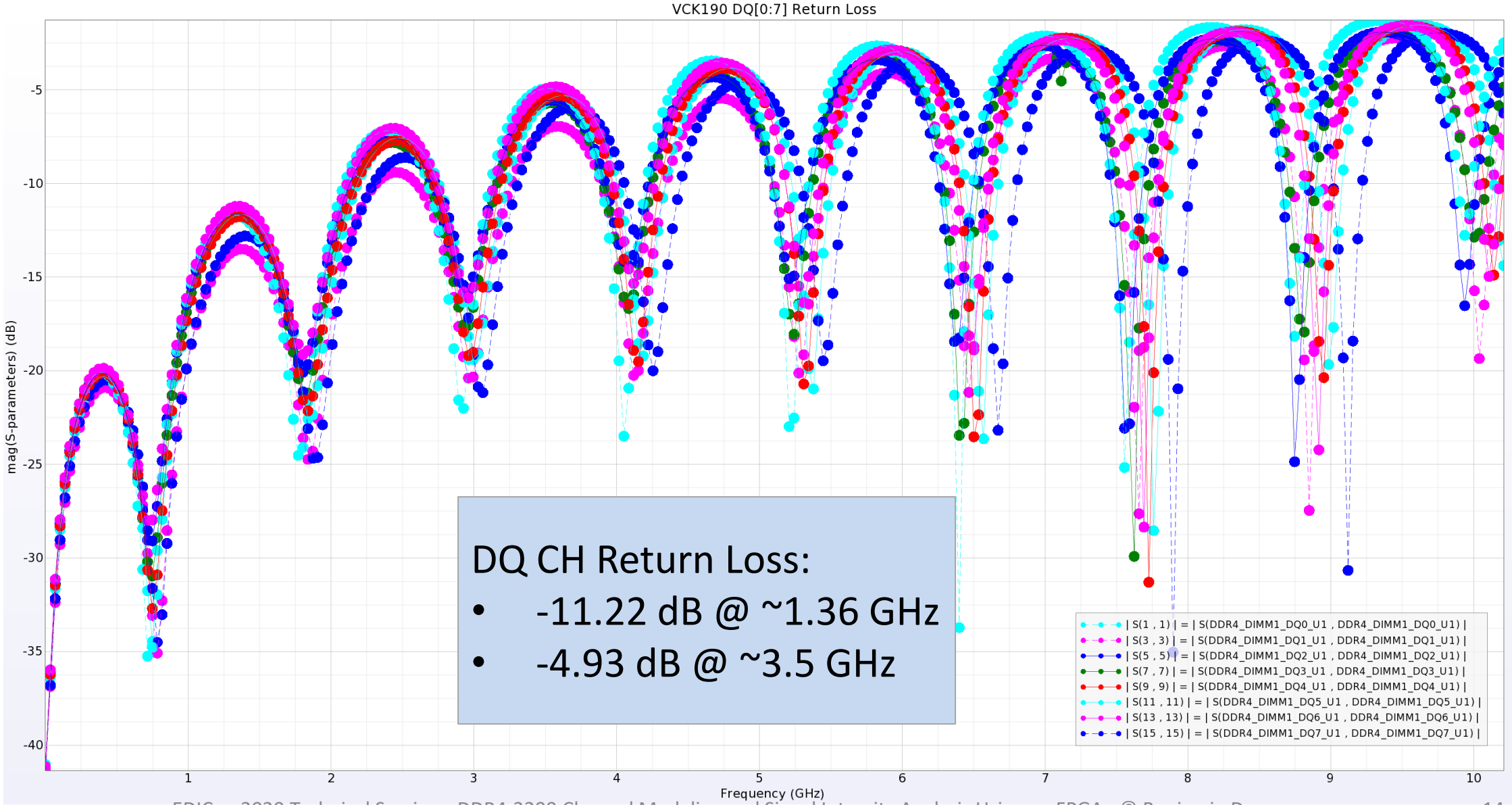
- W = Width = 3.3 mils
- T = Trace thickness (inches) = 0.5 oz CU = 0.6 mil
- Material's dissipation factor (Df)= 0.002 @ 2 GHz
- Dielectic constant (Dk) = 3.34 @ 2 GHz
- DQ0_Len = 2.6603 inch
- Z_0 = 45.6 Ω

$$atten_{DQ1\_2.6603\_in} \approx 0.497\ dB\ @\ 1.0\ GHz$$
$$atten_{DQ1\_2.6603\_in} \approx 0.629\ dB\ @\ 1.6\ GHz$$
$$atten_{DQ1\_2.6603\_in} \approx 0.703 dB\ @\ 2.0\ GHz$$

=> Good correlation!



VCK190 DQ[0:7] Channel Return Loss Results

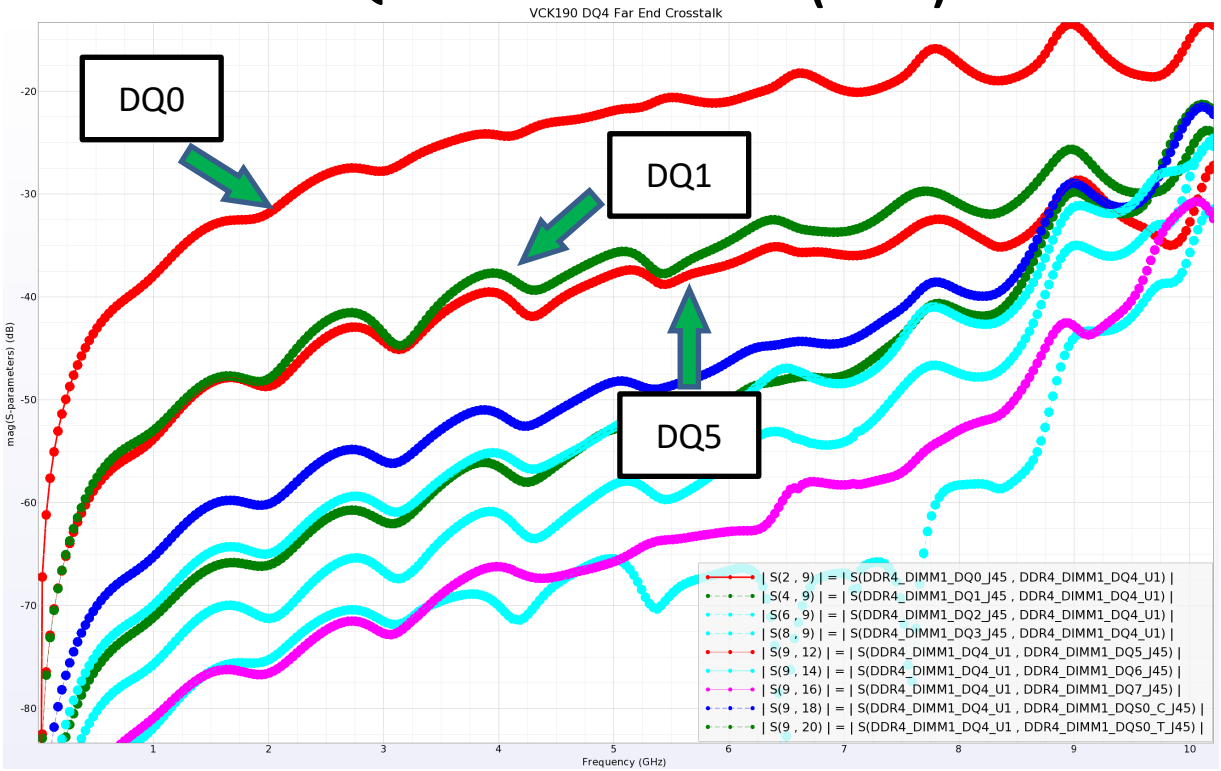


DQ CH Return Loss:

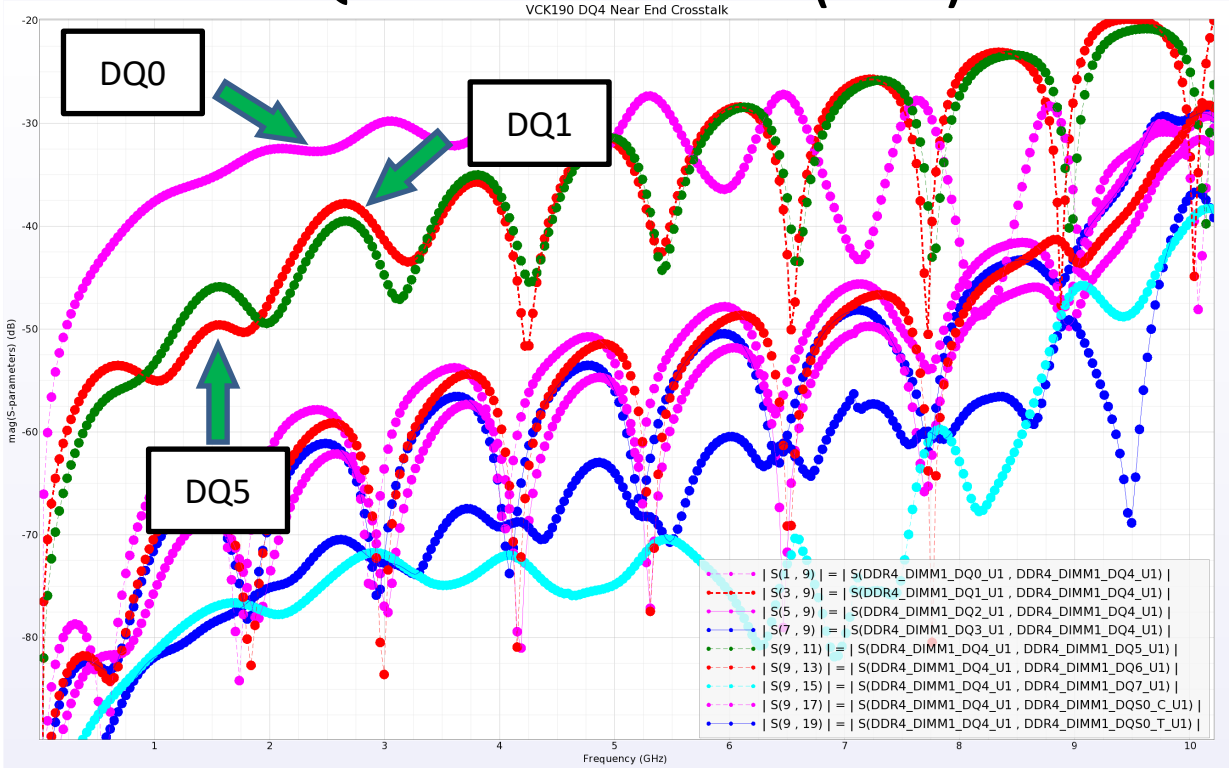
- -11.22 dB @ ~1.36 GHz
- -4.93 dB @ ~3.5 GHz

VCK190 DQ4 Channel Far End and Near End Crosstalks Results

DQ4 Far End Crosstalk (FEXT)



DQ4 Near End Crosstalk (NEXT)

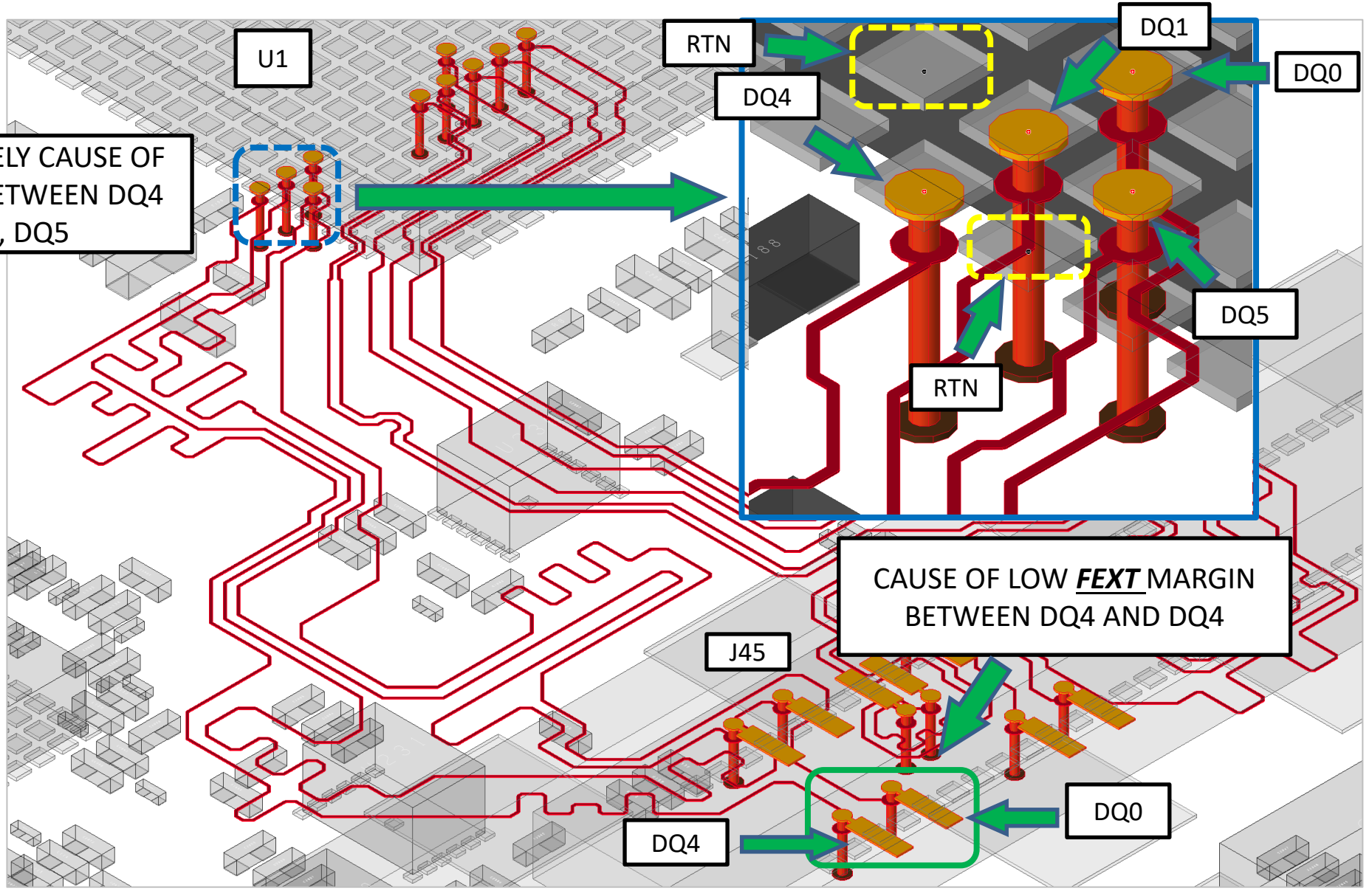


Significant eye closure due to crosstalk must be accounted for in system analysis

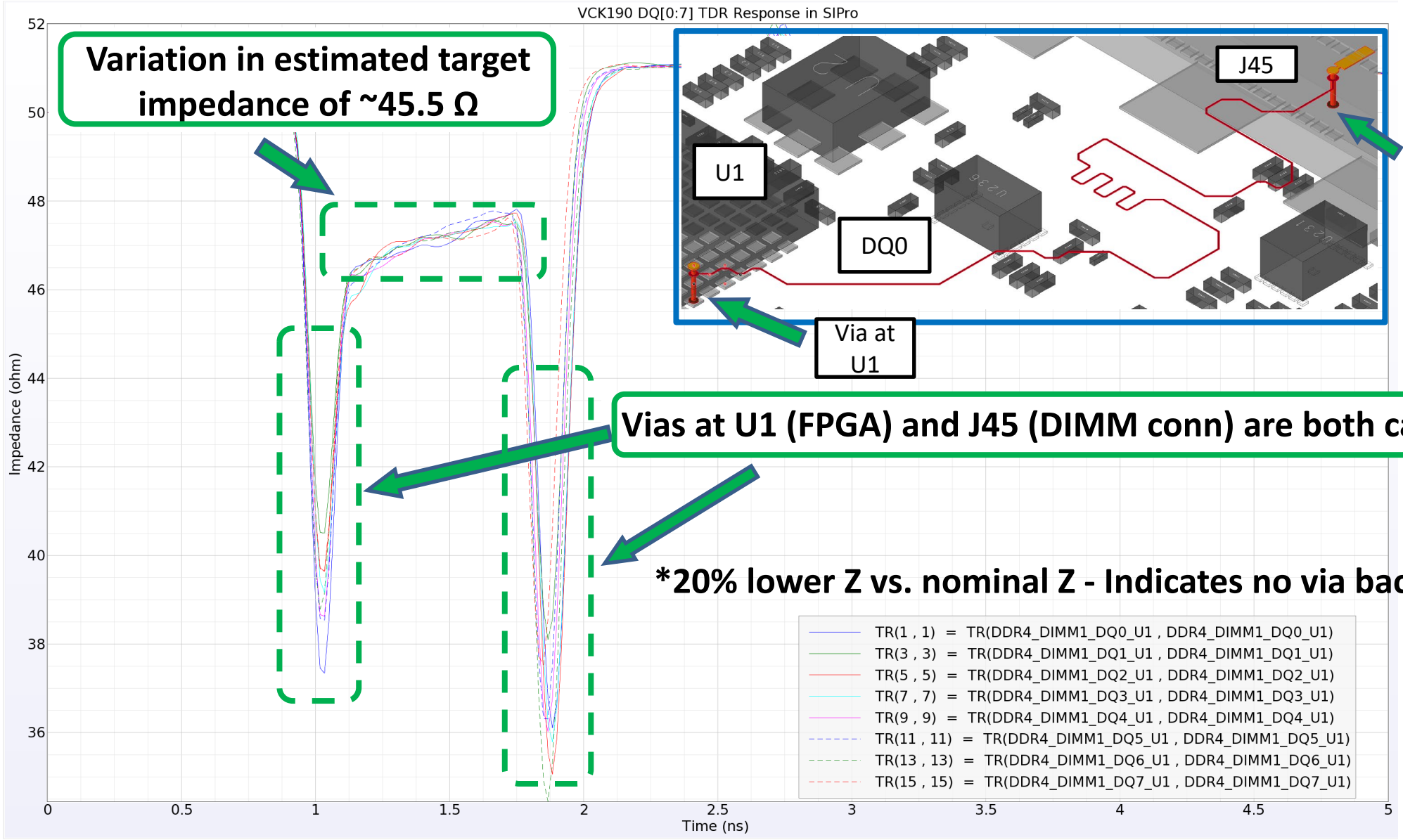
- DQ4 has ~10 dB less margin to DQ0 in both in FEXT and NEXT at 1.6 GHz
- DQ1 and DQ5 in both the FEXT and NEXT have the second least margin to DQ4

VCK190 DQ4 Channel Far End and Near End Crosstalks Results

Let's do a quick check of layout to inspect for possible FEXT or NEXT issues……..



VCK190 DQ[0:7] Channel Impedance Analysis



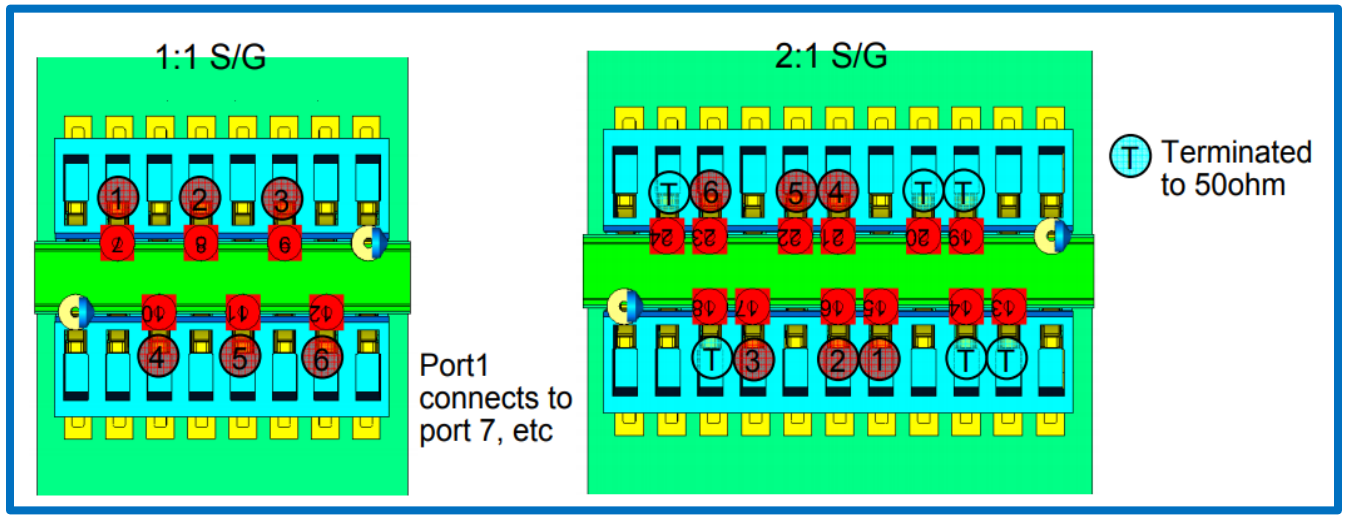
DIMM Connector Channel Model Setup

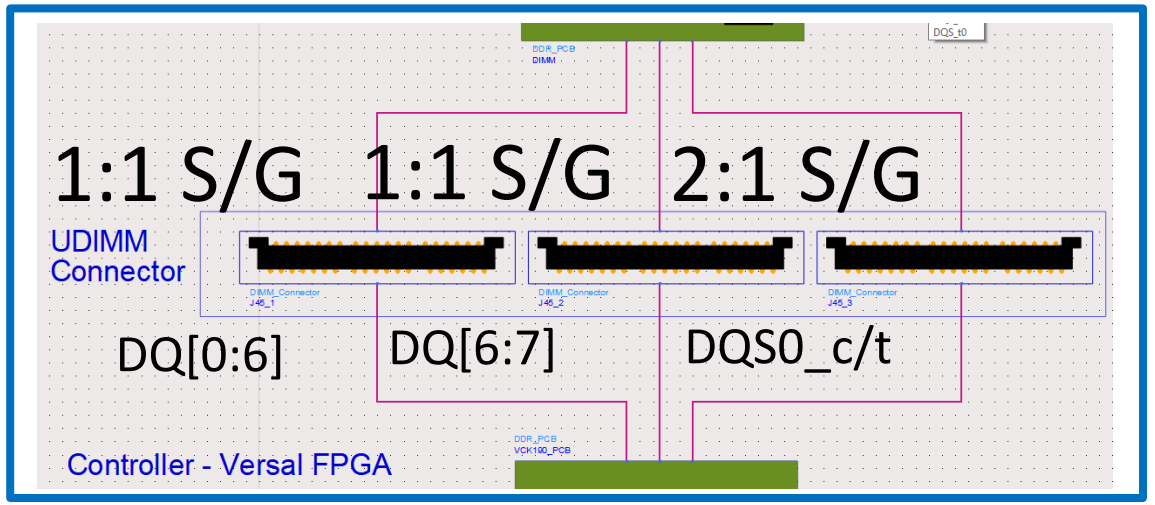
To simulate complete DDR4 byte lane:

- **Only 6 through ports available on 1:1 S/G model**
  - => 2 instances used for DQ[0:7]
- **2:1 S/G model used for Differential pairs (DQS0_t/DQS0_c)**

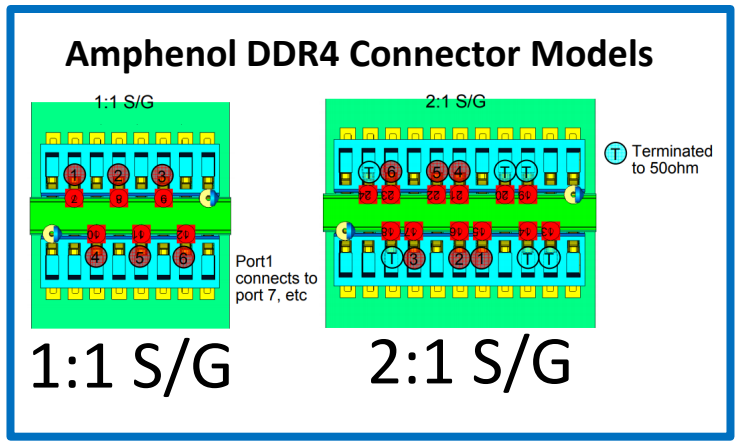
For the connector model in Memory Designer……

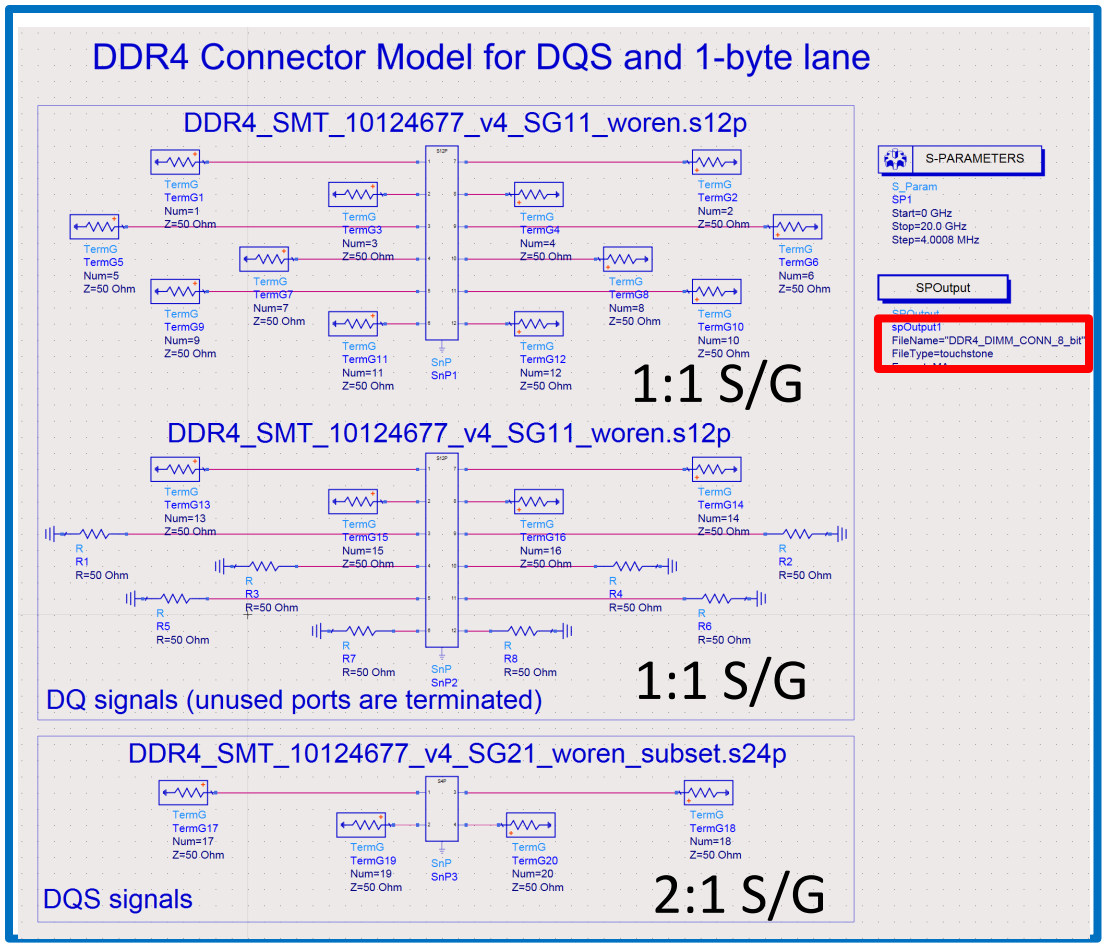
Is this the best way to setup the connector model?





DIMM Connector Channel Model Setup





New SP file exported to Memory Designer

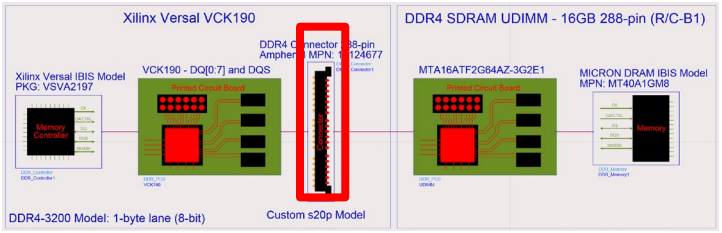
DDR4_DIMM_CONN_8_bit.s20p

Here is the better way to model your DDR4 Connector

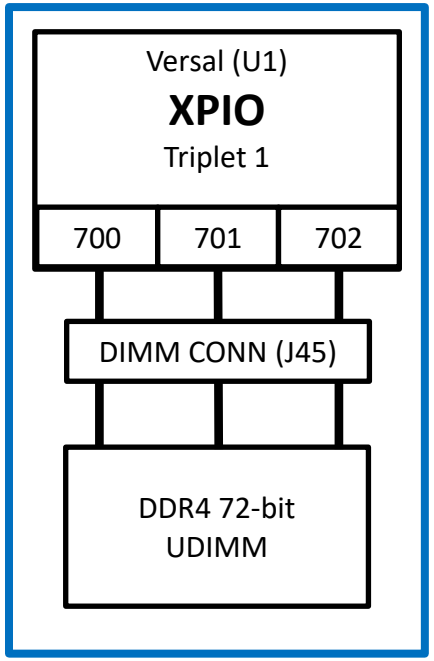
To simulate complete DDR4 byte lane:

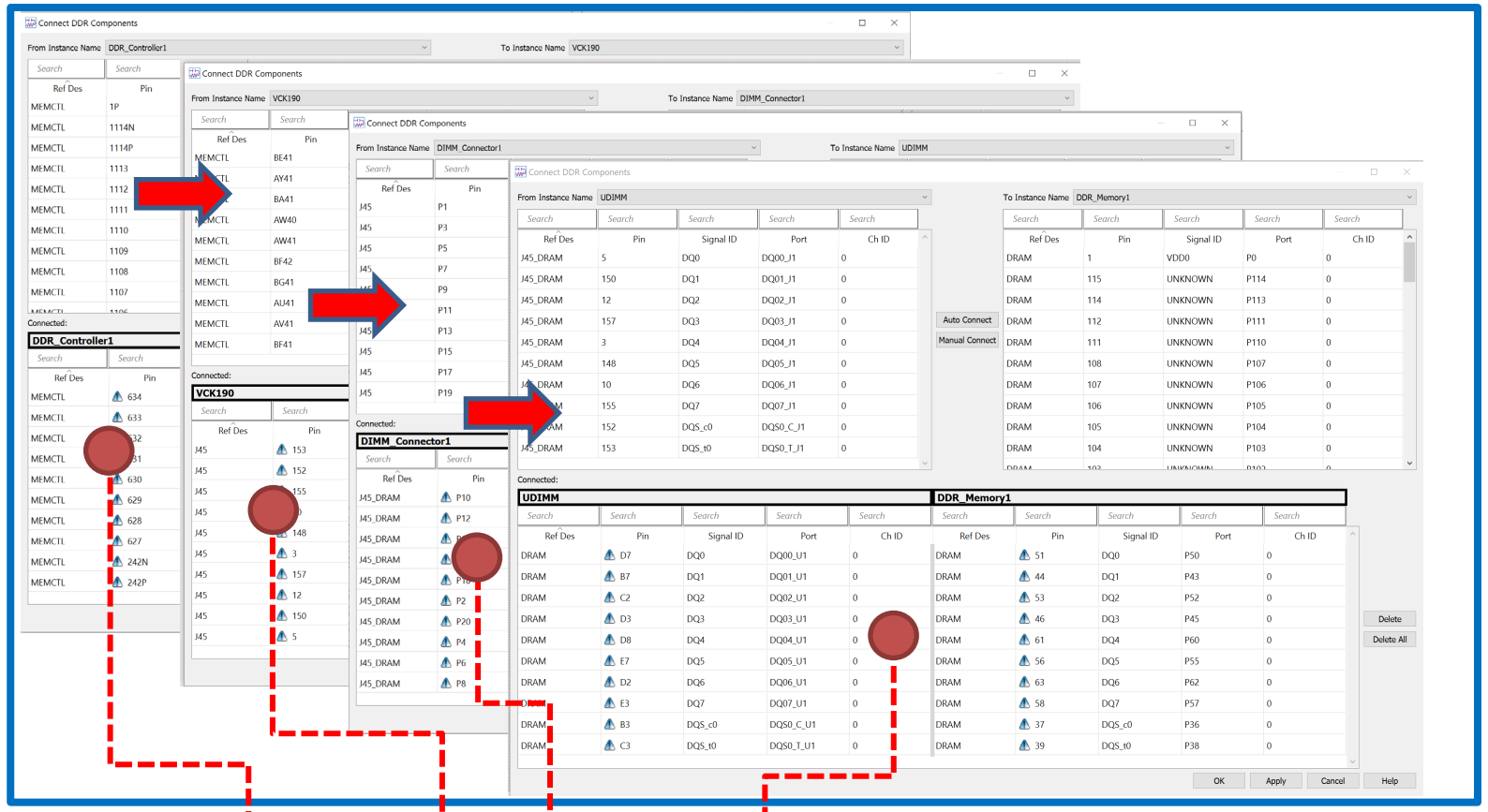
- **(x2) 1:1 S/G combined with (x1) 2:1 S/G to create s20p model**

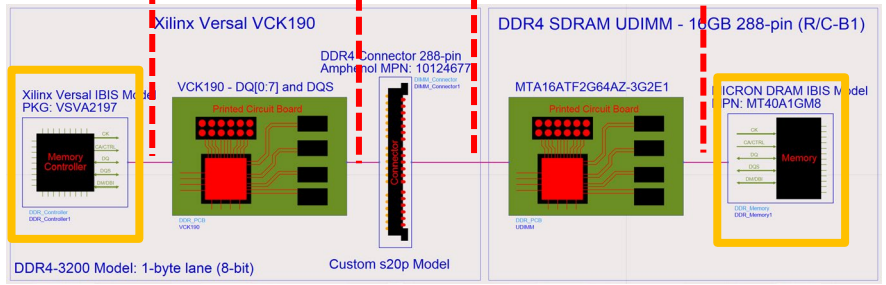
=> Only one DIMM connector instance for DQ[0:7] and DQS0_t/DQS0_c



Channel Model Port Connection and IBIS Model Setup





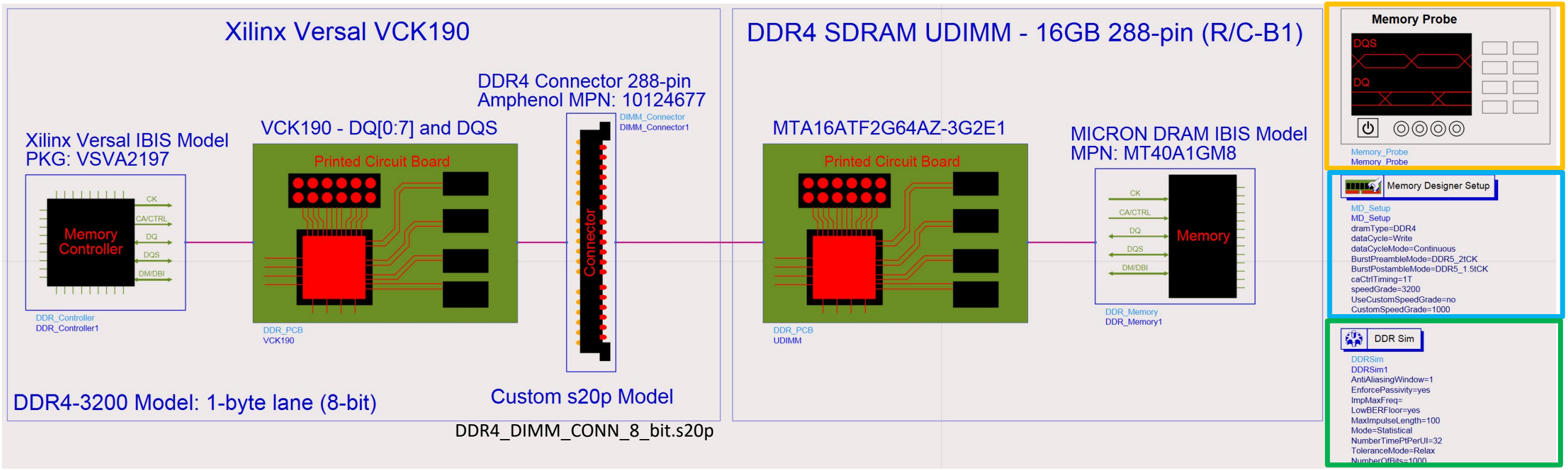


Memory Controller IBIS Models

- DQx – XP_POD12_xx
- DQS_c – XP_DIFF_POD12_xx_N
- DQS_t – XP_DIFF_POD12_xx_P

Select correct IBIS models and enable for Memory Controller and Memory

DDR4 Channel Model Setup on VCK190 with UDIMM



Setup Memory Probe (e.g. Select signals, set parameters)

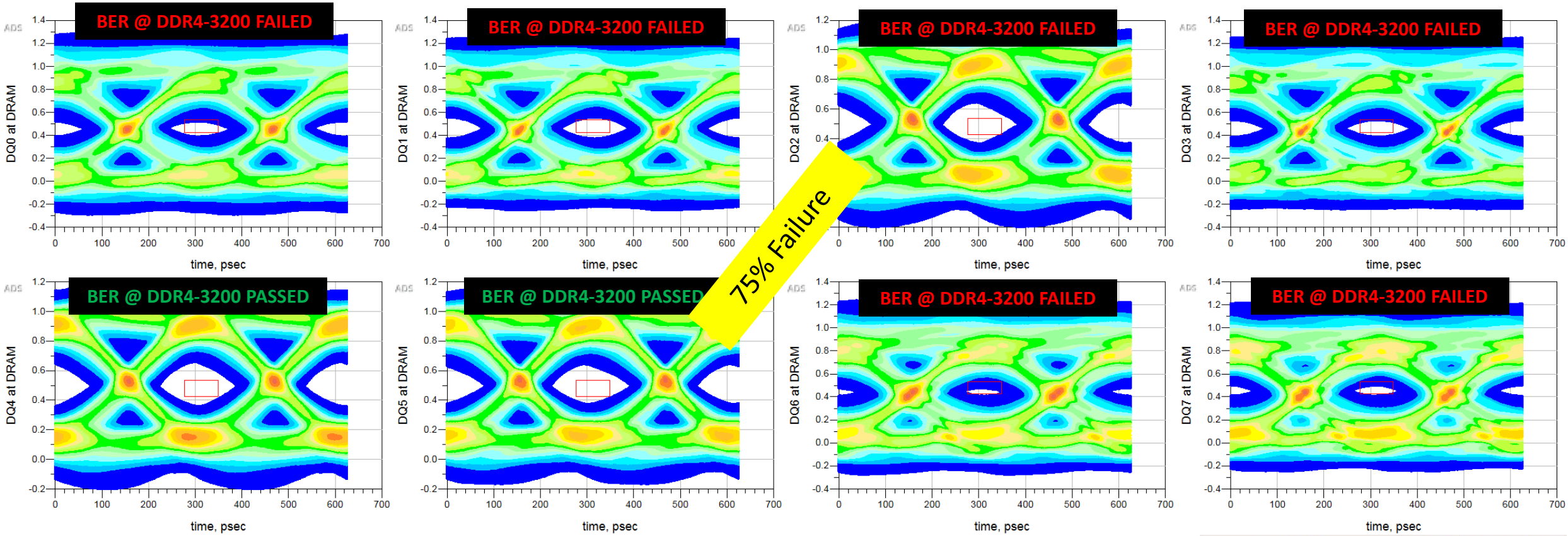
Select Correct Speed Grade and dataCycle

Ensure LowBERFloor = yes (to set simulation BER = 1E-16)

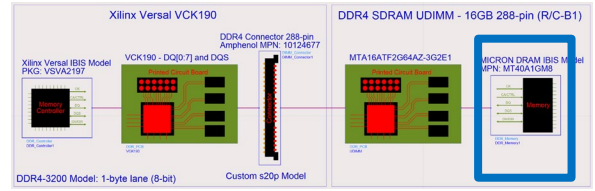
>>>>> READY TO SIMULATE!!!

Eye Diagram Initial Results DQ[0:7] for Write at DRAM

**DQ eye mask shown is for JEDEC DDR4-3200 to achieve BER 1E-16. Same eye mask for all test cases.

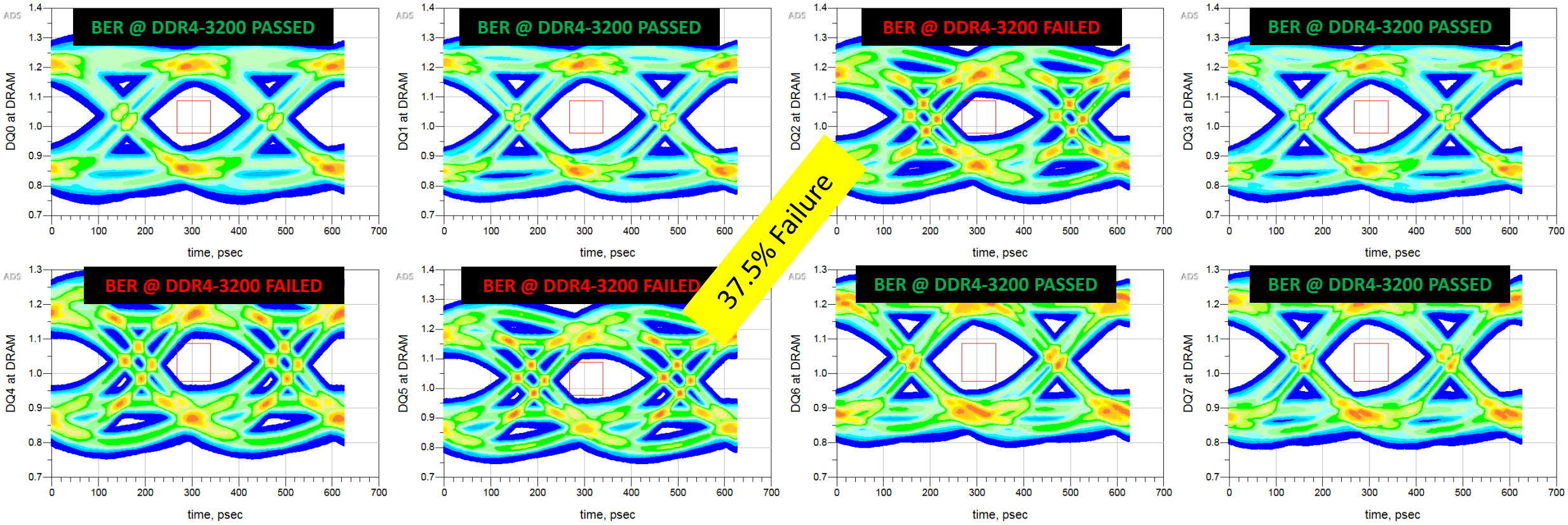


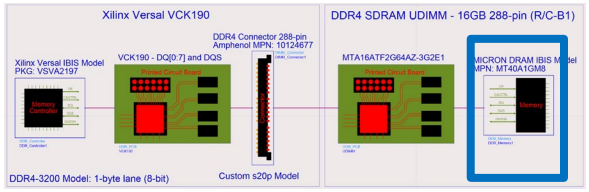
- Using Default DRAM IBIS Setting **DQ_ODT = OFF**



Eye Diagram Results DQ[0:7] for Write at DRAM with ODT

**DQ eye mask shown is for JEDEC DDR4-3200 to achieve BER 1E-16. Same eye mask for all test cases.





DRAM DQ_ODT = 60 Ω (arbitrarily selected)

- => Improved Results Achieved!
- There must be a better way to tune the channel for SI!!

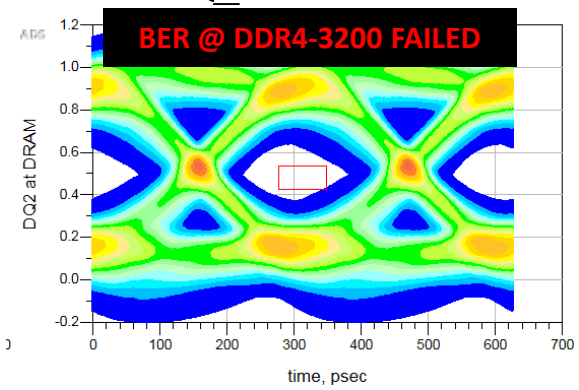
Eye Diagram (DQ2) Write Results at DRAM - ODT tuning

```
BATCH SIMULATION
BatchSimController
BatchSim1
Var= Start=1.0 Stop=10.0 Step=1.0 Lin=
UseSweepPlan=no
Analysis[1]="DDRSim1"
UseSweepModule=yes
SweepModule="CSV_List"
SweepArgument="DRAM_ODT_Sweep_8bit.csv"
UseSeparateProcess=yes
MergeDatasets=yes
RemoveDatasets=no
```

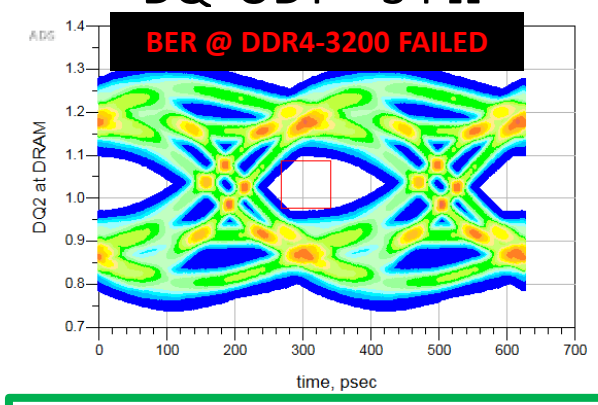
Use a BATCH SIMULATION to tune ODT values on the DRAM

**DQ eye mask shown is for JEDEC DDR4-3200 to achieve BER 1E-16. Same eye mask for all test cases.

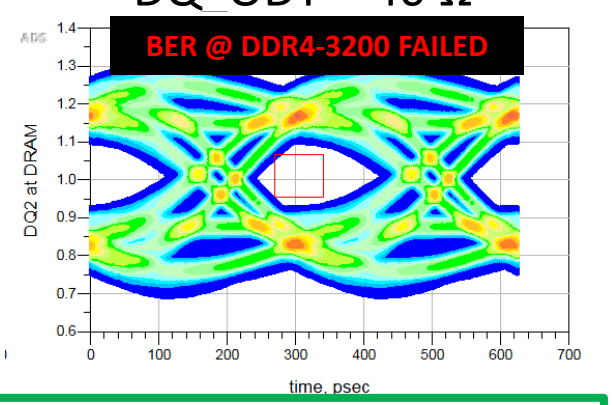
DQ_ODT = OFF



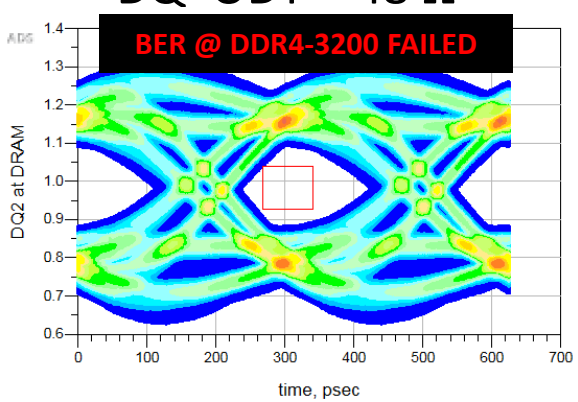
DQ_ODT = 34 Ω



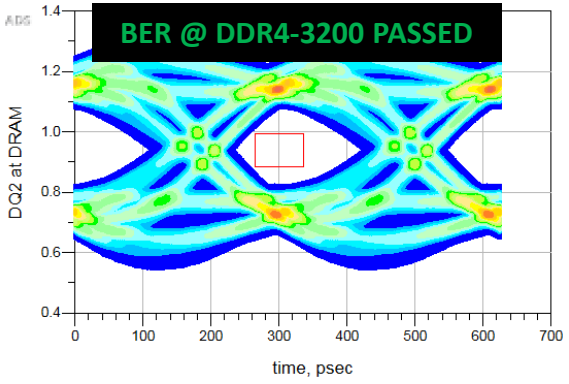
DQ_ODT = 40 Ω



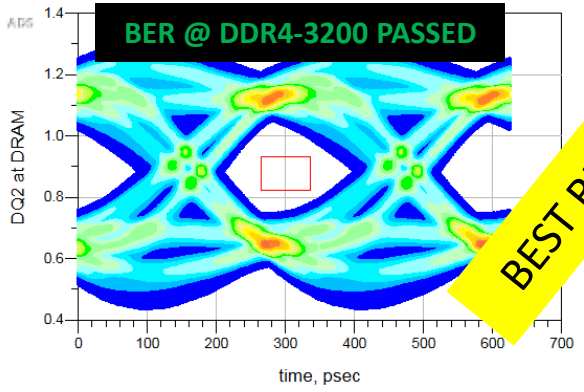
DQ_ODT = 48 Ω



DQ_ODT = 60 Ω

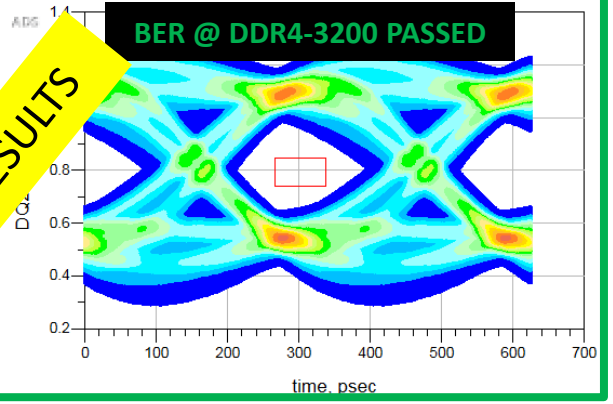


DQ_ODT = 80 Ω

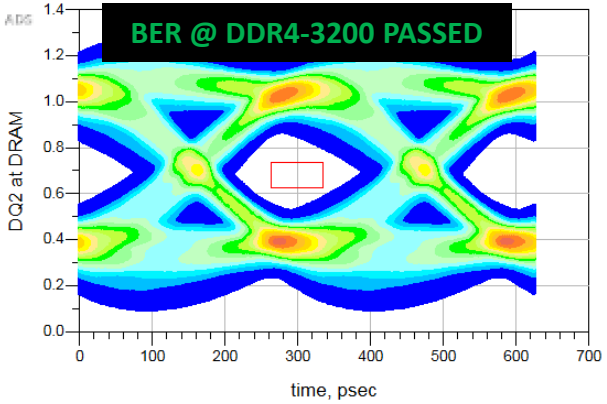


BEST RESULTS

DQ_ODT = 120 Ω



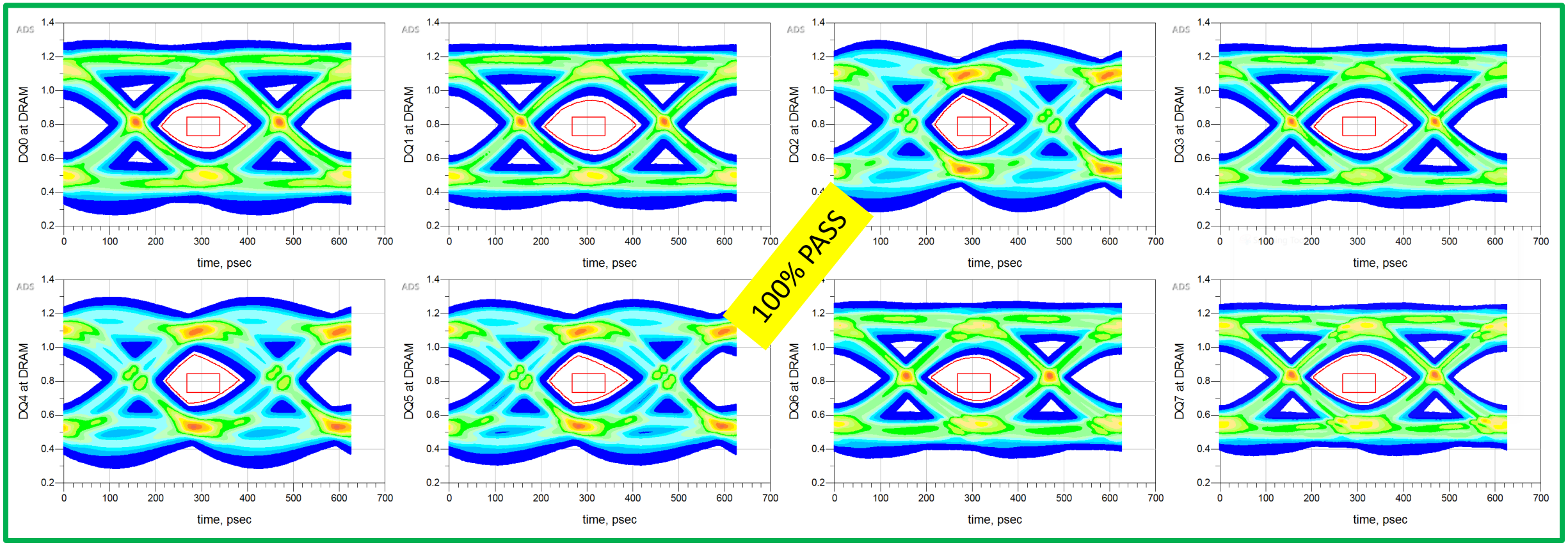
DQ_ODT = 240 Ω

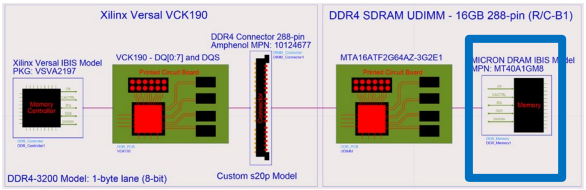


Eye Diagram Results DQ[0:7] for Write at DRAM (post-tuning ODT)

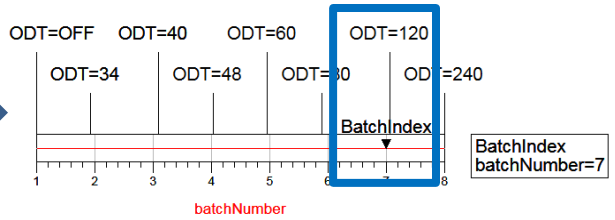
BER @ DDR4-3200 PASSED

**DQ eye mask shown is for JEDEC DDR4-3200 to achieve BER 1E-16. Same eye mask for all test cases. BER Contour shown for 1E-16





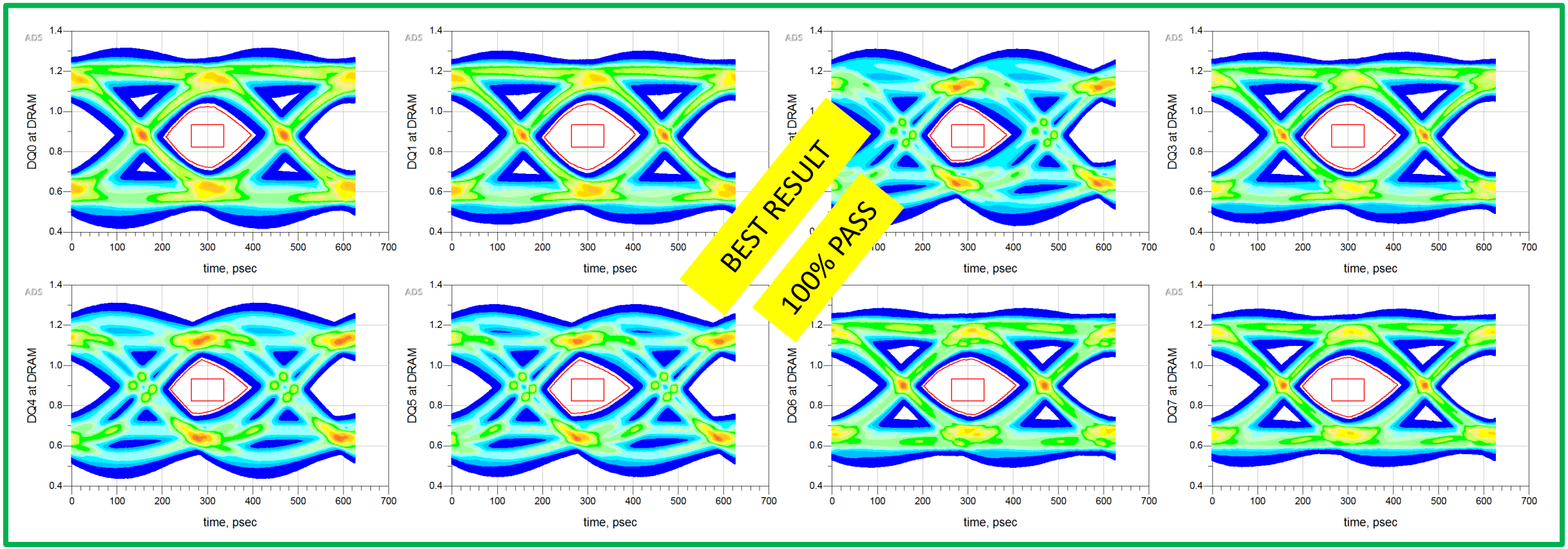
ALL DRAM DQ_ODT = 120 Ω

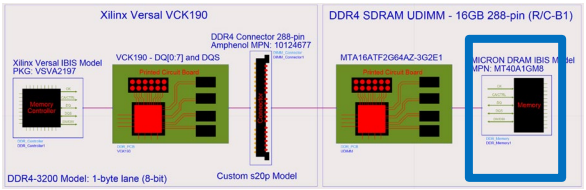


Eye Diagram Results DQ[0:7] for Write at DRAM (post-tuning ODT)

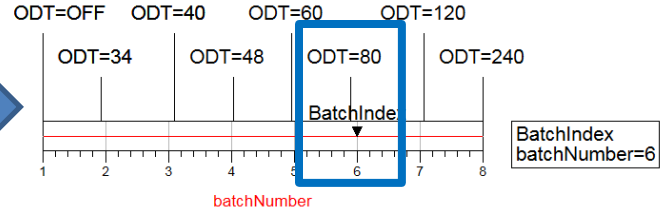
BER @ DDR4-3200 PASSED

**DQ eye mask shown is for JEDEC DDR4-3200 to achieve BER 1E-16. Same eye mask for all test cases. BER Contour shown for 1E-16





ALL DRAM DQ_ODT = 80 Ω

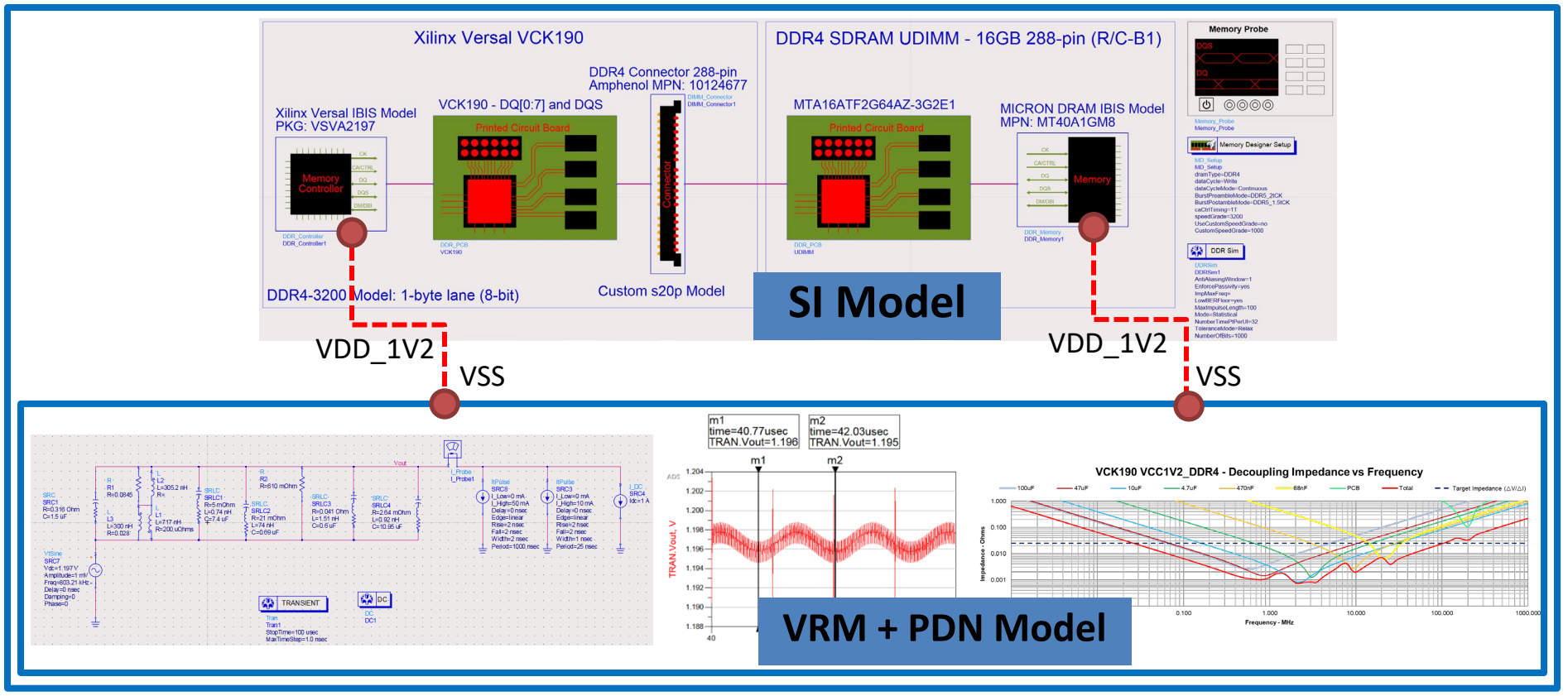


What's Next

- **Simulate Power-Aware SI model**
  - Includes PDN & Simultaneous Switching Noise (SSN)
  - IBIS v5.0 or later necessary for Power-Aware (makes VDD/VSS pins available)
- **Simulate with CLK, CMD, ADD**
- **Simulate complete DDR4 DQ bus**

  => More switching signals = greater di/dt => greater SSN
- **Enable EQ (CTLE)**
- **Jitter analysis**

Power Aware SI Model



Summary and Conclusions

- **Always verify the PCB stack-up on your design!**
- **The VCK190 DDR4-3200 Solution Passes with UDIMM**
  - This model didn't include Jitter or other noise (SSN) from Power Sources
- **Using a Power Aware SI model with a complete DQ bus will increase di/dt increasing ISI, jitter, and crosstalk**
  - Enabling EQ will be required to improve these results to meet DDR4 eye mask compliance
- **DDR5 is here! => Smaller UI means more challenging SI problems**

  ==> Shrinking margin, equalization required, correlated/non-correlated jitter tracking, unmatched IO conditions, etc.

Thank You for Attending

Any questions?

Source: dilbert.com

Let's connect!

Message me with subject line as "EDICon 2020" on:

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