DDR4-3200 FPGA Based System with Interposer Power-Aware SI Simulation to Measurement Correlation

Benjamin Dannan, Northrop Grumman
Randy White, Keysight Technologies

Benjamin Dannan (Northrop Grumman), Randy White (Keysight Technologies), Hermann Ruckerbauer (EyeKnowHow), HeeSoo Lee (Keysight Technologies)

SPEAKERS

Benjamin Dannan

Technical Fellow & Staff Digital Engineer, Northrop Grumman

benjamin.dannan@ngc.com | northropgrumman.com

Benjamin Dannan is a Technical Fellow and a Staff Digital Engineer at Northrop Grumman Mission Systems. He has a BSEE from Purdue University, a Masters of Engineering in Electrical Engineering from The Pennsylvania State University, and graduated from the USAF Undergraduate Combat Systems Officer training school with an aeronautical rating. He received the prestigious DesignCon best paper award in 2020 and is a Keysight Certified Expert in ADS.

Randy White

Memory Solutions Program Manager, Keysight Technologies

randy.white@keysight.com | keysight.com

Randy White is the Memory Solutions Program Manager for Keysight Technologies. He is focused on test methodologies for emerging memory technologies in server, mobile, and embedded applications. He has participated on many standards committees including PCI-SIG, USB-IF, SATA-IO, JEDEC to help define new test methodologies, and is currently the chair of the JEDEC JC40.5 Logic Validation subcommittee. He graduated with a BSEE from Oregon State University.

Today's Key Takeaways

- To validate design performance on one of the first DDR4-3200 FPGA memory controllers as well as verify whether the design's electrical performance meets the JEDEC specifications through power aware simulations and measurements. These power aware simulations will look at the effects of SSN/SSO while including the effects of probe loading and a memory component interposer that is present during the measurement.

- This effort will look at EM extracted models from a 3D solver and show considerations to properly simulate with these models. While concluding with actual measurement correlation being done on the same simulated DDR4-3200 model.

Overview

- Big Data Evolution
- Background on Interposers
- Measurement Setup with Interposer
- DDR4-3200 Measurement Results
- Simulation Setup
- Simulation Results
- DDR5 Channel Reflections and DFE Considerations
- DDR5 Golden Channel
- Next Steps
- Conclusion
- Questions

Big Data Evolution

- The era of “Big Data”
- Global “Big Data” consumption increased 5000% between 2010 and 2020
- Data usage increased from 1.2 trillion GB to ~60 trillion GB
- By 2025, estimated that over 463 Exabytes (463,000 Petabytes) of data created each day (212,765,957 DVDs)
- Memory bandwidth continues performance scaling to meet requirements of the next-generation data center, IoT, and other high-speed applications
- Increased pressure from “Big Data” means SI engineers need to ensure high-speed memory designs will work

Source: The Evolution of Big Data
https://www.qubole.com/blog/big-data-evolution/

Measurement Platform

XILINX VCK190

- Xilinx Versal ACAP
- Validate DDR4-3200 Speed
- Hardened integrated DDR Memory Controller (DDRMC) + soft memory interface IP options
- AXI Traffic Generator used to exercise memory IP in both simulation and post-synthesis for hardware analysis

Source: Xilinx.com

Background on DDR4 SSN

WHAT IS SSN

- **Parallel single-ended signaling always suffers from Simultaneous Switching Noise (SSN)**
  - On Die and on package power delivery is never perfect, and will introduce VDD/GND dips/bounces that will be seen on the signals, as the driver is supplied by VDD and GND
  - Single ended push/pull drivers will cause a significant $\frac{dI}{dt}$ where any impedance (usually defined by inductance) will cause noise on the voltage rail that supplies a set of e. g. 11 output drivers (8* DQ, 1*DM/DBI, 2*DQS)
    - *Differential interfaces (e. g. CML) usually are loading the power rails with more DC like current*
- **It is not just switching all TX outputs (SSO), but also when receiving and terminating many parallel signals this can introduce significant on-die noise, potentially disturbing internal circuitry.**
- **Experience shows, that quite often the Controller package is the limiting factor, as it is difficult to provide low inductive power planes, as an example:**
  - 11 signals per byte lane (DQ/DM/DQS) * 9-byte lanes * 2 channels = 198 output drivers that might switch in parallel!

Background on DDR Power Aware Simulations

SSN AND SSO IMPACTS TO DDR MODELING

- **Simultaneous switching output noise, in single-ended signaling, is one of the major performance limiters as data-rates scale higher**

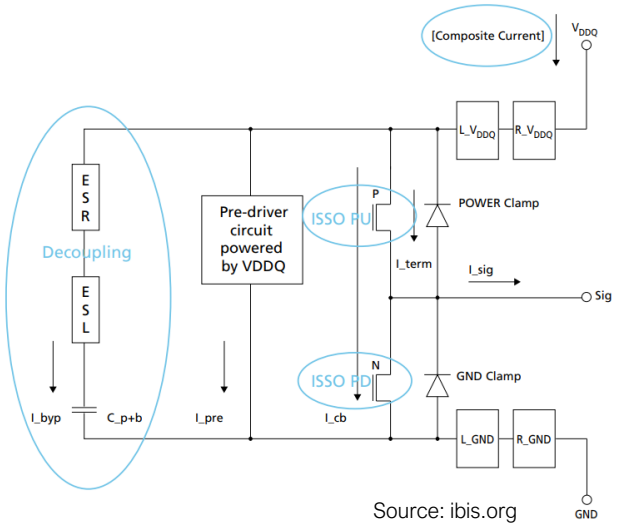
- **Output drivers are major contributors of noise in the system**
  - Power Supply noise and current profile are important in SSO simulations

- **Latest generation DDR4 and next-generation DDR5 solutions, simulations need to include SSN, and therefore power-aware SI simulation modeling is necessary.**

- **Today's SI engineers need to be able to do both SI and PI when it comes to modeling DDR interfaces**

PI Modeling requires [Composite Current], [ISSO PU], [ISSO PD], & IBIS ISS on-die decoupling circuit model

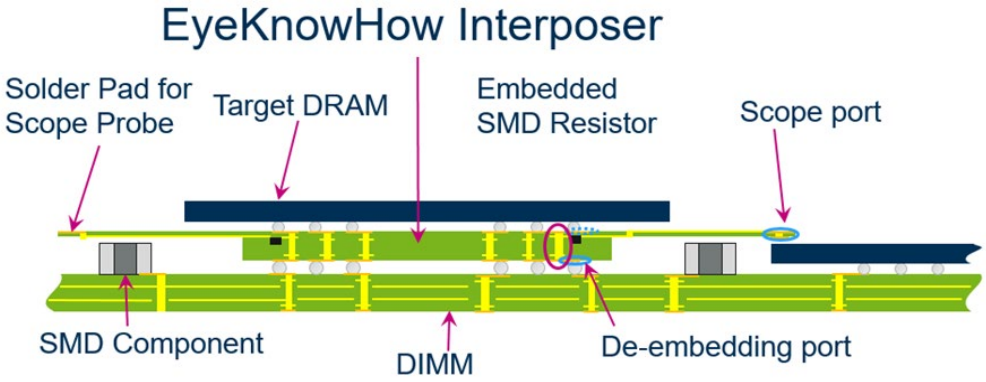
This is defined in the IBIS Model



Source: ibis.org

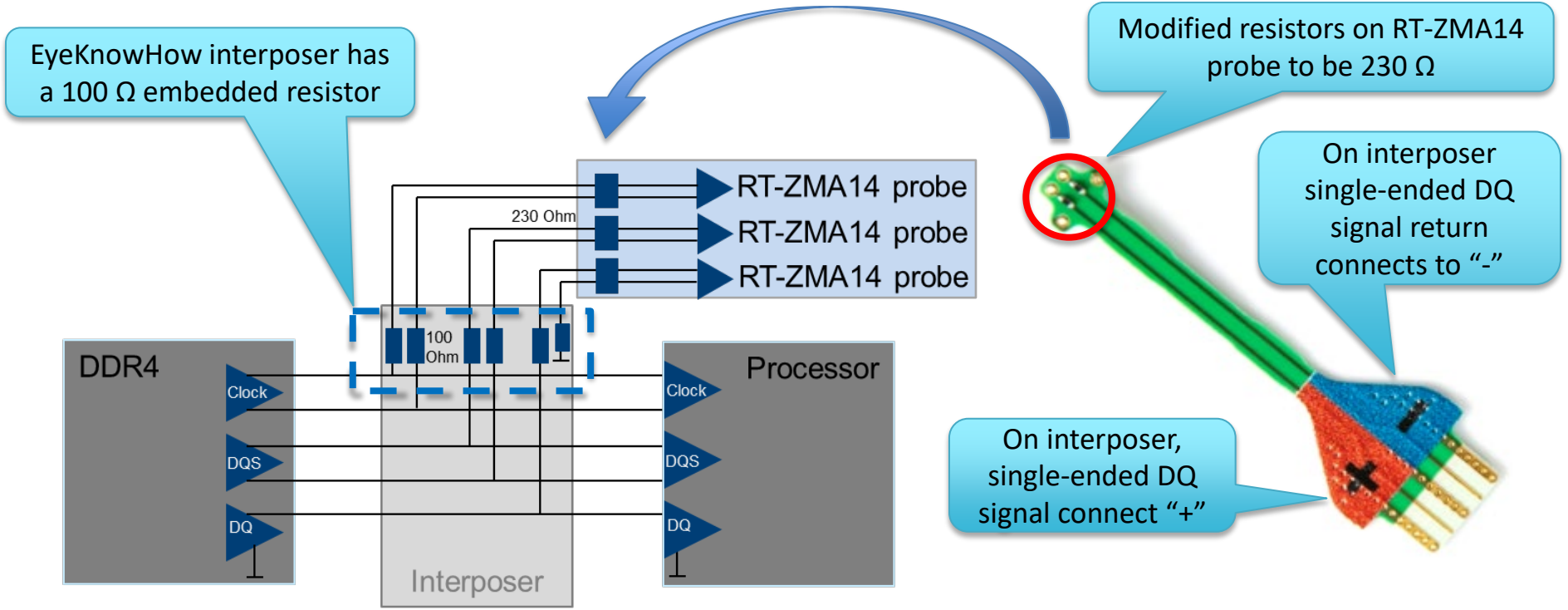
Background on Interposers

- **BGA component interposer for signal access**
- **Interposer model**
  - 2- or 4-port for simulation loading
  - 3- or 6-port for oscilloscope de-embedding
- **Probing side includes series resistor to minimize reflections**
  - Different types of active scope probes will react differently (e.g. due to the change of source impedance of the DUT)
  - Dependent on the type of probe a modification of the input resistors is required (see next slide)



Source: EyeKnowHow.de

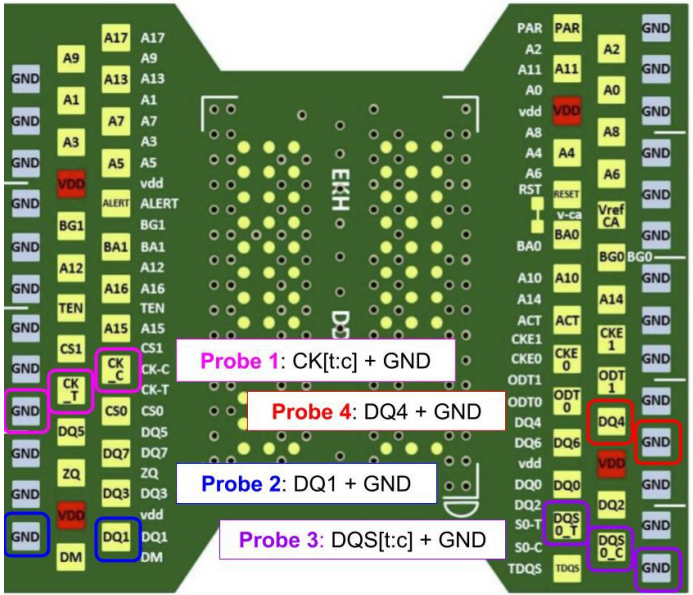
Measurement Setup with Interposer



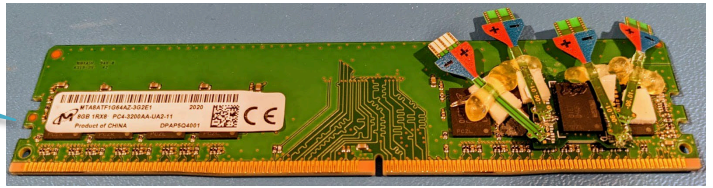
Source: "Deembedding of DDR Interposer" by Guido Schulze, April 2020 Rohde & Schwarz

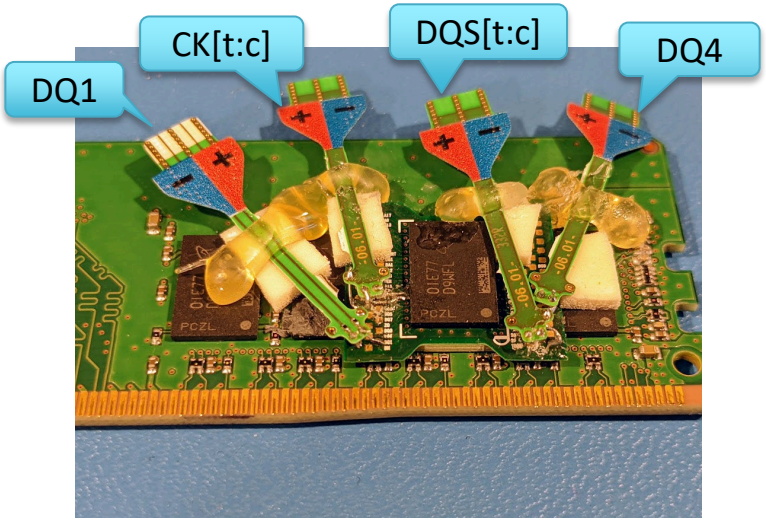
Measurement Setup with Interposer

INTERPOSER PROBE SETUP WITH UDIMM



Micron R/C A2
UDIMM

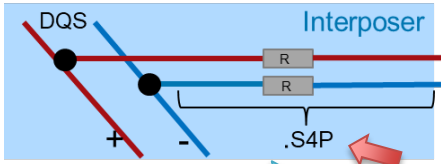




Measurement Setup with Interposer

DE-EMBEDDING THE INTERPOSER

De-embedding DQS requires 2 models (red arrows)

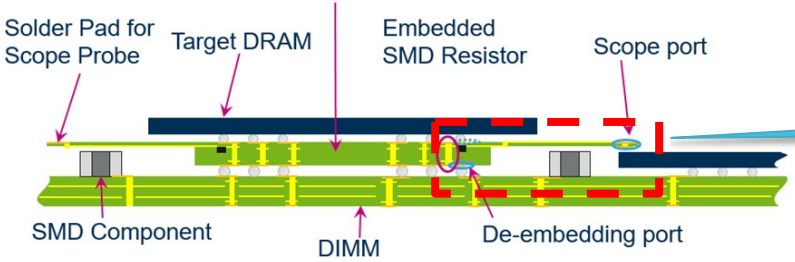


Provided from R&S

.S4P

Provided from EKH

EyeKnowHow Interposer

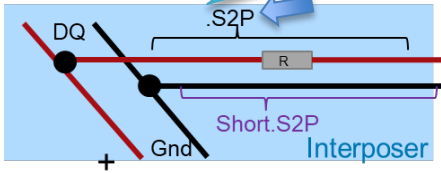


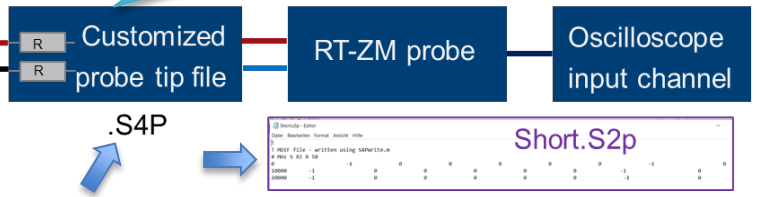
What is being de-embedded during measurement

Provided from EKH

Provided from R&S

De-embedding DQ requires 3 models (blue arrows)





.S4P

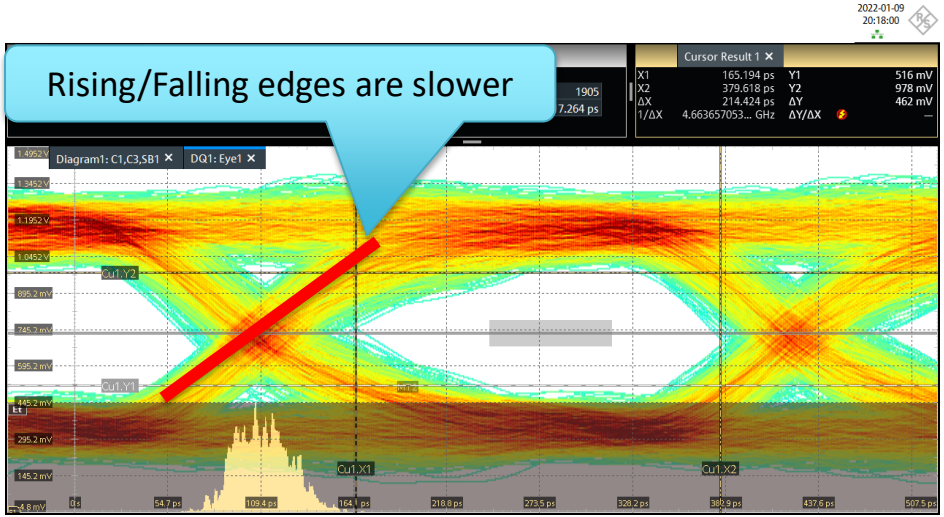
Source: "Deembedding of DDR Interposer" by Guido Schulze, April 2020 Rohde & Schwarz

Measurement Setup with Interposer

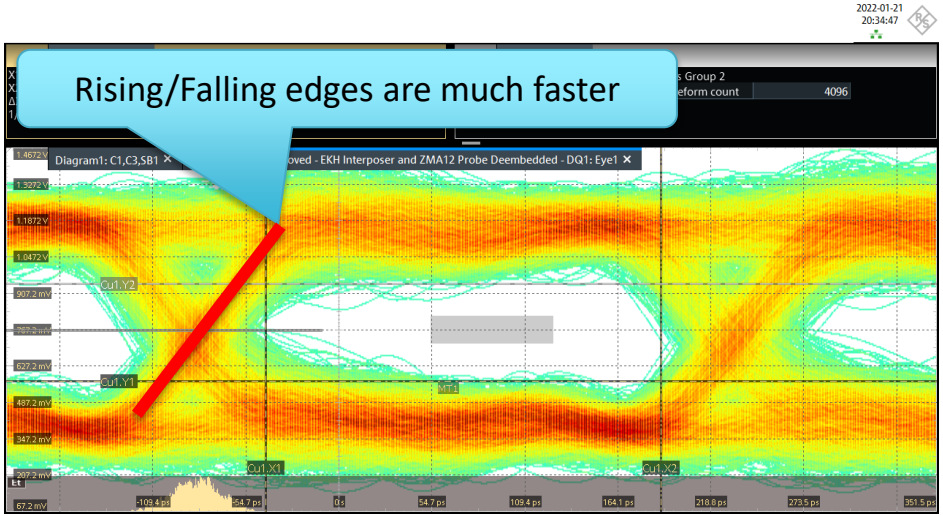
WHY DE-EMBEDDING THE INTERPOSER MATTERS

***Both measurement results shown are without Probe Loading**

BY DE-EMBEDDING THE CORRECT EYE SHAPE CAN BE CAPTURED DURING MEASUREMENT!



INTERPOSER ***NOT*** DE-EMBEDDED

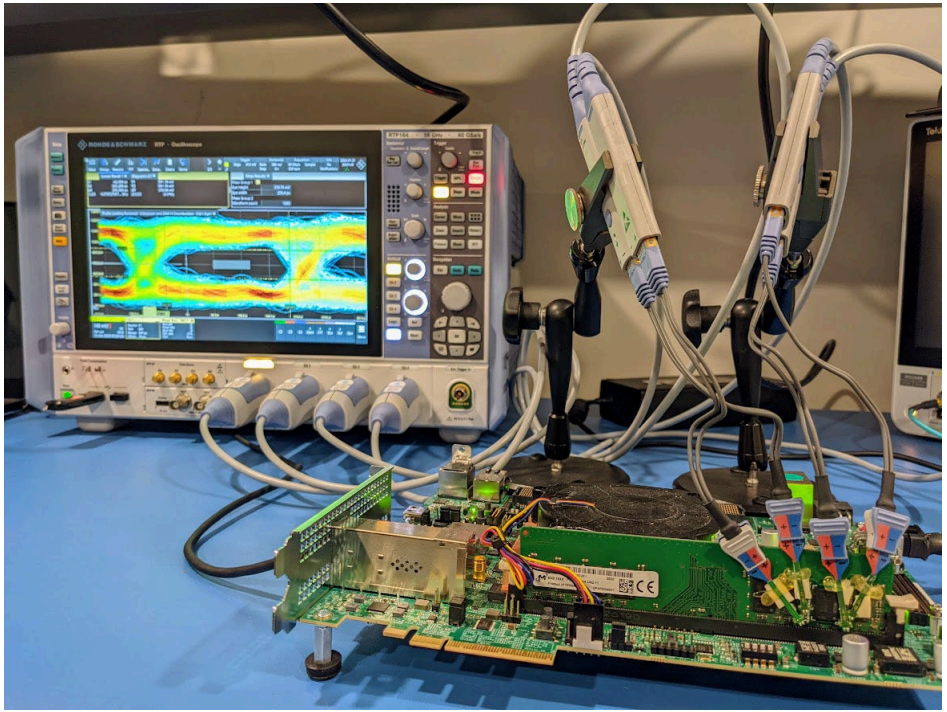


INTERPOSER DE-EMBEDDED

Measurement Setup with Interposer

MEASUREMENT PLATFORM WITH R&S RTP164 SCOPE

- R&S RTP164 16GHz BW Oscilloscope
- RT-ZM160 – 16GHz Modular Probe
- RT-ZMA14 Probe Tip (modified w/230Ω resistor)

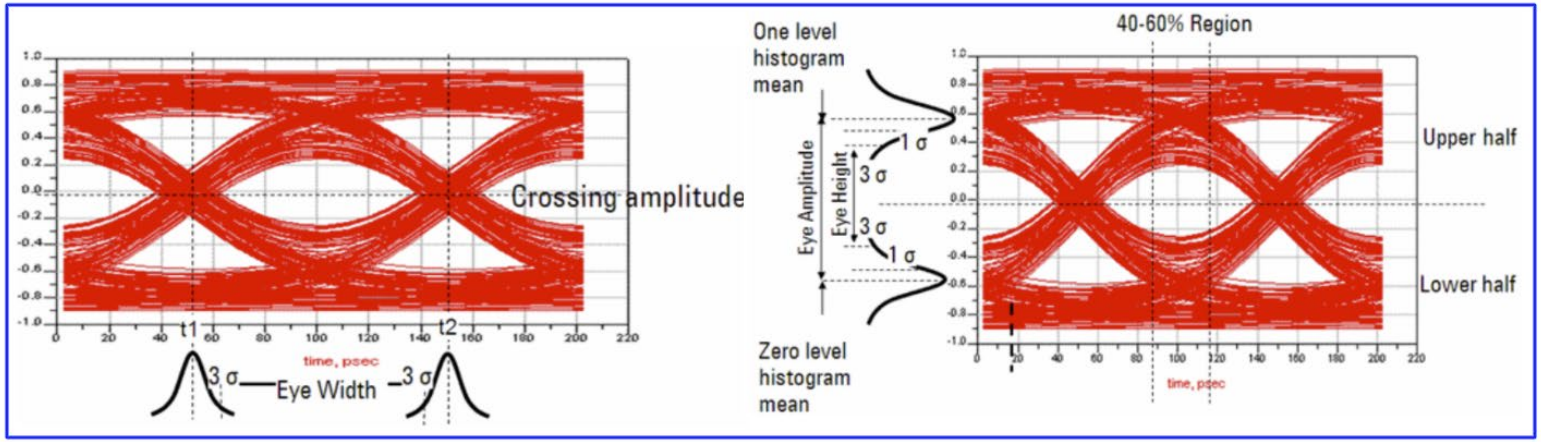


Eye Width and Eye Height Measurements

- **R&S RTP164 and Keysight PathWave Memory Designer use the same equations to calculate Eye Width and Eye Height**

$$Eye\ Width = (t_2 - 3 \cdot \sigma_2) - (t_1 + 3 \cdot \sigma_1)$$

$$Eye\ Height = (Level1 - 3 \cdot \sigma_{LEVEL1}) - (Level0 + 3 \cdot \sigma_{LEVEL2})$$



SOURCE: http://literature.cdn.keysight.com/litweb/pdf/5989-9453EN.pdf

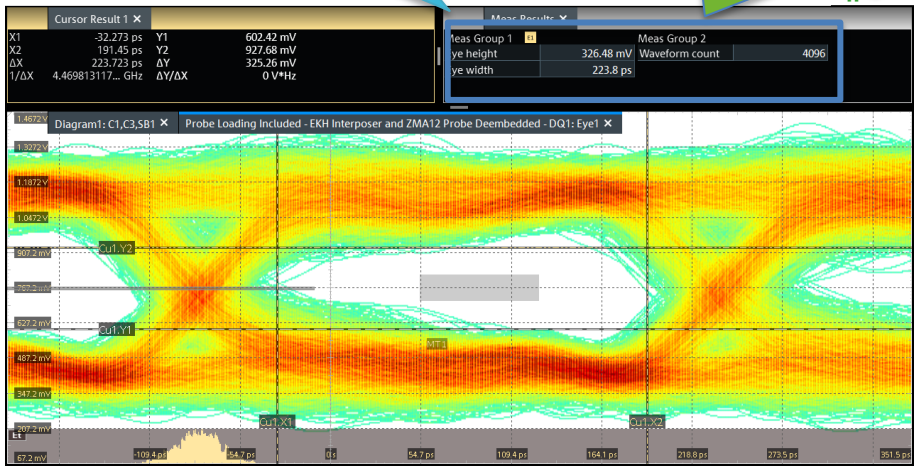
Measurement Results and Probe Loading

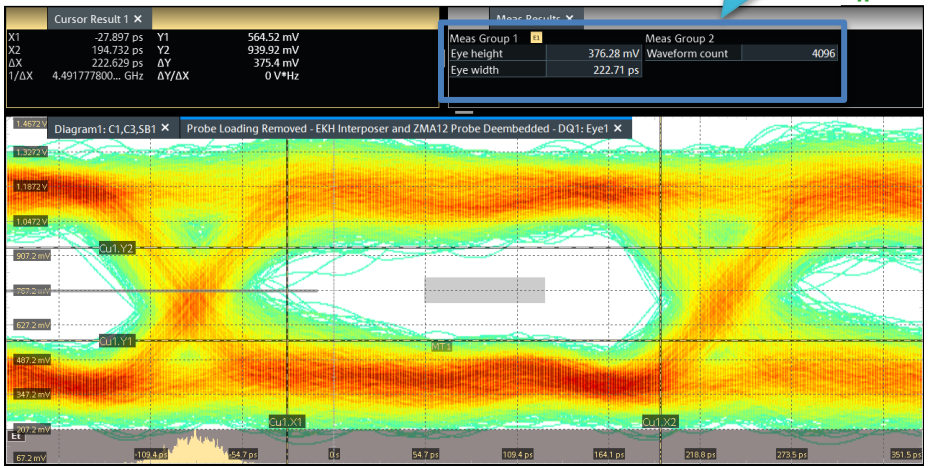
***Results shown are exact same measurement with and without Probe Loading**

Eye Height: **326 mV**
Eye Width: 223 ps

Probe loading reduces signal amplitude by 13%

Eye Height: **376 mV**
Eye Width: 222 ps





Probe Loading Included

Probe Loading Removed

Measurement Results

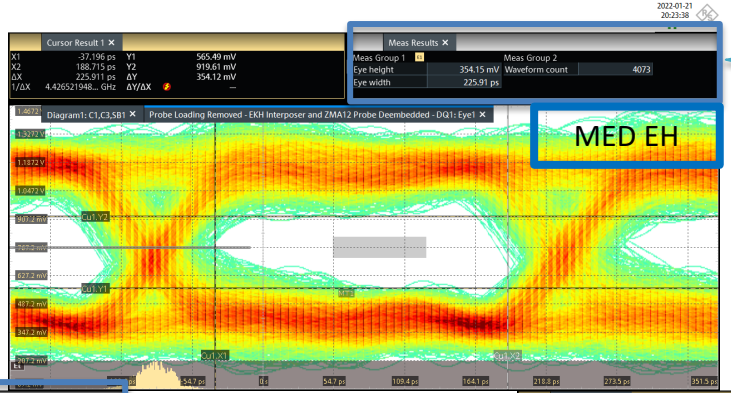
AVERAGE EYE HEIGHT AND EYE WIDTH – PROBE LOADING REMOVED

Average Eye Height: 348 mV

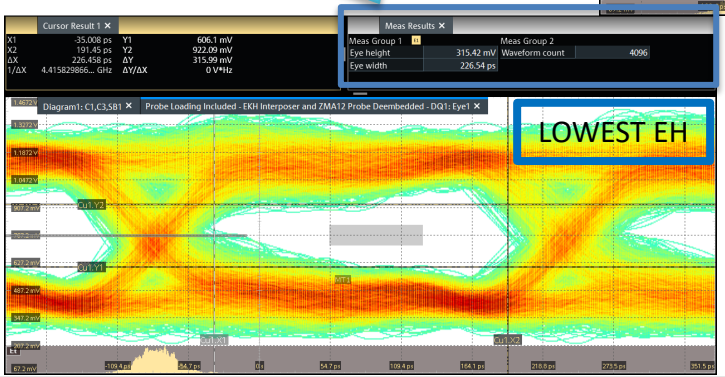
Average Eye Width: 228 ps

***Multiple measurements captured. Lowest, Medium and Highest Eye Height result was averaged**

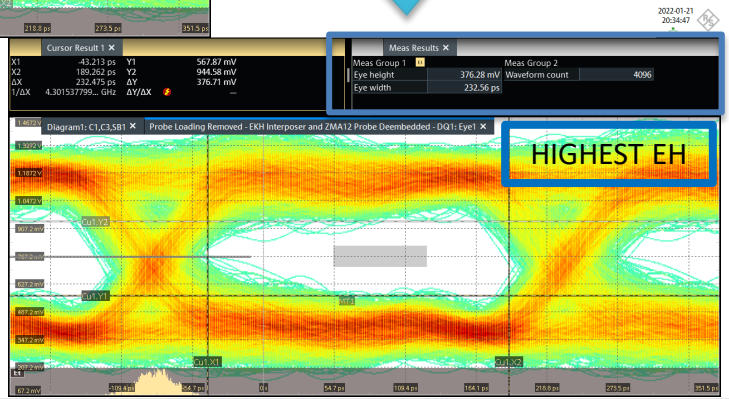
Eye Height: 354 mV
Eye Width: 226 ps



Eye Height: 315 mV
Eye Width: 226 ps



Eye Height: 376 mV
Eye Width: 232 ps

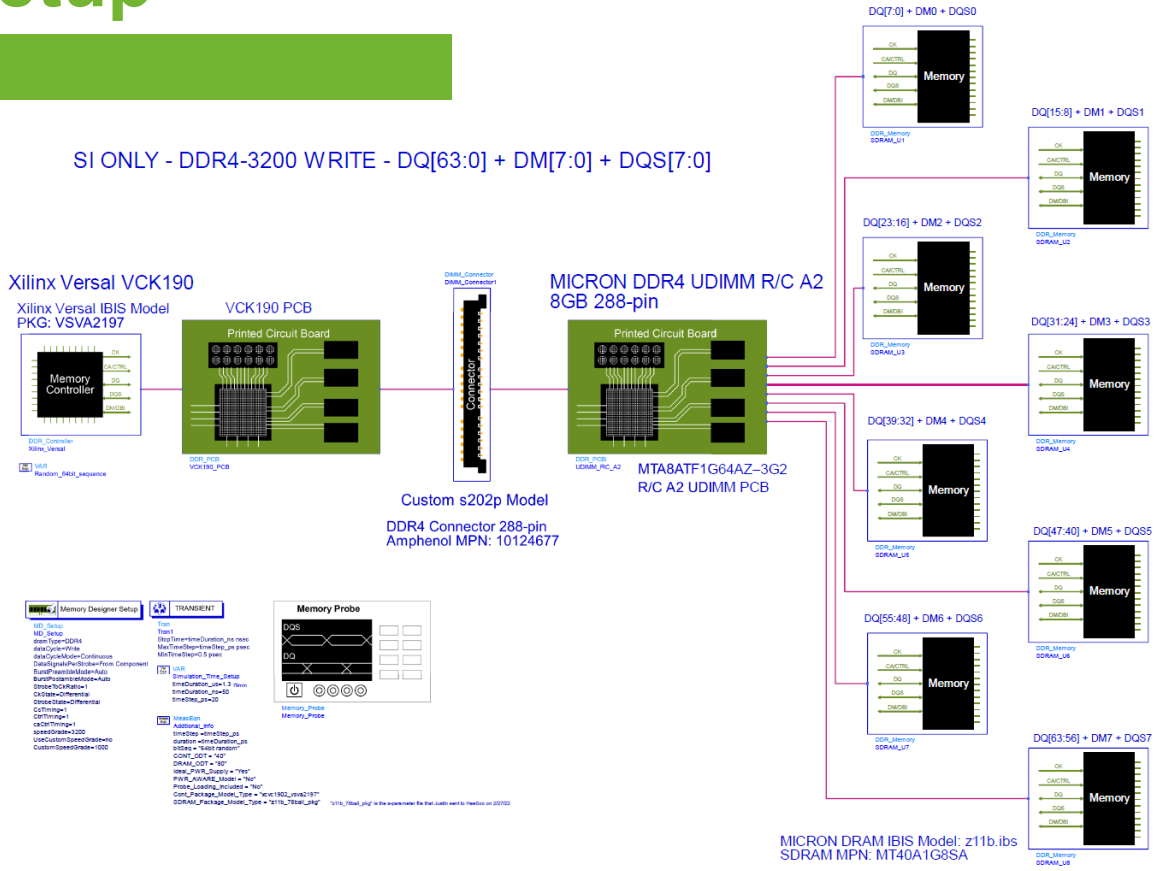


Simulation Model Setup

SI ONLY MODEL – DDR4-3200

Simulation Settings

- DDR4-3200 Speed Grade
- Pattern: 64-bit PRBS pattern across all 64 data bits
- SIM Duration: 1.3usec = 4160 bits across the channel
- Transient time step = 20ps

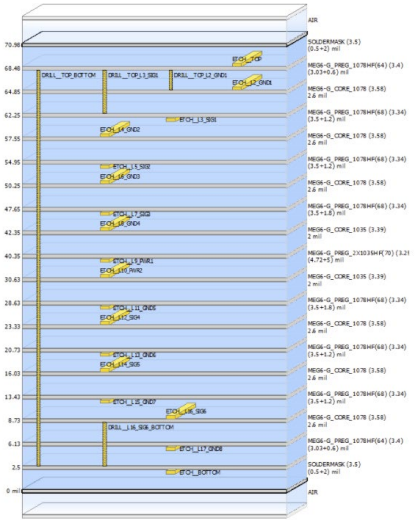


Simulation Model Setup

VCK190 PCB AND R/C A2 UDIMM PCB STACKUPS

- **SIPro used to create EM extracted models for SI nets**
  - ALL 8-byte lanes for DQ, DM, DQS nets were co-extracted together, on the VCK190 and UDIMM PCBs, to account for the net-to-net coupling
- **PIPro used to create EM extracted models for PDN on VCK190 and UDIMM**
- **All EM extracted models were fully passive and only some models had minor causality violations**
- **VCK190 PCB stack-up total thickness is 70.98 mil**
  - 18 total layers
- **UDIMM R/C A2 PCB stack-up total thickness is 1.442 mm (meets JEDEC UDIMM standard for thickness)**
  - 8 total layers

Xilinx VCK190 PCB Stack-up



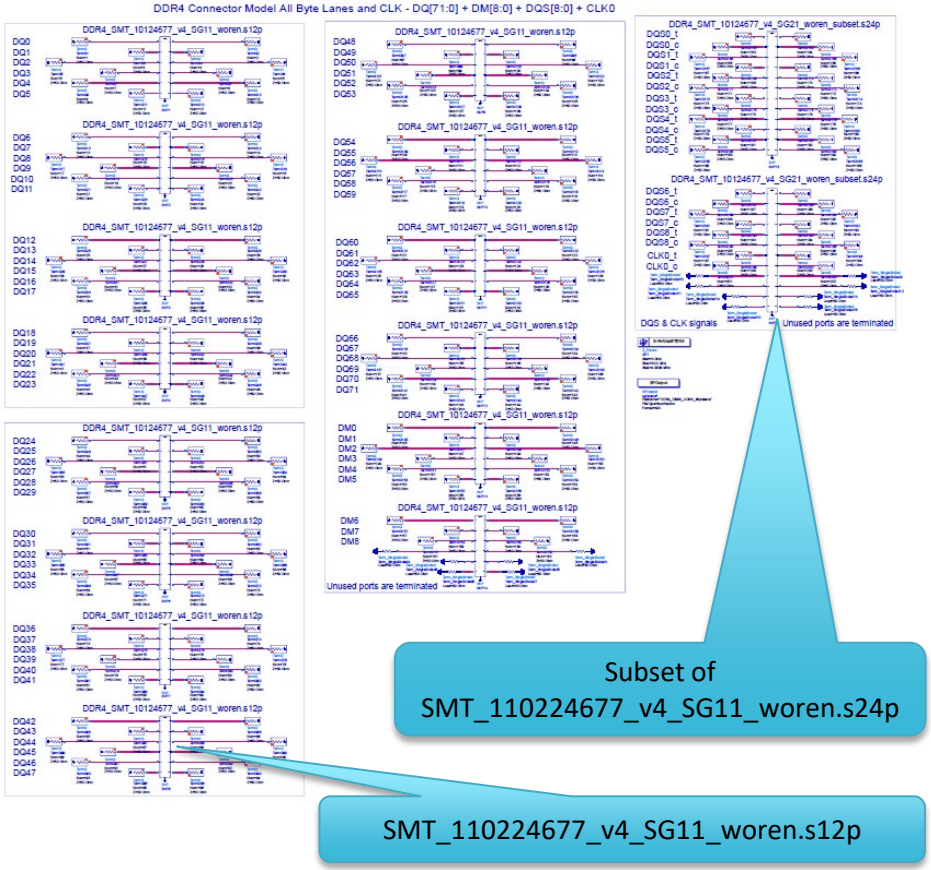
UDIMM PC4-3200 R/C A2 PCB Stack-up

NOTE: JEDEC UDIMM standard thickness is 1.4 +/-0.1 mm without solder mask

Simulation Model Setup

SETTING UP UDIMM CONNECTOR MODEL

- **Amphenol provides 12-port SG & 24-port SS touchstone models for DDR4 288-pin DIMM connector**
  - 202-port custom model generated for 9-byte lanes with CLK
- **A limitation is simulated crosstalk between byte lanes is limited at the connector to only signals within 12-port SG and 24-port SS model.**

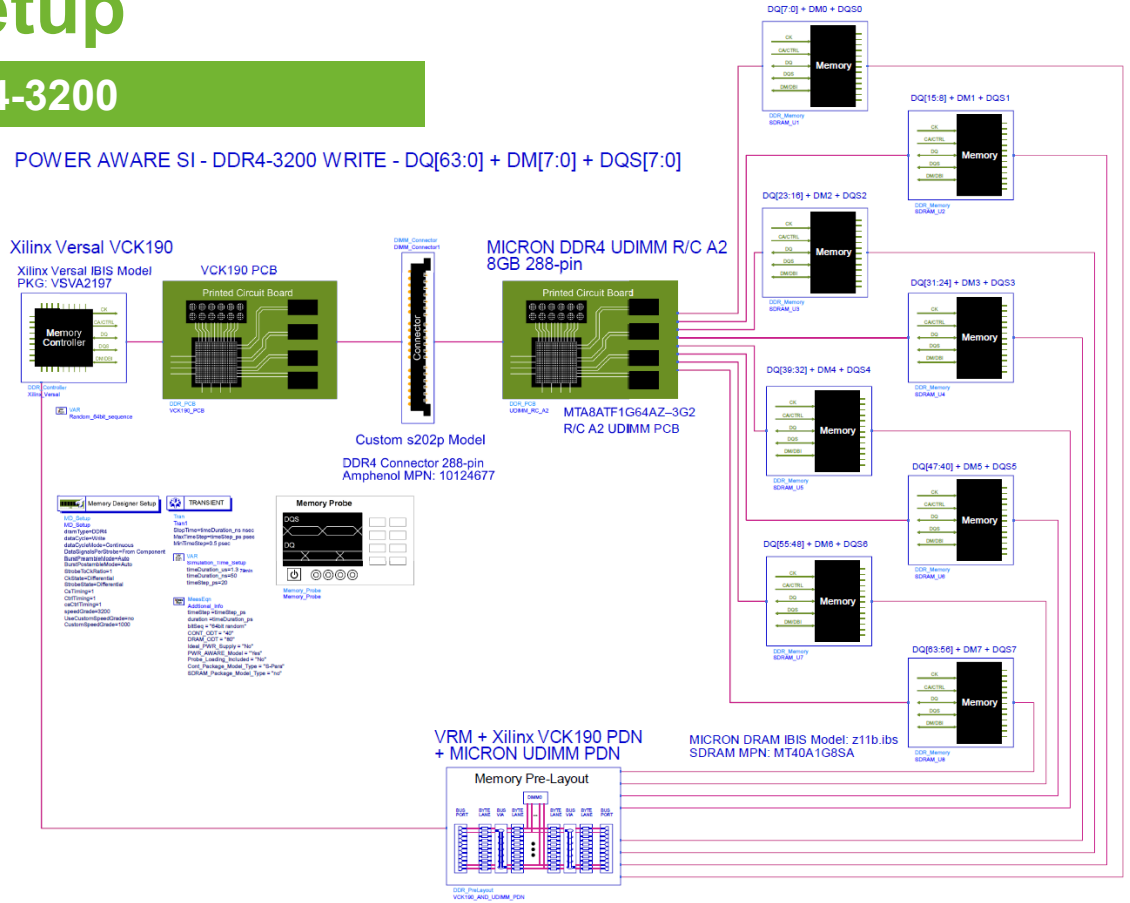


Simulation Model Setup

POWER AWARE SI MODEL – DDR4-3200

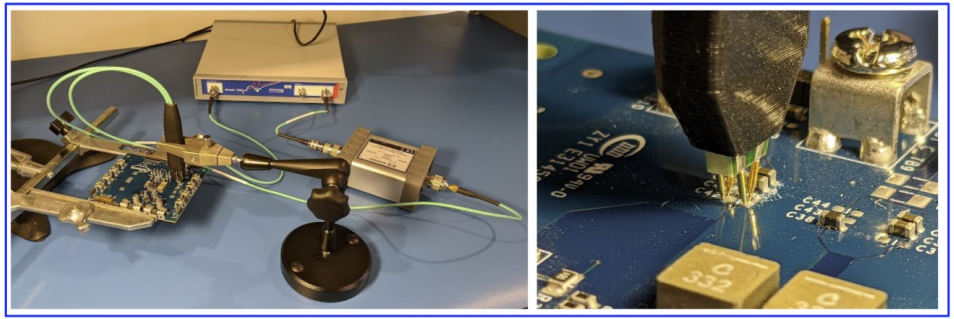
Simulation Settings

- DDR4-3200 Speed Grade
- Pattern: 64-bit PRBS pattern across all 64 data bits
- SIM Duration: 1.3usec = 4160 bits across the channel
- Transient time step = 20ps

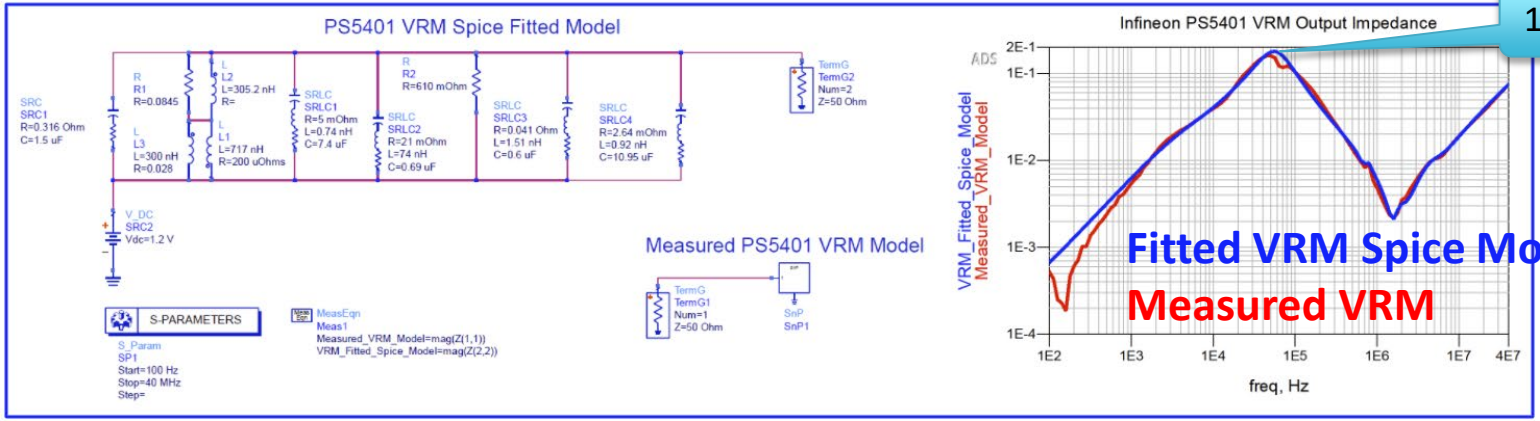


Simulation Model Setup

VCK190 VRM CHARACTERIZATION

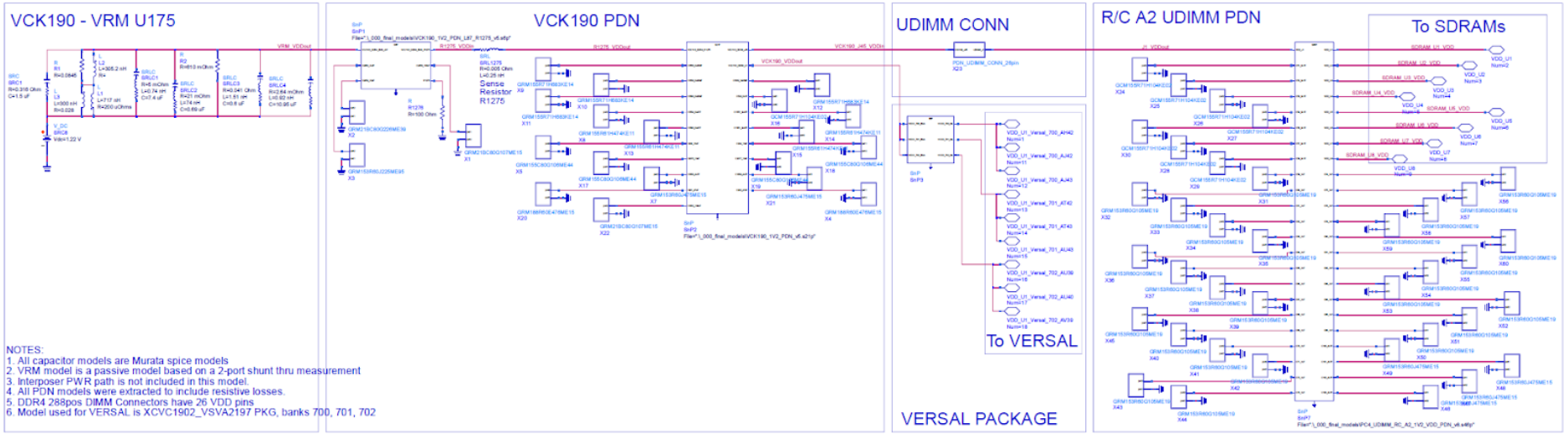


- Omicron Lab Bode 100
- Picotest P2102A-1X 2-port Probe
- Picotest J2102B Common Mode Transformer
- Picotest PDN Cable – BNC-BNC 0.25m
- DUT – Infineon PS5401 EVAL Kit



Simulation Model Setup

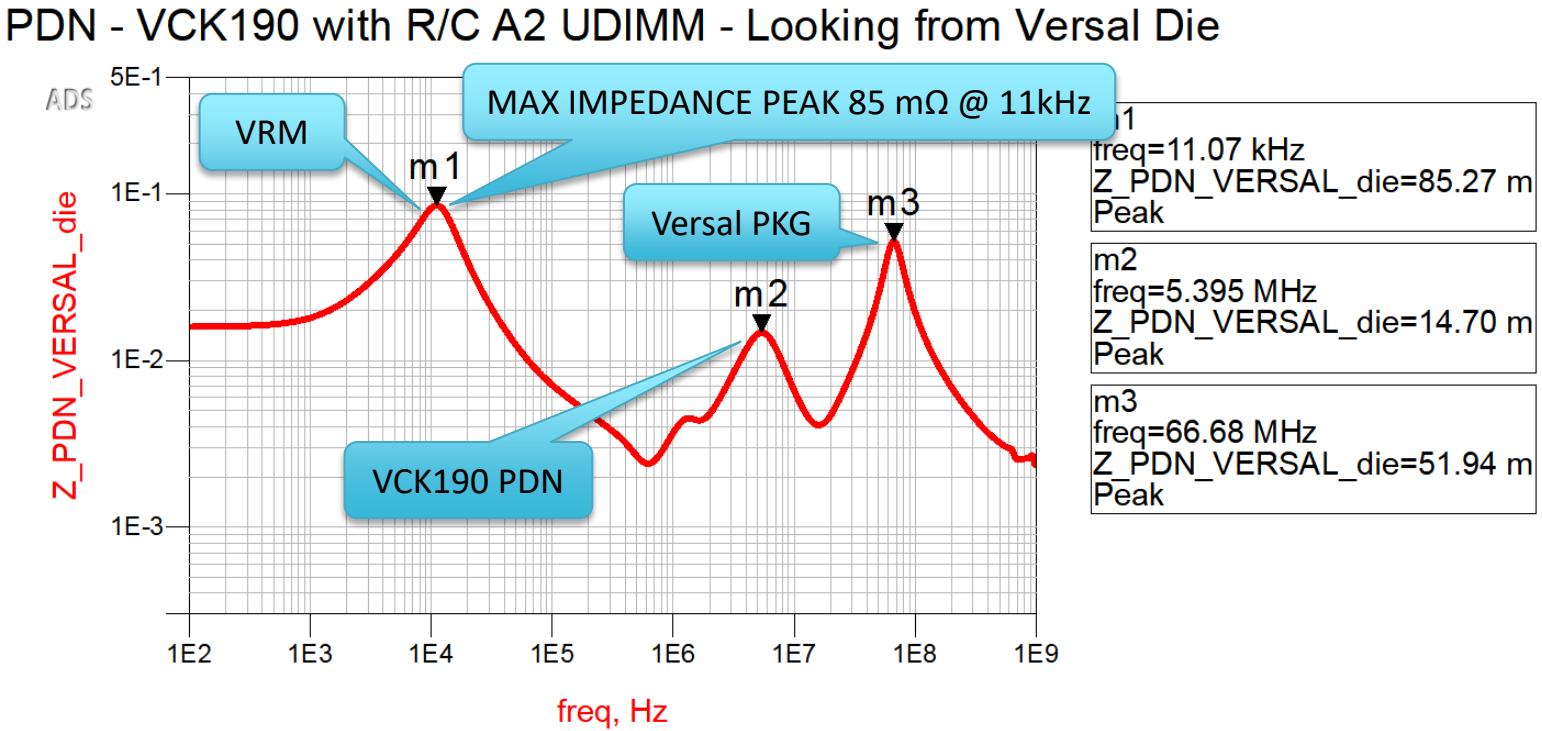
VRM + VCK190 PDN + R/C A2 UDIMM PDN



- All capacitor models are Murata spice models
- Versal VCCO PKG Model included for banks 700, 701, 702 – used for DDR4
- UDIMM Connector model includes 26 VDD pins to ensure accurate spreading inductance
- UDIMM connector model is assumed to include GND losses

Simulation Model Setup

PDN LOOKING FROM VERSAL DIE



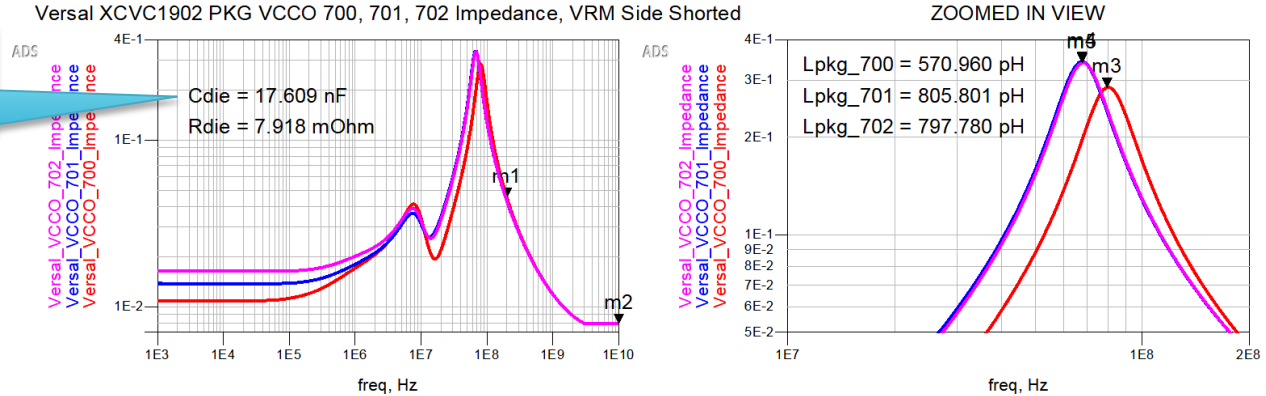
Simulation Model Setup

VERSAL DIE AND PKG – VCCO BANK 700, 701, 702 ANALYSIS

- In Versal IBIS model, capacitance per power pin (AJ42, AT43, AV39) are all about 50 pF, which is unusually high for the C_pkg

During DDR4 write cycle there is **~440 pF/DQ/DM/DQS** available

$$C_{die} = \frac{1}{2\pi f X_C}$$



From Micron IBIS/HSPICE Model Quality Report: Z11B

VDDQ/VSSQ Decoupling Capacitance (Approximate value at 10MHz) – Full Die: 6.7nF

Included in HSPICE DQ/DQS/DM models? Yes Amount per DQ/DQS/DM model: 304.4pF

As a comparison Micron SDRAM MPN: MT40A1G8SA provides **304.4 pF/DQ/DM/DQS**

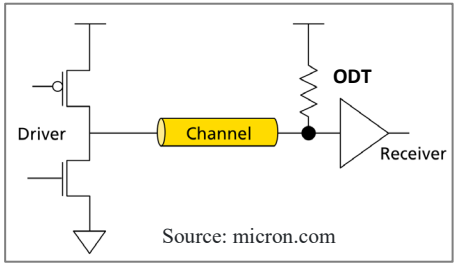
Ensures a reasonable amount of on-die decoupling has been included in Memory CTL to support SSO

Background on ODT Levels

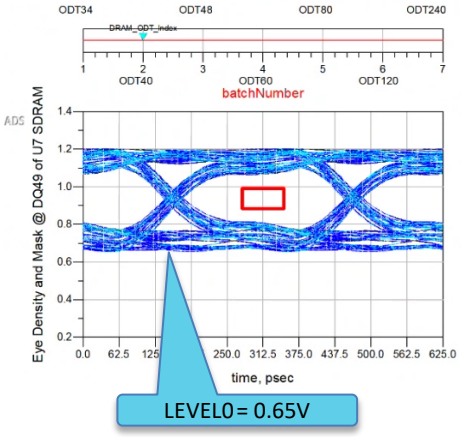
HOW ODT WORKS WITH DDR4

- On-Die Termination (ODT) for reducing reflections from discontinuities
- Source (driver) + Load → voltage divider network with pseudo-open drain

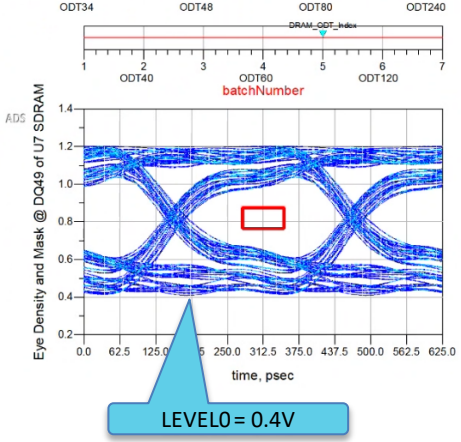
POD I/O Buffer



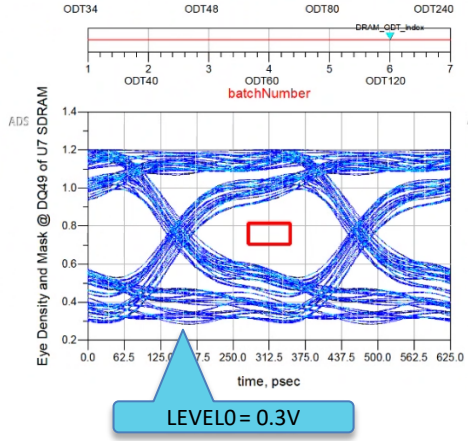
ODT = 40 ohms



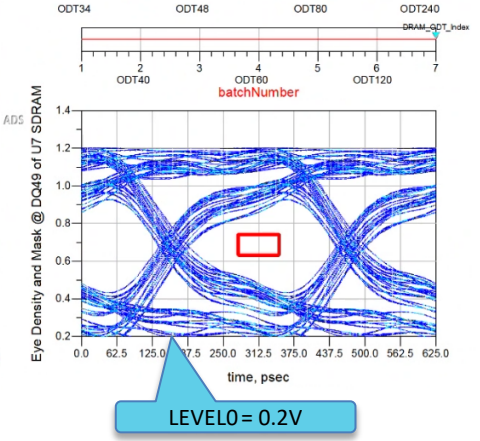
ODT = 80 ohms



ODT = 120 ohms



ODT = 240 ohms

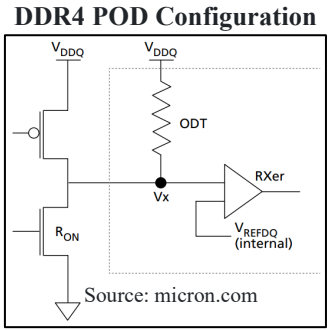


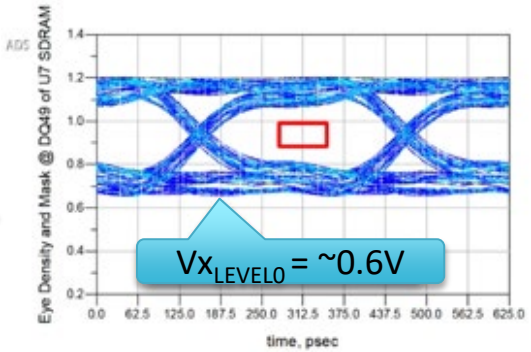
Background on ODT Levels

XILINX VERSAL REPORTED ODT VALUE DURING MEASUREMENT

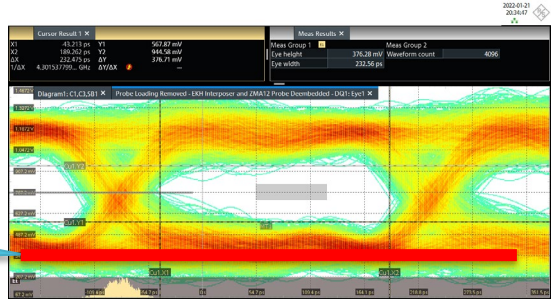
- During measurement Versal register settings reported ODT = 40Ω

VDDQ = 1.2V
Versal DRV = R_{ON} = 40Ω
ODT = 40Ω
Vx_{LEVEL0} = 0.6V





$$Vx_{LEVEL0} = VDDQ \cdot \frac{R_{ON}}{R_{ON} + ODT}$$



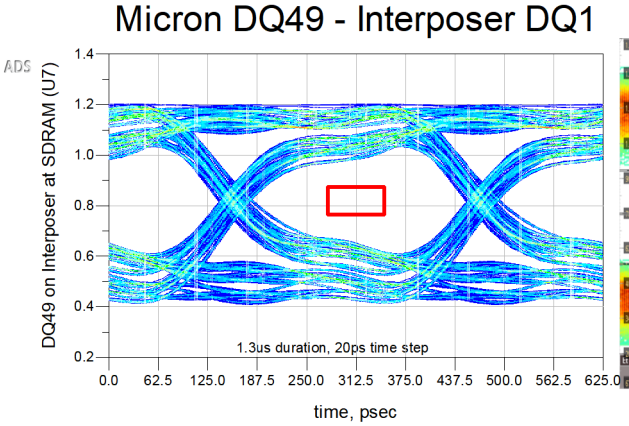
Measurement with Xilinx Versal during DDR4 write shows Vx_{LEVEL0} = ~400 mV

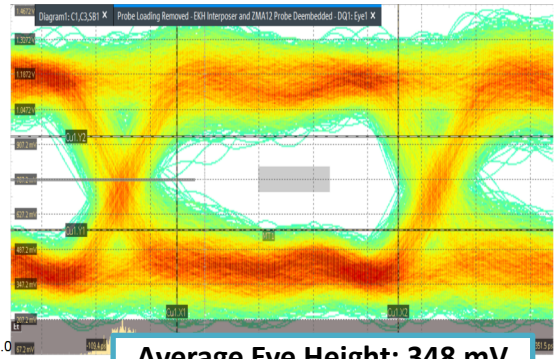
For simulation correlation to measurement a minimum ODT setting of 80Ω is required

Simulation Model Results

SI ONLY – MEM CTL SP DISTRIBUTED PKG MODEL

- Results shown with optimized eye using ODT = 80Ω
- Versal distributed SP model included
- SDRAM IBIS model v2.4
  - DRAM PKG model not included





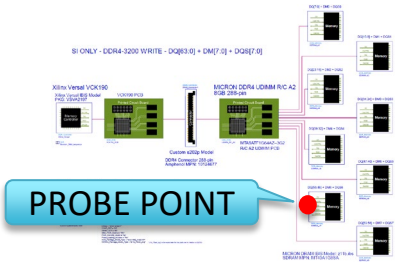
Average Eye Height: 348 mV

Average Eye Width: 228 ps

Measurement	...emory_Probe.EyeWidth
EyeWidth	256.2 p

Measurement	...mory_Probe.EyeHeight
EyeHeight	301.0 m

Simulation Summary:
Bit Sequence = 64bit random
CONT_ODT = 40 Ohm
DRAM_ODT = 80 Ohm
Controller pkg model = S-Para
DRAM pkg model = no
PWR Aware Sim = No
Ideal PWR Supply = Yes

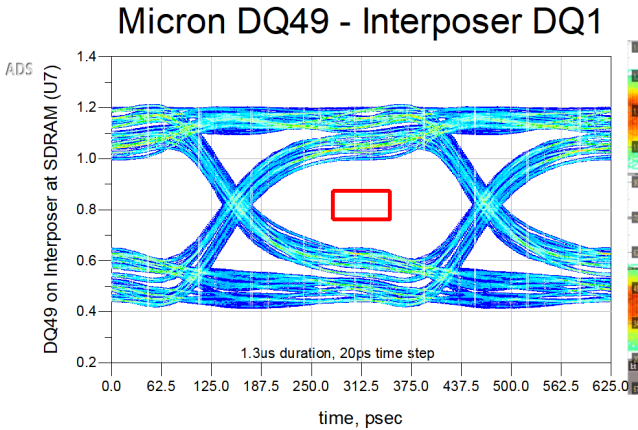


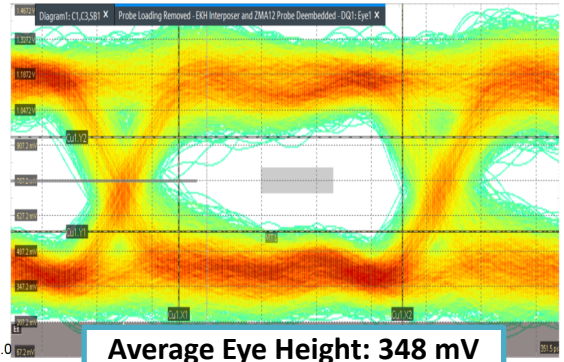
Result shown is with Versal S-parameter Distributed PKG Model

Simulation Model Results

SI ONLY - MEM CTL SPARSE MATRIX PKG MODEL & NO DRAM PKG MODEL, DRAM ibis v2.4

- Results are shown with optimized eye using ODT = 80Ω
- Versal sparse matrix PKG model included
- SDRAM IBIS model v2.4
  - DRAM PKG model not included





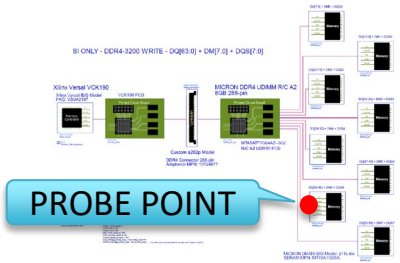
Average Eye Height: 348 mV

Average Eye Width: 228 ps

Measurement	...emory_Probe.EyeWidth
EyeWidth	265.6 p

Measurement	...mory_Probe.EyeHeight
EyeHeight	339.0 m

Simulation Summary:
Bit Sequence = 64bit random
CONT_ODT = 40 Ohm
DRAM_ODT = 80 Ohm
Controller pkg model = xcvc1902_vsva2197
DRAM pkg model = no
PWR Aware Sim = No
Ideal PWR Supply = Yes



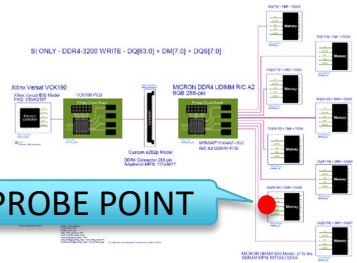
13% (38 mV) increase in Eye Height by using Versal Sparse Matrix PKG Model

Simulation Model Results

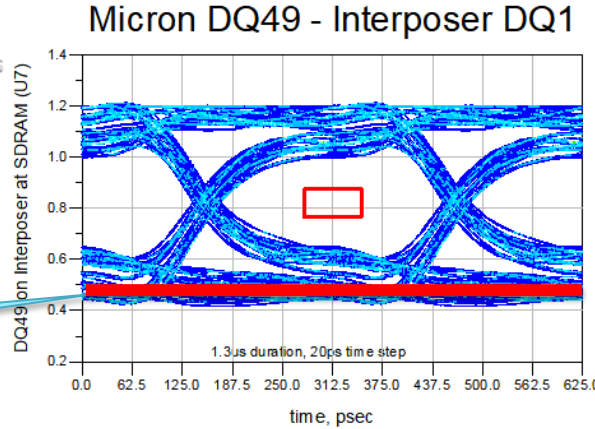
SI ONLY - MEM CTL SPARSE MATRIX PKG MODEL & NO DRAM PKG MODEL, DRAM ibis v2.8.2

- Results are shown with optimized eye using ODT = 80Ω
- Versal sparse matrix PKG model included
- SDRAM IBIS model v2.8.2
  - DRAM PKG model not included

Level0 point is lower in measurement vs. simulation

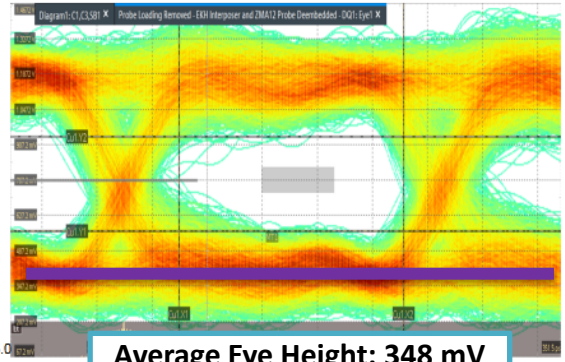


PROBE POINT



Measurement	...emory_Probe.EyeWidth
EyeWidth	265.6 p

Measurement	...mory_Probe.EyeHeight
EyeHeight	341.0 m



Average Eye Height: 348 mV

Average Eye Width: 228 ps

Simulation Summary:
Bit Sequence = 64bit random
CONT_ODT = 40 Ohm
DRAM_ODT = 80 Ohm
Controller pkg model = xcvc1902_vsva2197
DRAM pkg model = no
PWR Aware Sim = No
Ideal PWR Supply = Yes

0.6% (2 mV) increase in Eye Height when using newer DRAM ibis model v2.8.2

Simulation Model Results

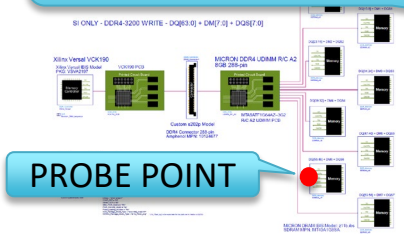
SI ONLY MEM CTL SPARSE MATRIX PKG MODEL, NO DRAM PKG MODEL, DRAM ibis v2.8.2, DRAM SLOW CORNER

DRAM IBIS CORNER - ODT SETTING*		
TYP	SLOW	FAST
82.3 Ω	92.8 Ω	71.8 Ω

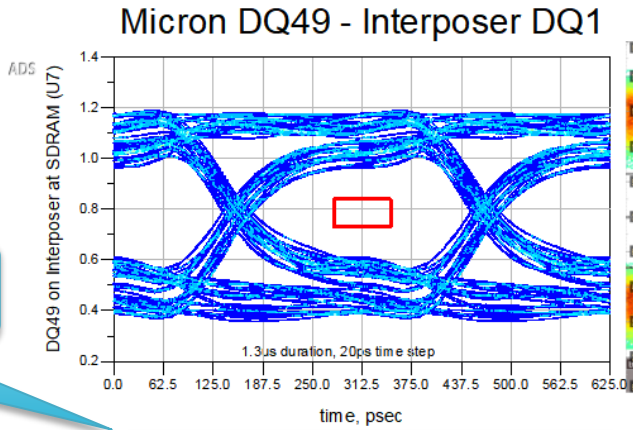
*Provided by Micron

Eye Width is 15.7% (36 ps) larger than Average measurement

1.8% (6 mV) increase in Eye Height with SLOW DRAM IBIS CORNER

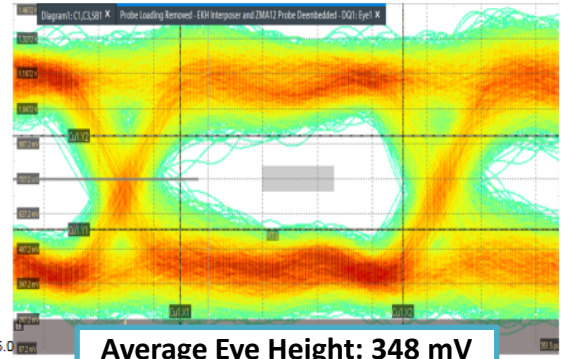


PROBE POINT



Measurement	...emory_Probe.EyeWidth
EyeWidth	264.1 p

Measurement	...mory_Probe.EyeHeight
EyeHeight	347.0 m



Average Eye Height: 348 mV

Average Eye Width: 228 ps

Simulation Summary:
Bit Sequence = 64bit random
CONT_ODT = 40 Ohm
DRAM_ODT = 80 Ohm
Controller pkg model = xcvc1902_vsva2197
DRAM pkg model = z11b 2.8.2 no package slowcorner
PWR Aware Sim = No
Ideal PWR Supply = Yes

Eye Height is 0.3% (1 mV) lower than Average measurement with no injected jitter

Simulation Model Results with Injected Jitter

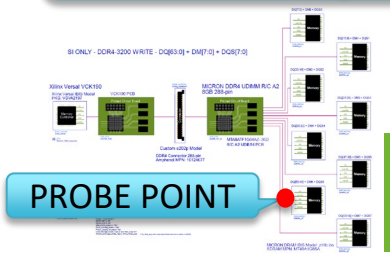
BEST RESULT

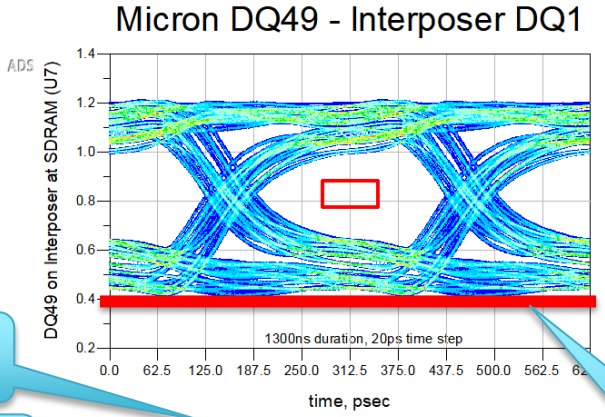
SI ONLY MEM CTL SPARSE MATRIX PKG MODEL, NO DRAM PKG MODEL, DRAM ibis v2.8.2, DRAM SLOW CORNER

- Results shown with optimized eye using ODT = 80Ω
- Versal sparse matrix PKG model included
- SDRAM IBIS model v2.8.2
  - DRAM PKG model not included
- MEM CTL RJ = 0.36 ps, PJ = 23.4 ps @ 200MHz

Eye Width is 2.65% (6 ps) larger than Average measurement

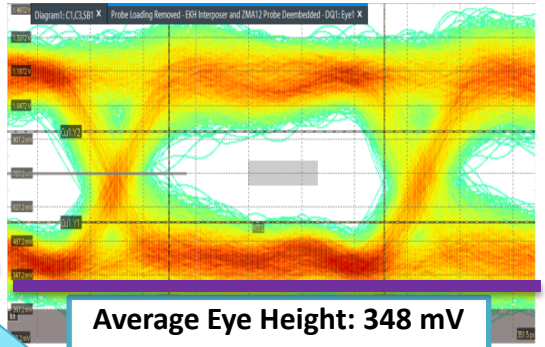
Eye Height is 9.4% (33 mV) lower than Average measurement





Measurement	...emory_Probe.EyeWidth
EyeWidth	234.4 p

Measurement	...mory_Probe.EyeHeight
EyeHeight	316.0 m



Average Eye Height: 348 mV

Average Eye Width: 228 ps

Level0 is higher in simulation

Simulation Summary:
Bit Sequence = 64bit random
Controller Tx Rj in ps = 0.356
ps = 23.438
quency in MHz = 200.000
Ohm
Ohm
del = xcvc1902_vsva2197
= z11b 2.8.2 no package
PWR Aware Sim = No
Ideal PWR Supply = Yes

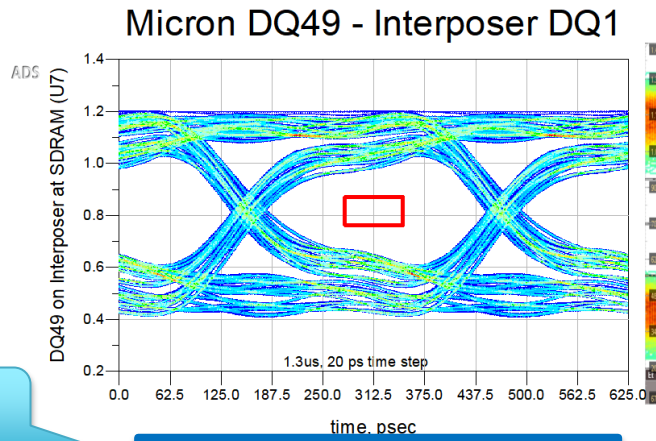
Eye Width correlates to Measurement! The SDRAM ODT model prevented us from matching Eye Height measurement with injected Jitter.

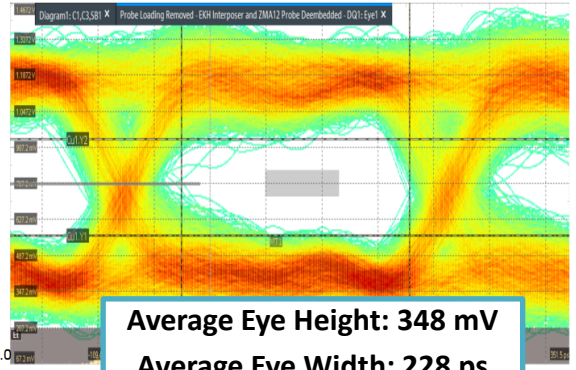
Simulation Model Results

POWER AWARE SI RESULTS

- Results are shown with optimized eye using ODT = 80Ω
- Versal distributed SP model included
- SDRAM IBIS model v2.8.2
  - DRAM PKG model not included

Measurement model includes SSN from SSO





Average Eye Height: 348 mV

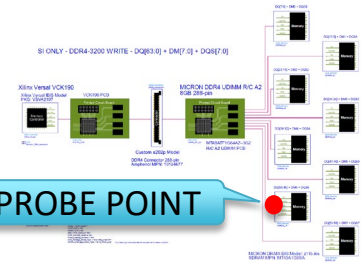
Average Eye Width: 228 ps

Eye Width is 12% (28 ps) larger than Average measurement

Measurement	...emory_Probe.EyeWidth
EyeWidth	256.2 p

Measurement	...mory_Probe.EyeHeight
EyeHeight	296.0 m

Simulation Summary:
Bit Sequence = 64bit random
Controller Tx Rj in ps = @TxJitter_Rj_ps
Controller Tx Pj in ps = @TxJitter_Pj_ps
Controller Tx Pj frequency in MHz = @TxJitter_Pj_freq
CONT_ODT = 40 Ohm
DRAM_ODT = 80 Ohm
Controller pkg model = S-Para
DRAM pkg model = no
PWR Aware Sim = Yes
Ideal PWR Supply = No



PROBE POINT

15% (52 mV) decrease in Eye Height vs. Average Measurement

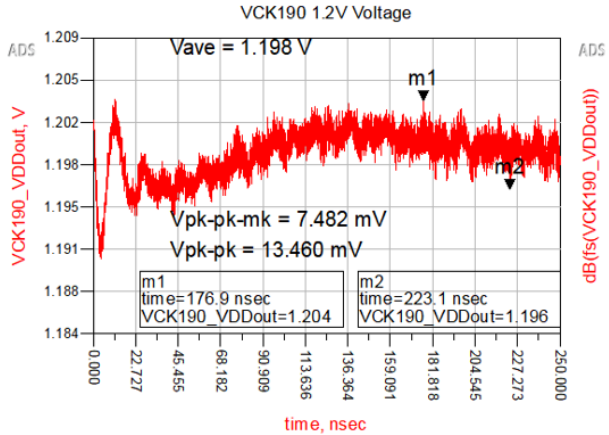
6.3% (20 mV) decrease in Eye Height vs. SI only result Jitter

Simulation Model Results

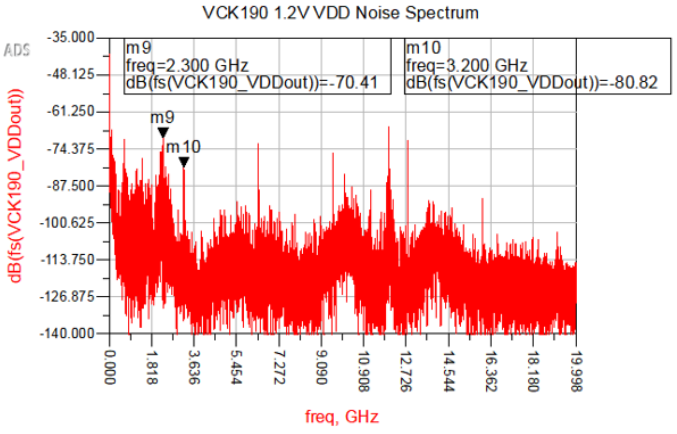
POWER AWARE SI RESULTS

- Power Aware SI Model includes 64 bits switching in PRBS pattern

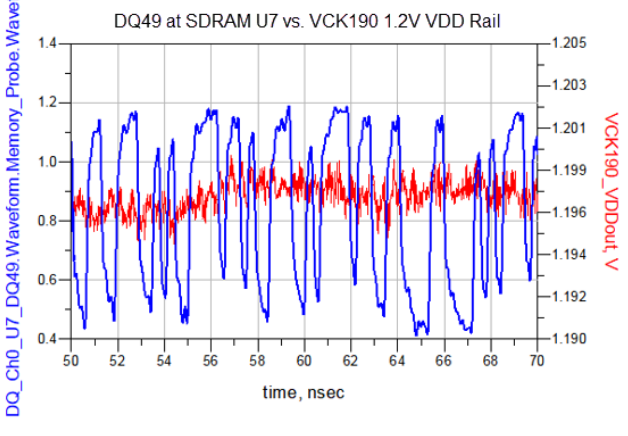
Very little ripple voltage seen where is Vpk-pk (steady state) = 7.5 mV



Almost no noise seen at 3.2 GHz, the noise is -80.8 dB



Very little SSN superimposed on DQ49 waveform



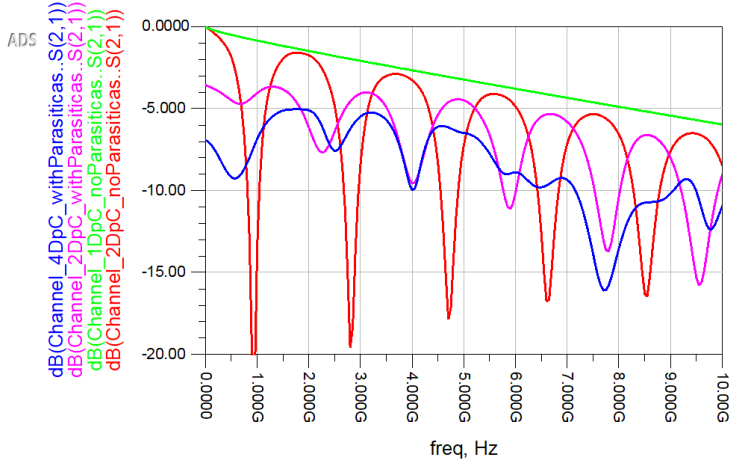
MEMORY CONTROLLER MODEL LIKELY UNDERREPRESENTING NOISE PROFILE

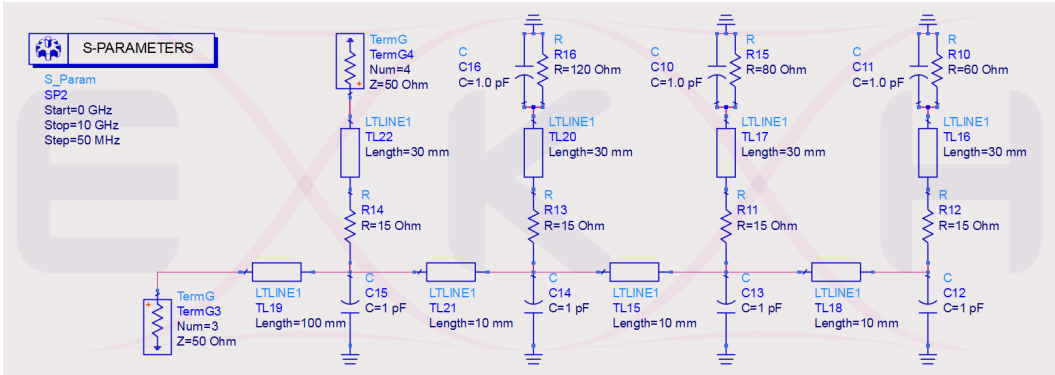
Equalizer: Impact of Topology

CHANNEL RESPONSE FOR MEMORY INTERFACES

- Channel Responses for a higher number of DIMMs per Channel
  - R-DIMM does have a series Resistor on DIMM
  - Stub is too long to compensate with 4-tap DFE (blue S21 plot)

→ **It will be difficult (near impossible) to implement 4 DIMM systems at high speed!**





4 DIMM slots: 10mm DIMM2DIMM + 30mm DIMM stub

Reflections in a DDR5 2 DIMM per Channel

CHANNEL RESPONSE FOR MEMORY INTERFACES

- Reflections due to 2 DpC configuration

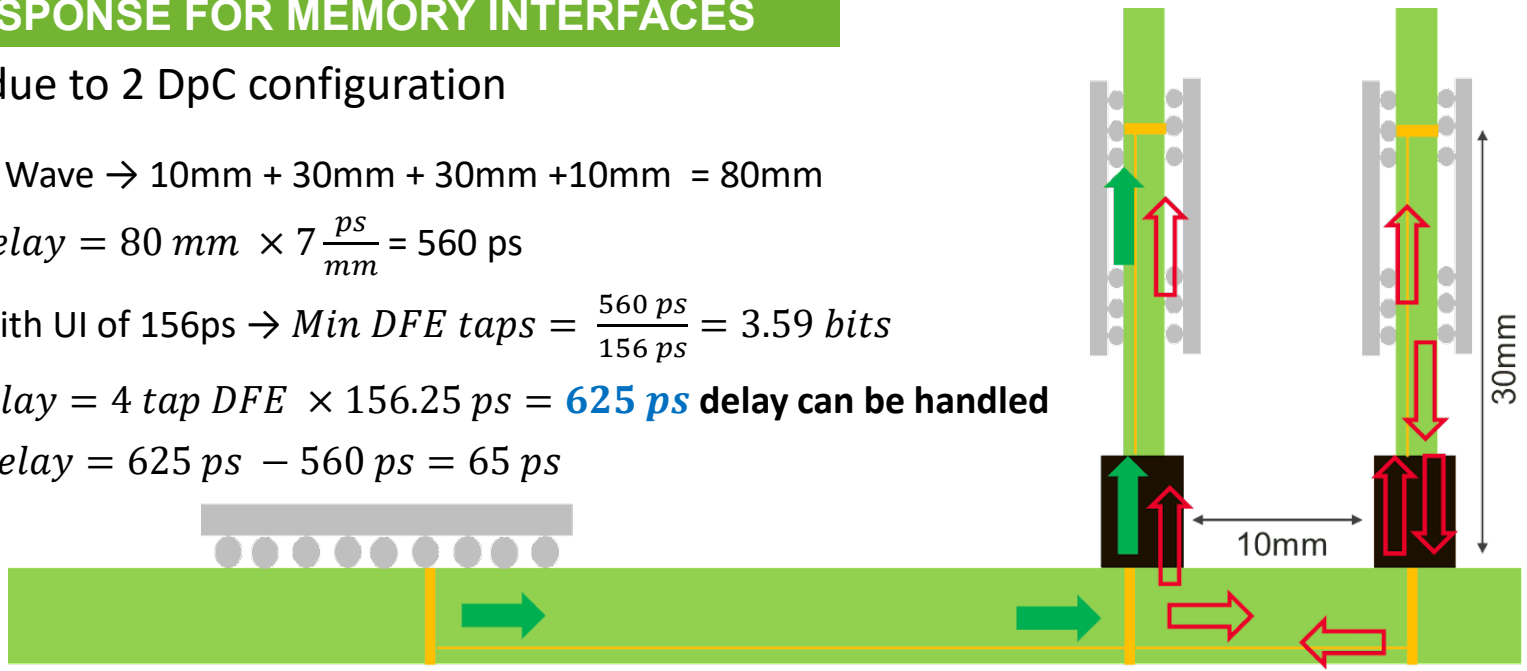
Length for reflected Wave → 10mm + 30mm + 30mm +10mm = 80mm

$Reflected\ wave\ delay = 80\ mm \times 7\frac{ps}{mm}$ = 560 ps

6.4Gbps interface with UI of 156ps → $Min\ DFE\ taps = \frac{560\ ps}{156\ ps} = 3.59\ bits$

$Maximum\ DFE\ Delay = 4\ tap\ DFE \times 156.25\ ps = \mathbf{625\ ps}$ **delay can be handled**

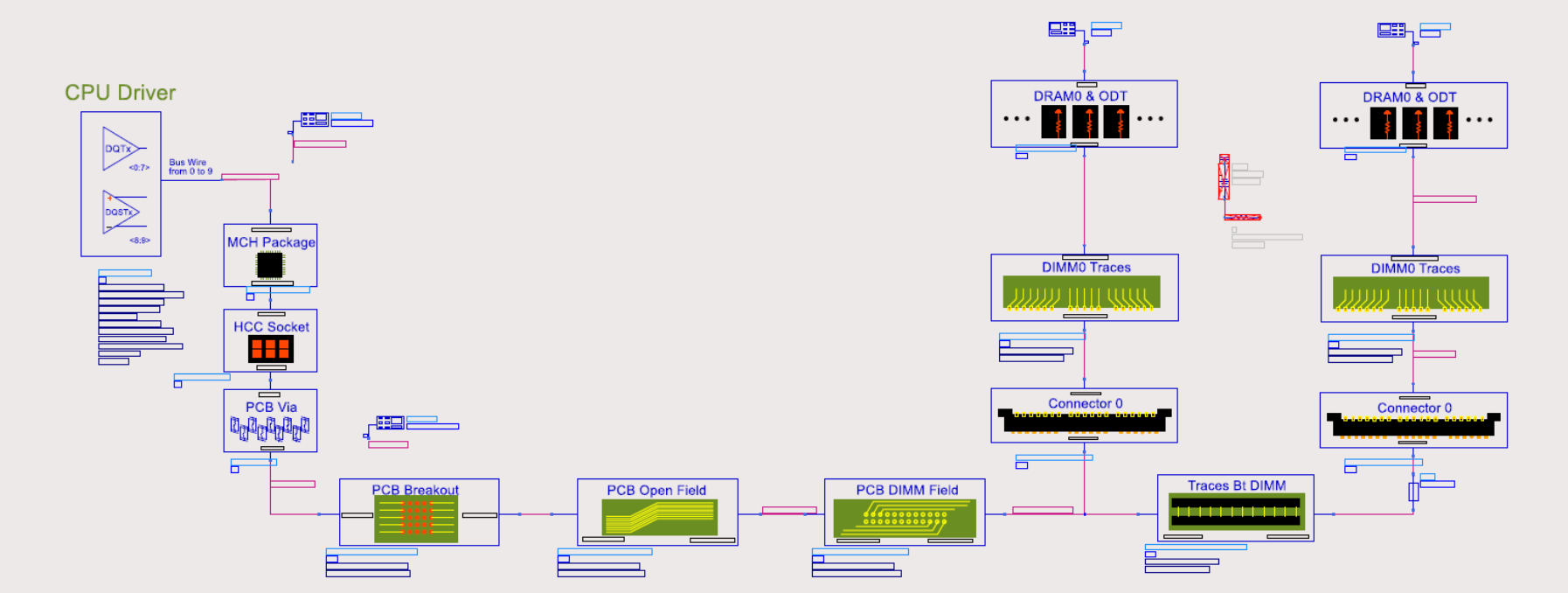
$Remaining\ DFE\ Delay = 625\ ps - 560\ ps = 65\ ps$



Large DRAM subsystems will never get a P2P environment and will therefore always have to deal with reflections!

The Future of DDR Simulation

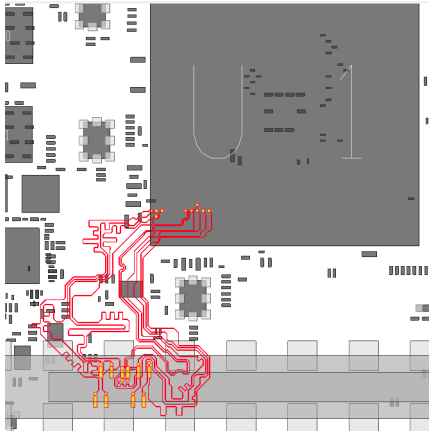
THE DDR5 GOLDEN CHANNEL

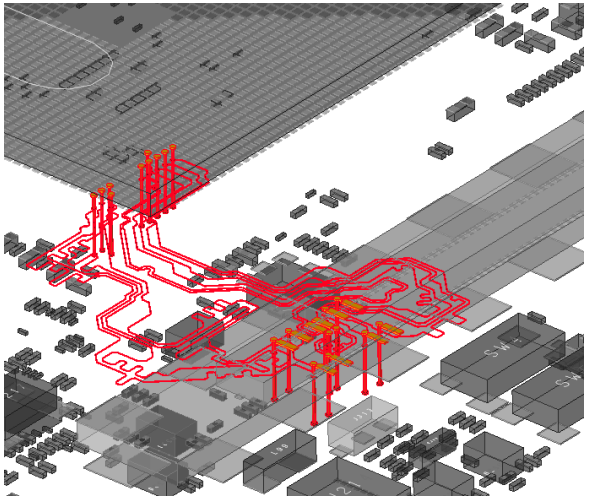


Source: Evolution of High-Speed Server and Computing Interfaces - https://keysightevent.com/kw2019/handout/b5

Next Steps

- Update Versal IBIS model with ISSO PU and PD curves to achieve correlated power-aware SI model to measurement
- Explore DDR5 paths to do power-aware SI simulation using AMI models
- IC vendors and EDA software tools need a suitable solution that allows power-aware SI and AMI modeling with equalization
- Explore effects of SSN with State-Space Average VRM model
- Explore effects of this noise generated through the return path at the UDIMM connector, Versal package, VCK190 PCB, and UDIMM PCB.
- Drive industry to implement a Golden reference channel + DFE (DDR5)





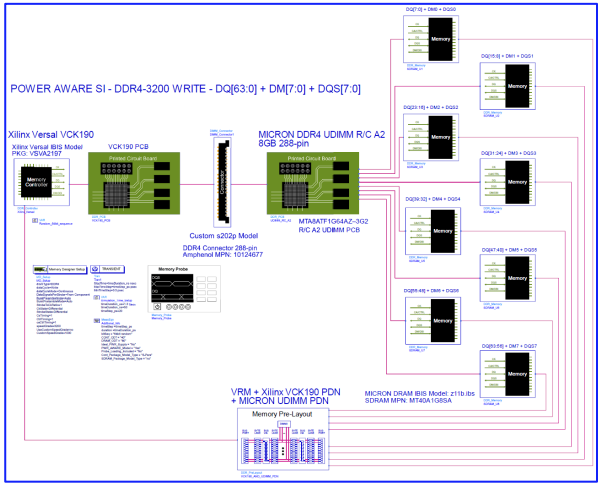
Summary

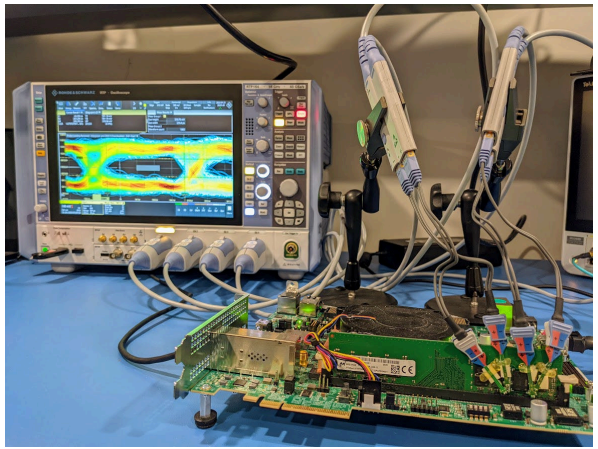
Validated DDR4-3200 design

- Correlated SI only simulation with jitter to measurement
- Power-aware SI models
- Interposer-based measurement setup

Key learnings

- Must include de-embedding & probe loading effects
- Vendor IBIS model importance
- Vendor package models matter!
- Chip vendors need to work harder to provide more accurate models





Thank you!

QUESTIONS?

Acknowledgements

- Picotest: Steven Sandler
- Rohde & Schwarz: Jason Ruffing, Mike Schnecker
- Keysight: Stephen Slater, Nacim Bravo
- Xilinx: Taylor Maddix, Ryan Arp, Fran Olveri, Jon Schimek, Sam Hendrix, John Rinck
- Micron: Justin Butterfield

References

1. Eye Diagram Measurements in Advanced Design System - http://literature.cdn.keysight.com/litweb/pdf/5989-9453EN.pdf
2. "Deembedding of DDR Interposer" by Guido Schulze, April 2020 Rohde & Schwarz
3. Evolution of High-Speed Server and Computing Interfaces - https://keysightevent.com/kw2019/handout/b5
4. Rohde & Schwarz - RTP164, 16GHz Bandwidth Oscilloscope - https://www.rohde-schwarz.com/us/product/rtp-productstartpage_63493-469056.html
5. Rohde & Schwarz - Probe Amplifier Module 16 GHz Bandwidth - RT-ZM160 - https://www.rohde-schwarz.com/us/product/rt-zm-productstartpage_63493-326208.html
6. Rohde & Schwarz - Flex Connect solder-in Probe Tips 16GHz Bandwidth - RT-ZMA14 - https://www.rohde-schwarz.com/us/product/rt-zm-productstartpage_63493-326208.html
7. Xilinx VCK190 - https://www.xilinx.com/products/boards-and-kits/vck190.html
8. Picotest P2102A - 2 Port PDN Transmission Line Probe - https://www.picotest.com/products_PDN_Probe.html
9. Picotest J2102B-N – Common Mode Transformer - https://www.picotest.com/products_J2102B.html
10. Picotest PDN Cable® - https://www.picotest.com/pdn-cable.html
11. Keysight N2787A 3D Probe Positioner - https://www.keysight.com/us/en/product/N2787A/3d-probe-positioner.html
12. Infineon EVAL_PS5401-INT - https://www.infineon.com/cms/en/product/evaluation-boards/eval_ps5401-int/
13. Amphenol DDR4 DIMM Connector, https://www.amphenol-icc.com/ddr4-101246770221r11lf.html
14. Modeling On-Die Power Supply Decoupling - https://ibis.org/summits/feb12/wolff.pdf