DesignCon 2020

Signal Integrity Characterization of Via Stubs on High Speed DDR4 Channels

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Abstract

DDR4 requires tight specifications for high-speed operation, and its channel modeling requires high accuracy, since real world designs could operate close to the specification limits. The JEDEC standard defines the maximum speed for DDR4 as 3200 megatransfers per second (MT/s), although the first DDR4 DIMMs just became available at those speeds. As printed circuit boards (PCBs) continue to become more complex with higher densities, this is driving an increase in the number of layers in a PCB stack-up used to ensure all signals in the design are routed effectively. Thick PCB vias with long stubs create unwanted resonances in the channel these resonances occur near the Nyquist frequency of the bit rate, and they can devastate the eye opening at the receiver. The question is, how big are the parasitic capacitance from these vias and will it have an adverse effect on the switching edge? The scope of this research aims to understand the impact of via stubs to the impedance of the signal lines on DDR4 memory. Another goal of this research effort is to present ideas intended to see how far a complex design can be pushed, using DDR4 with via stubs. The intent of this effort is to prove, with SI simulations, at what via length DDR4 link failures will occur, and correlate those results (with link failures) to the resonant frequency of the via created by the stub.

Author Biography

Benjamin Dannan is currently an Engineering Manager and Principal Electrical Engineer at Diversey, Inc., in charge of the Robotics Electrical Engineering team. At Diversey, he develops fully autonomous cleaning robots, to include embedded systems and sensors. He has over 10 years of design experience in high-volume, high-reliability, engineering environments, to include robotics, embedded systems, high speed PCBA design, mechatronics design, and designing for EMC requirements. He is a specialist in signal and power integrity concepts, high-speed circuit and multi-layered PCB design, vision systems, robotics, as well as has multiple years of experience with EMI/EMC product mitigation and certifications. He graduated from Purdue University with a BSEE in May 2009, and from USAF Undergraduate Combat Systems Officer training with an Aeronautical rating, in September 2012. Benjamin is also a trained Electronic Warfare Officer in the USAF with deployments on the EC-130J Commando Solo in Afghanistan and Iraq totaling 47 combat missions. In addition, Benjamin holds three patents in his name. He recently completed his Masters of Engineering in Electrical Engineering from the Pennsylvania State University, and has started a new military career in cybersecurity with the 175th Cyber Operations Group in the Maryland Air National Guard.

I. INTRODUCTION AND BACKGROUND

The world we live in today has become a completely data-driven society. For example, according to YouTube usage statistics, 400 hours of video are uploaded to YouTube every minute. Additionally, over one billion hours of video are watched on YouTube every day [1]. According to Business insider, 350 million photos are uploaded to Facebook every day, with 14.58 million photo uploads per hour, 243,000 photo uploads per minute, and 4,000 uploads per second [2]. With all of this data, there needs to be a means to store and process it quickly, thus making memory and fast-storage solutions central to the basic functions of computing. The top speeds of DDR DRAM devices bring forth a legion of signal integrity and power integrity concerns that if the designer doesn't approach systematically, will leave margin, performance and reliability on the table. In summary, the memory channel has become the bottleneck of computer systems, whether it is data center, server, or workstation. This will become even further evident when DDR5 is available which is anticipated to have data rates approaching 6400 MT/s. As DDR data transmission rates continue to increase, the signal integrity of the DDR channel has become one of the most critical concerns.

II. BACKGROUND OF VIA STUB IMPACT ON SIGNAL INTEGRITY

There are various types of stubs that can be part of the interconnects and degrade the electrical performance. For example, the stub of a via in printed circuit boards (PCBs) can dramatically deteriorate the signal integrity when a digital system operates at multi-gigahertz data rates. In addition, according to Huang, et al. [19], “the equivalent stub of an unpopulated or empty DIMM connector can also have significant negative impacts on a computer system—for instance, the DDR4 memory interface

Vias are widely used as the vertical interconnect in PCBs. There are various types, such as plated through hole (PTH), buried, and micro (also known as blind) vias. PTH vias are most commonly used in the PCB industry because they are easy to fabricate and are low cost. Stubs are the portion of PTH vias that are not on the intended signaling path and create a discontinuity which can degrade the high-speed signal quality. It is a known fact that the signal will degrade further if the stub length is longer in a thicker PCB, or if the data rate increases. There are various industry practices to avoid via stub issues, such as routing high-speed signals in specific layers, slowing down the channel speeds, making design tradeoffs on other portions of the channel, using high-density interconnect (HDI) manufacturing techniques like blind or buried vias, or use back-drilling to remove the via stub [19]. HDI designs are known to be very expensive, even more so in the enterprise market that uses multi-socket platforms implementing larger PCBs. HDI is also limited by a finite number of lamination cycles that a PCB can withstand, and, thus, it is impossible to fully eliminate all via stubs on a multi-layer PCB.

Back-drilling is a widely used technology since it is an effective way of minimizing stub effects. However, backdrilling becomes challenging for denser vias such as the via field underneath a central processing unit (CPU) and chipset package, or the stub length becomes longer on a thick board. Back-drilling cannot completely remove the stubs because of the drill depth tolerance and the manufacture requirements on some vias such as the ones for press-fit connectors.

Via stubs can cause various issues in the design. They resonate at a quarter wavelength and dramatically degrade the insertion loss. They are often capacitive in nature and can affect the return loss and crosstalk dramatically [14]. The figures below demonstrate the effect of the via stubs on return loss, crosstalk and insertion loss” [14].

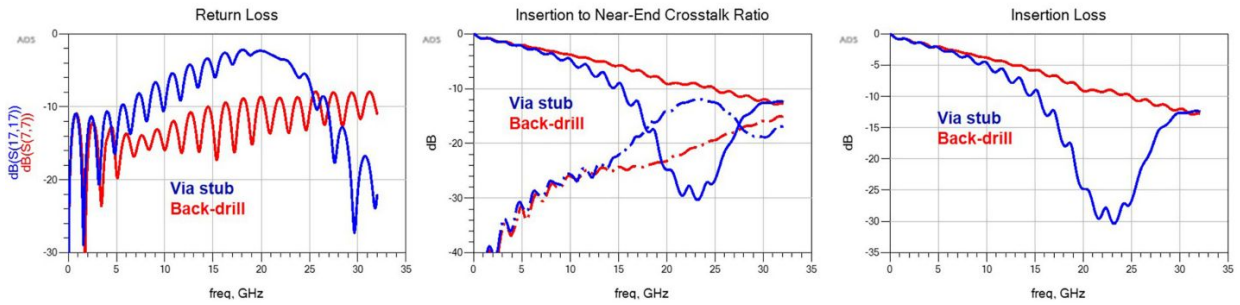

Figure 1 - Via Stubs on Return loss, Crosstalk and Insertion Loss [14]

By referring to figure 2, stub resonances occur when a portion of the signal traversing the active region of a via diverts down into the stub section, reflects off the open-circuited end, and returns later to recombine with the main signal. At a high frequency—the quarter-wave resonant frequency—the round-trip delay from the active region of the via to the end of the stub and back equals a half-cycle. If this scenario occurs, the main wave and the reflected wave appear 180 degrees out of phase, producing destructive signal cancellation. The longer the stub, the lower the resonant frequency is [11].

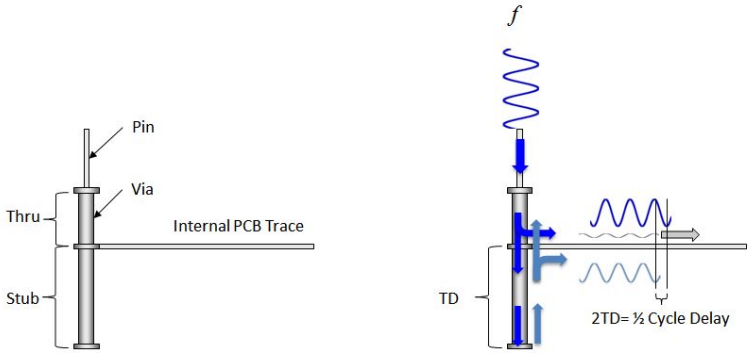

Fig. 2 - Illustration of a ¼ -wave resonance of a stub. [12]

Designers can shorten their PCBs via stubs by back-drilling the vias as close as possible to the active internal-signal layer. This complex and costly process requires that one specifies the necessary back-drilling depth for each via using special design features in the artwork. Occasionally, glitches in the back-drilling process leave some vias with longer-than-expected stubs. It is only after the board has been fully assembled and tested in the system that such a problem can show up in the form of a higher bit error rate [11]. Even worse, during back-drilling, the drill bit could break causing damage to the PCB fab, thus resulting in a loss of the entire PCB.

III. STATEMENT OF THE PROBLEM

As PCBs continue to become more complex with higher densities, this drives an increase in the number of layers in a PCB stack-up used to ensure all signals in the design are routed effectively. Thick PCB vias with long stubs create unwanted resonances in the channel insertion loss, whereas vias with short or no stubs do not. If these resonances occur near the Nyquist frequency of the bit rate, they will devastate the eye opening at the receiver [11].

Typical routing for DDR4 SDRAM components require at least two internal signal layers, two surface signal layers, and four other layers (2 VDD and 2 VSS) as solid reference planes. Data server mainboards or PCBs, continue to be become significantly more dense in the space constraints thus requiring additional copper layers to be added to

accommodate the signal layers needed to route the DDR signals. In a networking product design, it is common that DDR signal traces be routed on the top half of the PCB to allow signal layers for routing the 10 Gbps ethernet signals, since these are three times faster than DDR signals. A PCB of this design could be 22 layers and approximately 100-mil thick. As a result, this creates the opportunity for via stubs to greatly impact the signal integrity of these DDR signals. To improve signal performance as data transfer rates increase and signal amplitude decreases, the clock and strobe signals (DQS) are differential, which cancels out common mode noise. The other signals, specifically data (DQ), address (ADD) and control (CTL) still operate in single-ended mode, which makes them more susceptible to noise, crosstalk and interference" [8]. The DQ signals operate at two times the data rate as ADD and CTL signals, which make them the most critical.

As a rule of thumb, we usually strive to have an interconnect bandwidth (BW) to be five times the Nyquist frequency (or clock frequency) of the bit-rate. This is important in order to estimate the rise time of the signal. This follows many oscilloscope manufacturers' specifications for rise time bandwidth product to be equal to 0.35. Five times the Nyquist represents the 5th harmonic sinusoidal component of a Fourier series making up an ideal square wave. An interconnect BW up to the 5th harmonic, preserves the integrity of rise time down to 7% of the period of the fundamental frequency [12]. Hence, it is a reasonable generalization that the rise time is 7% of the clock period. This is represented by EQ (1).

$$RT = \frac{0.35}{BW} = \frac{0.35}{5f} = 0.07T \quad (1)$$

Where:
RT : 10-90 rise time, in nsec
BW : bandwidth (BW) product to the 5th harmonic of the fundamental frequency
f : Nyquist or clock frequency
T : Nyquist frequency period, equivalent to 1/f

Per JEDEC standard 79-4B [5], the slew rate limits for single ended DDR4-3200 outputs (e.g. DQ) can range from 4 V/ns to 9 V/ns. For DDR4-3200 differential signals, DQS can have an output slew rate that varies from 4 V/ns to 18 V/ns. It should be clarified that the actual slew rate will be determined by the silicon manufacturer and is typically contained in the respective IC manufacturer's IBIS model. JEDEC DDR4 standard 79-4B [5] specifies that a 3.2 GHz data signal, with a Nyquist frequency (f) of 1.6 GHz, needs a BW of 8 GHz to preserve any RT down to 7% of the Nyquist frequency period (T) of 625 ps. Therefore, the intent is to explore where the link failures in DDR4 channel occur, and if any via structures have stubs that resonate at or close to the clock frequency, which in this case is the Nyquist rate.

IV. PROPOSED SIMULATION MODEL, SIMULATION SETUP, PARAMETERS USED FOR SIMULATION

A single DDR4 Byte lane will be simulated using a Keysight ADS DDR bus simulator based on the test cases, and parameters defined later in this section. The DDR bus simulator allows for simulation that meets the DQ receiver compliance mask at 1x10-16 BER in the JEDEC DDR4 specification shown below. This is achieved by the DDR4 tool using a statistical simulation, which also accounts for crosstalk and for asymmetry between rising and falling transition times [4].

The DQ input receiver compliance mask defines the area that the input signal must not encroach in order for DRAM input receiver to be expected to successfully capture a valid input signal with BER of 1x10-16; any input signal

encroaching with the Rx Mask is subject to being invalid data [5]. This will be set for all BER contours during the presented analysis.

This effort will execute analysis based on the test cases defined below. Table 1 below defines the variables used for each test case. Sub-sections A to C define each test case that will be part of (i.e., simulated) in this experiment. Jitter will not be injected into any test cases since that is another exercise in experimentation in itself. Furthermore, no analysis will be done to explore receiver model de-emphasis and continuous-time linear equalization (CTLE).

Table 1 - Model Variables for each Test Case

Model Input	**Variable Details**	**Notes**
Signals	1/2 DDR4 byte lane	DQ[3:0], DQS_P0/DQS_N0
Total Channel Length	Static variable	Trace length from MEM CTR to DDR RCV, defined in section 4
Trace width	Static variable	As defined in section 4 to meet impedance requirements on respective routing layer
Distance between stubs	Static variable	As defined by each test case in section 4
Via structure	Static variable	As defined in section 4
Temperature	Static variable	Standard 25C temp will be used the simulation model
PCB Stack-up	12L, 14L, 16L, 18L, 20L, 22L, 24L, 26L, 28L	The stack-up determines the stub length. Emphasis of effort includes putting critical signals to be analyzed on layer 3 to maximize stub length
PCB Laminate	Isola FR408HR	All stack-ups are using FR408HR. See references [13] for datasheet link
RDIMM PCB stack-up	Static variable	Based off JEDEC R/C D1 PCB stack-up [6]. The margins demonstrated for each test case only apply specific dimm
DQ/DQS (Slew Rate) Rise Time	Static variable	All (slew rates) rise times used will be the maximum for both DQ/DQS as defined in JEDEC standard
Controller DRV Impedance (R_{on})	Static variable - 40 Ω	Unless stated otherwise
Series Resistor (R_s)	Dynamic variable	Each test case will optimize Rs to effectively tune the channel
DIMM socket	Static variable	Amphenol DDR4 SMT Connector: MPN:10124677 [7]
ODT Value	Dynamic variable	ODT Values: 34 Ω, 40 Ω, 48 Ω, 60 Ω, 120 Ω, 240 Ω
VDDQ	Static variable - 1.2V	Reference [5] for more details

IV.1. DEFINITION OF SIMULATION TEST CASES

IV.1.1. TEST CASE #1 - DDR4 DATA SIGNALS POINT-TO-POINT WITHOUT VIAS IN THE CHANNEL

The objective of test case #1 is to understand the simulation baseline at 3200 Mbps for the static total channel length without any discontinuities added in the channel from vias, connectors or other interconnect.

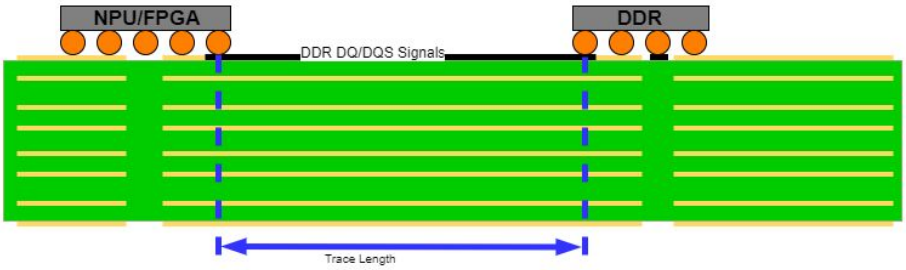

Figure 3 - Test Case #1 - 2D Model Depiction of DDR4 Data Signals Point-to-Point Without Vias in the Channel

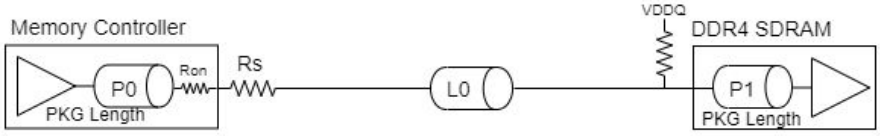

Figure 4 - Test Case #1 - DQ Channel Model of DDR4 Data Signals Point-to-Point Without Vias in the Channel

Table 2 - Test Case #1 - Impedance, Length, and Spacing Guidelines for DDR4 Signals

Test Case #1		
Parameter	**L0 (MB PCB)**	**Units**
Trace Type	Microstrip - L1	-
DQ single-ended impedance Z_0	50+/- 10%	Ω
DQS differential impedance Z_{DIFF}	100+/- 10%	Ω
DQ trace width (nominal)	5	mil
DQS differential trace width/spacing	5/15.0	mil
Total Channel Length = Trace length	0.937	inches
Spacing in byte lane signals (minimum)	15.0	mil
Maximum PCB via count	No vias in channel	-

IV.1.2. TEST CASE #2 - DDR4 DATA SIGNALS POINT-TO-POINT WITH VIAS IN THE CHANNEL

The objective of test case #2 is to provide a simulation model of the channel for a static total channel length, at 3200 Mbps, with only the via discontinuities included in the channel.

For all of the PCB stack-ups defined in the appendix section, all of the via structures are represented by figure 5. The via structure parameters are defined by table 3. The intent was to define a via structure that would allow close to a 10:1 aspect ratio from a 14L PCB stack-up to a 28L stack-up. Although this is not 100% feasible across the entire range of stack-ups with a 10 mil via drill diameter. The intent was to keep the drill diameter variable static to avoid introducing another variable permutation in this research effort. Further, the selection of the via structure parameters defined are to allow this solution to be as close to manufacturability as possible.

In real PCB designs, the via pad size is 10 mils over drill size and the designers need to keep 5 mil copper to pad space. Meaning, for a 10 mil drill diameter (not finished hole size) the pad diameter is 20 mils, and the minimum antipad diameter is 30 mils. Some high end PCB fabricators can do better for pad diameter and anti-pad diameter;

though, a mil for each via feature at most. Therefore, it is not necessarily feasible to make anti-pad less than 30 mils in this example, even though there is no pad on the inner layer since these dimensions are set to allow for drill wander and layer misregistration and to not result in an electrical short [23].

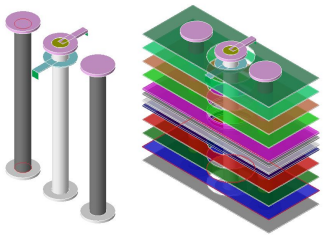

Figure 5 - Depiction of single-ended 3D Via Model Structure with feeds from L1 to L3, left image depicts via structure with plane layers turned enabled

Table 3 - Via Parameter Definition

Drill Diameter	10 mil	
Pad Diameter	20 mil	
Anti-pad	30 mil	
Plating Thickness	2 mil	
Stitching Via Drill Diameter	10 mil	
Stitching Via Pad Diameter	20 mil	
Single Via Parameters		
L1 feed width/length	4 mil / 15 mil	Single Via parameter
L3 feed width/length	5 mil /15 mil	Single Via parameter

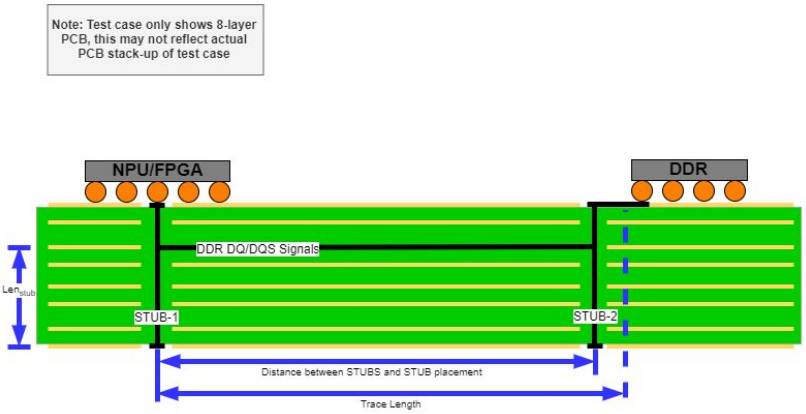

Figure 6 - Test Case #2 - 2D Model Depiction of DDR4 Data Signals Point-to-Point With Vias

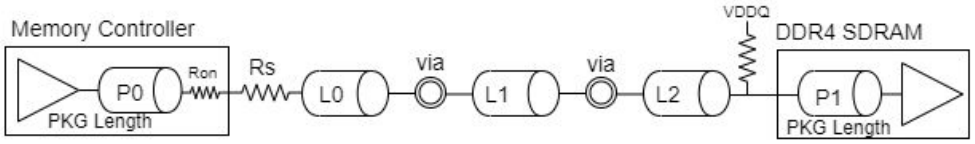

Figure 7 - Test Case #2 - DQ Channel Model of DDR4 Data Signals Point-to-Point With Vias in the Channel

Table 4 - Test Case #2 - Impedance, Length, and Spacing Guidelines for DDR4 Signals

Test Case #2				
Parameter	**L0 (CTL Breakout)**	**L1 (MB PCB)**	**L2 (L1 to DRAM)**	**Units**
Trace Type	Microstrip - L1	Stripline - L3	Microstrip - L1	-
DQ single-ended impedance Z_0	50+/- 10%	50+/- 10%	50+/- 10%	Ω
DQS differential impedance Z_{DIFF}	100+/- 10%	100+/- 10%	100+/- 10%	Ω
DQ trace width (nominal)	4.0	5	4.0	mil
DQS differential trace width/spacing	4.0/15	4.5/15.0	4.0/15.0	mil
Trace length	≤ 0.02	0.44	≤ 0.04 + 0.437 =0.477	inches
Spacing in byte lane signals (minimum)	15.0	15.0	15.0	mil
Maximum PCB via count	2 vias each with 60 mils in feeds			-
Total Channel Length	L0 + L1 + L2 = 0.937			inches

IV.1.3. TEST CASE #3 - SINGLE DDR4 DIMM PER CHANNEL

The objective of test case #3 is to understand if the DDR4-3200 eye mask violations will occur with multiple discontinuities in the DDR4 channel including vias, DIMM PCB, and DIMM connector in comparison to a channel of the same length in test case #2 without the DIMM interconnect. Further, the limits of this test case will be explored in order to understand where link failures can occur with a DIMM card as part of the DDR channel.

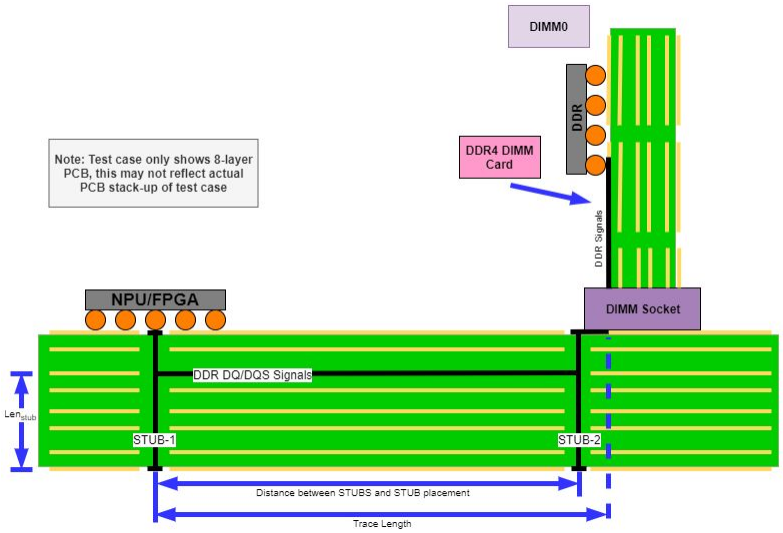

Figure 8 - Test Case #3 - 2D Model Depiction of Single DDR4 DIMM per Channel

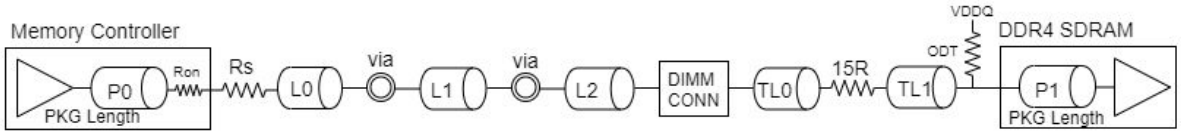

Figure 9 - Test Case #3- DQ Channel Model of Single DDR4 DIMM per Channel

Table 5 - Test Case #3 - Impedance, Length, and Spacing Guidelines for DDR4 Signals

Test Case #3						
Parameter	**L0 (CTL Breakout)**	**L1 (MB PCB)**	**L2 (L1 to DIMM CONN)**	**TL0 (D1 DIMM)**	**TL1 (D1 DIMM)**	**Units**
Trace Type	Microstrip - L1	Stripline - L3	Microstrip - L1	Microstrip - L1	Microstrip - L1	-
DQ single-ended impedance Z_0	50+/- 10%	50+/- 10%	50+/- 10%	50+/- 10%	50+/- 10%	Ω
DQS differential impedance Z_{DIFF}	100+/- 10%	100+/- 10%	100+/- 10%	85+/- 15%	85+/- 15%	Ω
DQ trace width (nominal)	4.0	5.0	4.0	6.0	6.0	mil
DQS differential trace width/spacing	4.0/15	4.5/15.0	4.0/15.0	5.5/4.0	5.5/4.0	mil
Trace length	≤ 0.02	0.44	≤ 0.04	(DQ) 0.11417 / (DQS) 0.125	(DQ) 0.3228 / (DQS) 0.232	inches
Spacing in byte lane signals (minimum)	15.0	15.0	15.0	4.0	4.0	mil
Maximum PCB via count	2 vias			no vias on DIMM		-
Total Channel Length (DQ)	L0 + L1 + L2 = 0.5			TL0 + TL1 = 0.437		inches
Total Channel Length (DQ)	L0 + L1 + L2 + 2*(Via feed) + TL0 + TL1 = 0.937					inches

Micron has DDR4 SDRAM RDIMM - 8GB (MPN: MTA9ASF1G72PZ) that supports PC4-3200. This RDIMM is a 288-pin RDIMM (MO-309, R/C-D1 format). The R/C-D1 RDIMM is defined by JEDEC standard [6]. The RDIMM DDR4 R/C D1 fabrication table which can be referenced in that JEDEC standard [6] was used to create the ADS stackup shown in figure A.7, which is used as part of the test case #3 simulation model. The net Structure for JEDEC RDIMM DQ signals does include 15R resistors in line with each signal on the RDIMM.

V. SIMULATION RESULTS AND ANALYSIS

For all cases, eye mask simulations are depicted as per JEDEC standard [5]; see also table 1.

V.1. TEST CASE #1 SIMULATION RESULTS

As shown by figure 10, the simulated channel for test case #1 does comply with the JEDEC DDR4-3200 BER requirements (eyes are open) for DQ[0-2], when all signals are routed on the top layer.

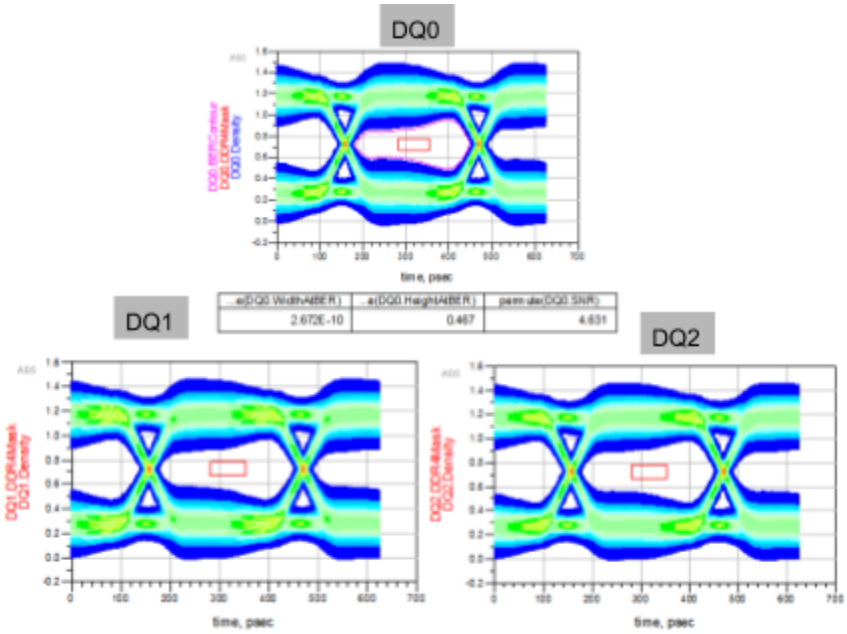

Figure 10 - Test Case #1 - DQ[0-2] - Data rate = 3200 Mbps, MB = 16L PCB, NO VIAS in the channel, Rs = 25, ODT = 240, MB Channel Length = 937 mil, ALL SIGNALS ON TOP LAYER

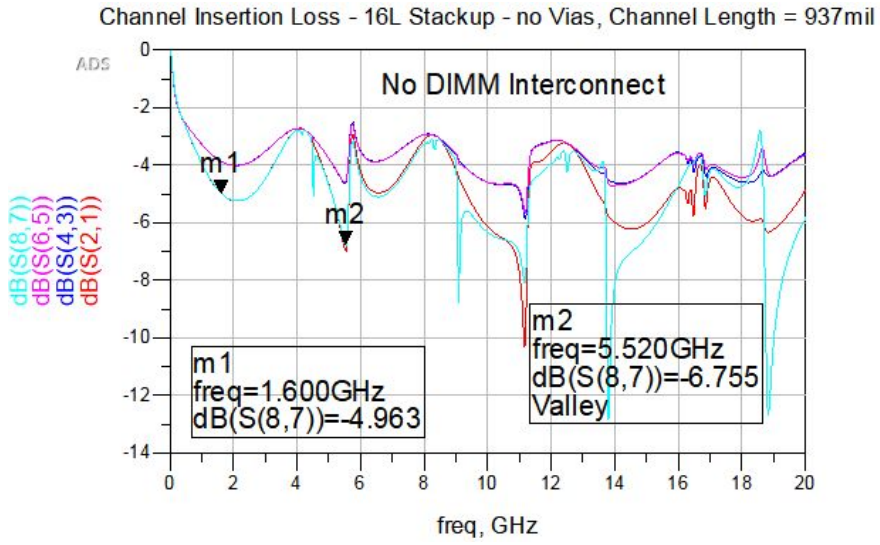

Figure 11 - Test Case #1 - DQ Channel Insertion Loss without stubs in channel

V.2. TEST CASE #2 SIMULATION RESULTS

Results shown below are after tuning the channel at 3200 Mbps, for the best Rs and ODT values. Due to the model limitations discussed in test case #3, only 4 bits DQ[0-3] and DQS were simulated to match the same parameters of test case #3. The results of each channel simulation can be referenced in table 6.

As shown in figure 13, the maximum stub length to meet DDR4-3200 compliance requirements for a 937 mil long channel is 73 mils. By referring to figures 15 and 16, the insertion loss in the channel doubles at 12 GHz by increasing the stub length from 73 mils to 83 mils.

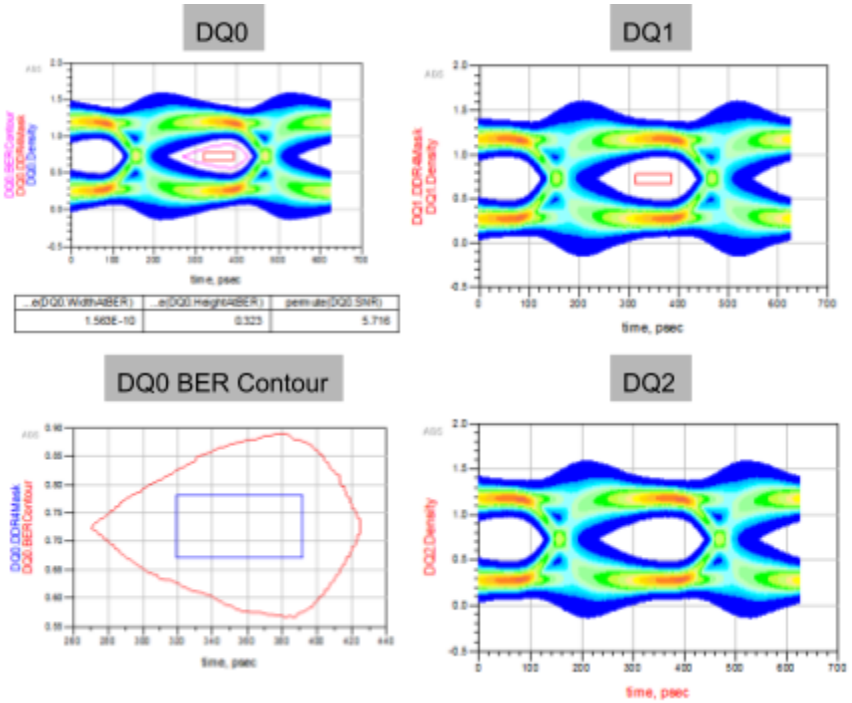

Figure 12 - Test Case #2 - DQ[0-3] - Data rate = 3200 Mbps, MB = 14L PCB (52.7 mil stubs), Rs = 25, ODT = 240, Total Channel Length = 937 mil

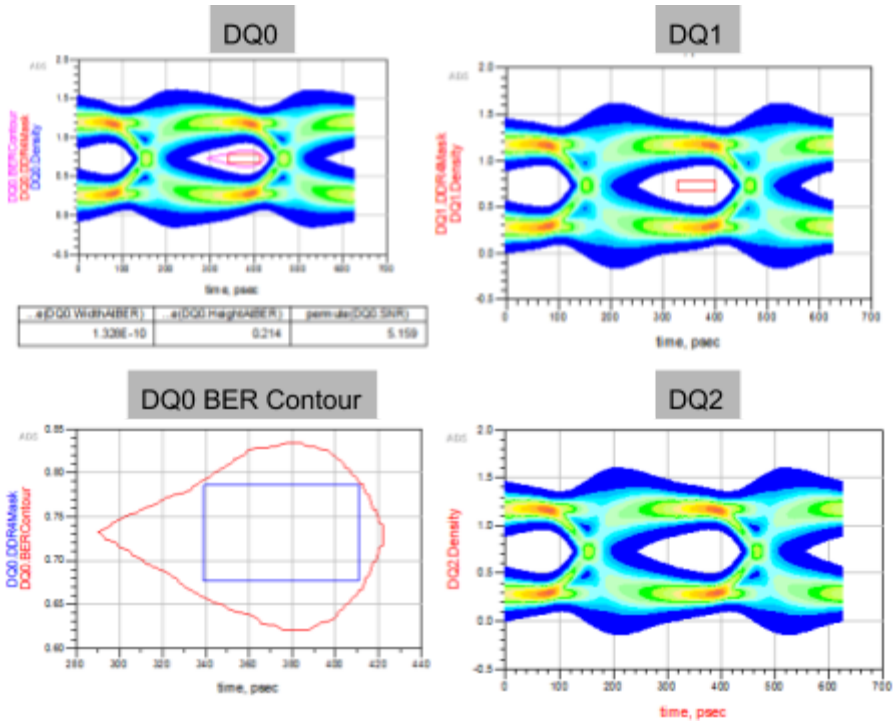

Figure 13 - Test Case #2 - DQ[0-2] - Data rate = 3200 Mbps, MB = 18L PCB (73.1 mil stubs), Rs = 25, ODT = 240, Total Channel Length = 937 mil

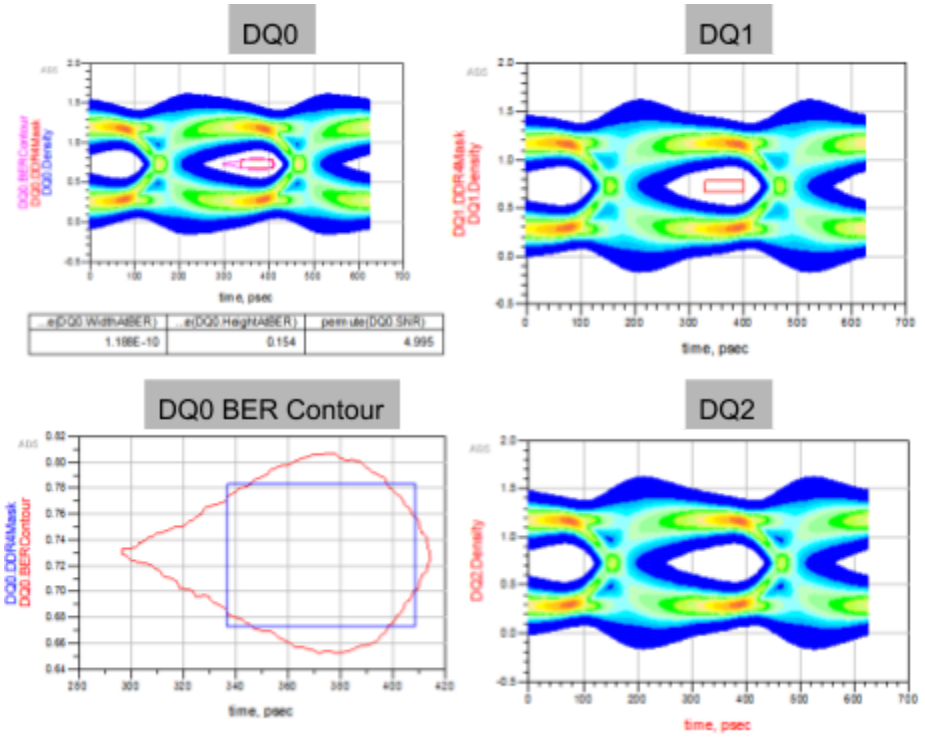

Figure 14 - Test Case #2 - DQ[0-2] - Data rate = 3200 Mbps, MB = 20L PCB (83.3 mil stubs), Rs = 25, ODT = 240, Total Channel Length = 937 mil

Table 6 - Test Case #2 Results Summary

TEST CASE #2 - DQ0 DDR BUS SIMULATION RESULT @ BER 1E-16, Rs = 25Ω, ODT - 240Ω, DATA RATE = 3200, Total Channel Length = 937 mil			
Via Stub-Length (mil)	Via Stub Resonant Frequency F_o (GHz)	PCB Stack-up	DDR4-3200 Eye Mask Violation (PASS/FAIL)
52.7	19.39	14L	PASS
62.9	15.625	16L	PASS
73.1	14.271	18L	PASS
83.3	12.143	20L	FAIL
92.1	11.429	22L	FAIL
104.1	10.238	24L	FAIL
114.3	9.2453	26L	FAIL
124.7	8.5714	28L	FAIL

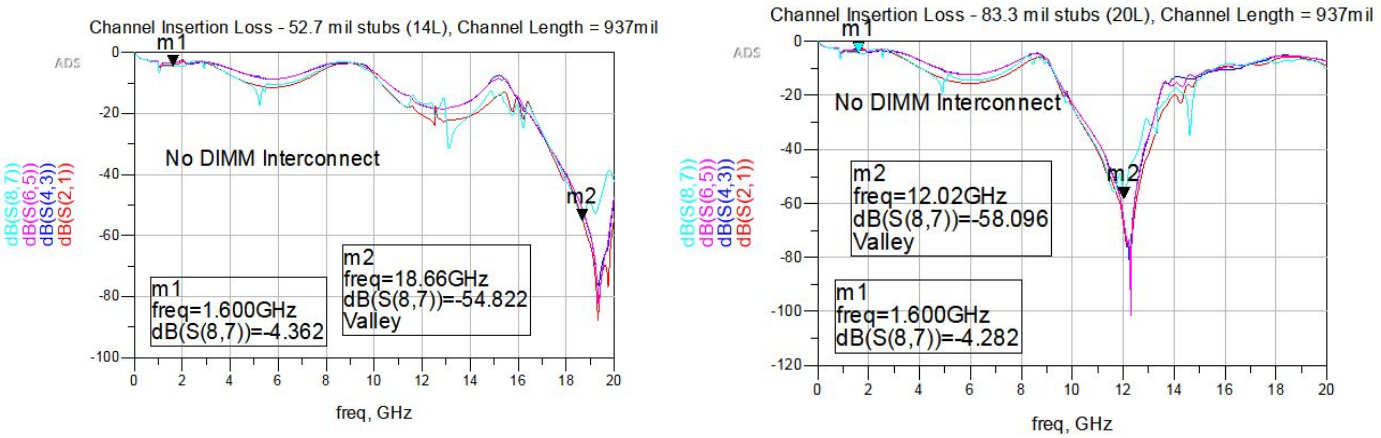

Figure 15 - Test Case #2 - DQ Channel Insertion Loss Without Stubs and With 83 mil Stubs in Channel

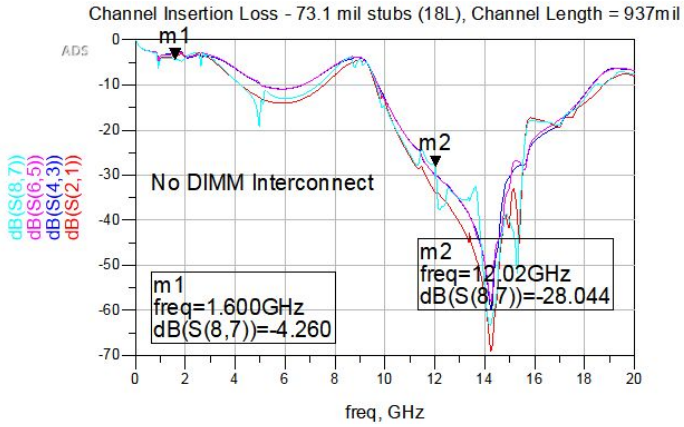

Figure 16 - Test Case #2 - DQ Channel Insertion Loss Without Stubs and With 73 mil Stubs in Channel

V.3. TEST CASE #3 SIMULATION RESULTS

Results shown below are after tuning the channel at 3200 Mbps, for the best Rs and ODT values. Only 4 bits DQ[0-3] and DQS can be simulated with the test case 3 model due to the Amphenol DIMM model only having 12 ports. All other bits DQ[4-7] are terminated to 50 ohms. The results of each channel simulation can be referenced in table 7.

As shown by figure 17, even with only the DIMM connector, the DIMM interconnect, and no vias included in the channel, it is not feasible to achieve data rates of 3200 Mbps in a DDR4 channel. This is primarily due to the channel losses from the DIMM components. Figure 17 to figure 18 are part of the results used to compile table 7. As shown by figure 21, as the ISI increases due to the longer stub discontinuities in the channel, the eye collapses. By knowing that 1 UI for 3200 Mbps data rate is equal 312.5 ps, the deterministic jitter can be estimated by subtracting the eye width from 1 UI. This is shown by the graph in figure 22. As a comparison figure 22 also depicts the estimated deterministic jitter for test case #2.

As per the eye diagrams depicted in test case #3, specifically figure 18 to figure 19, the degree of ISI from losses of the via discontinuities in the channel is collapsing the eye diagram at a data rate of 3200 Mbps even at a stub length of 52.7 mils.

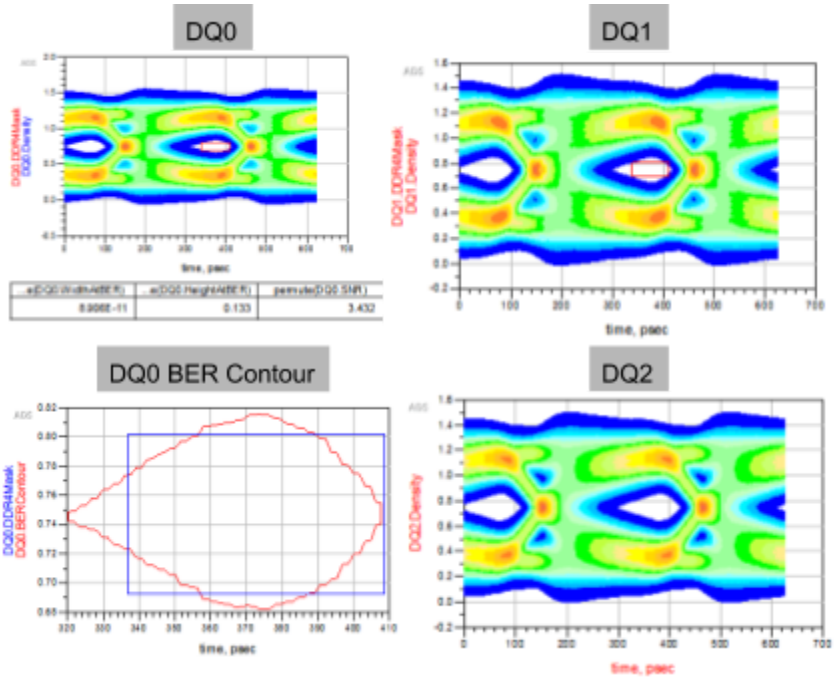

Figure 17 - Test Case #3 - DQ[0-2] - Data rate = 3200 Mbps, MB = 16L PCB, NO VIAS in the channel, Rs = 25, ODT = 240, MB CH Length = 500 mil, Total Channel Length = 937 mils, ALL SIGNALS ON TOP LAYER

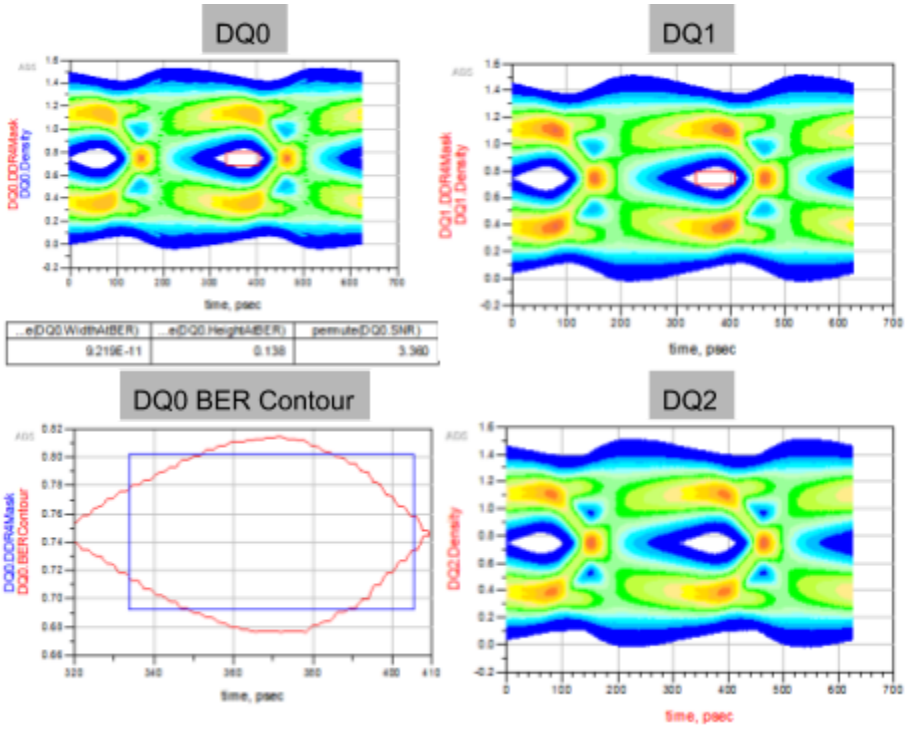

Figure 18 - Test Case #3 - DQ[0-2] - Data rate = 3200 Mbps, MB = 14L PCB (52.7 mil stubs), Rs = 25, ODT = 240, MB Channel Length = 500 mils, Total Channel Length = 937 mils

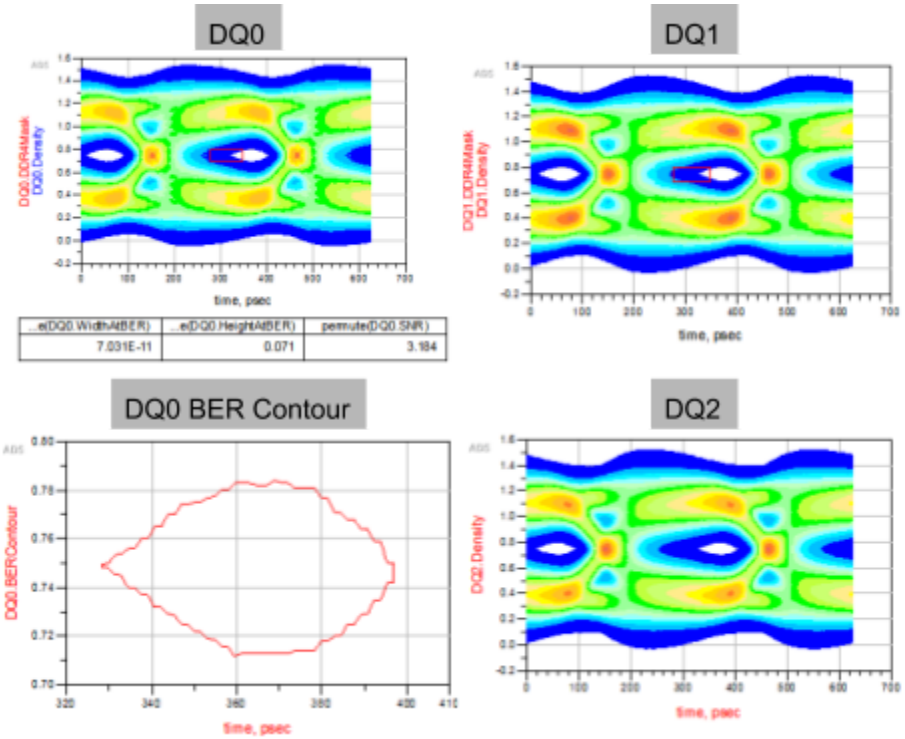

Figure 19 - Test Case #3 - DQ[0-2] - Data rate = 3200 Mbps, MB = 20L PCB (83.3 mil stubs), Rs = 25, ODT = 240, MB Channel Length = 500 mils, Total Channel Length = 937 mils

Table 7 - Test Case #3 Results

TEST CASE #3 - DQ0 DDR BUS SIMULATION RESULT @ BER 1E-16, Rs = 25Ω, ODT - 240Ω, DATA RATE = 3200			
Via Stub-Length (mil)	Via Stub Resonant Frequency F_o (GHz)	PCB Stack-up	DDR4-3200 Eye Mask Violation (PASS/FAIL)
52.7	19.39	14L	FAIL
62.9	15.625	16L	FAIL
73.1	14.271	18L	FAIL
83.3	12.143	20L	FAIL
92.1	11.429	22L	FAIL
104.1	10.238	24L	FAIL
114.3	9.2453	26L	FAIL
124.7	8.5714	28L	FAIL

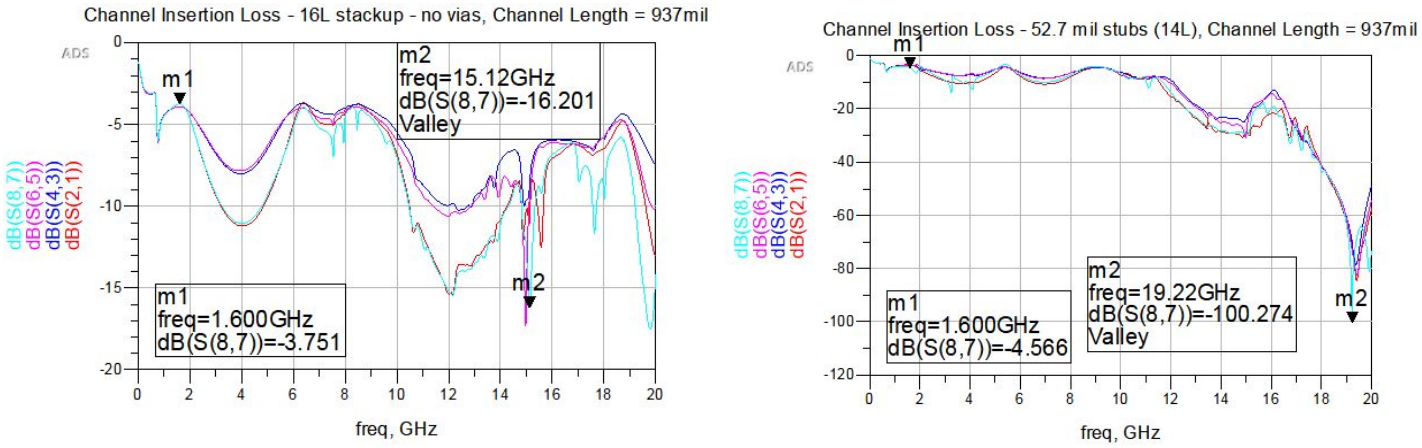

Figure 20 - Test Case #3 - DQ Channel Insertion Loss without stubs and with 52 mil stubs in channel

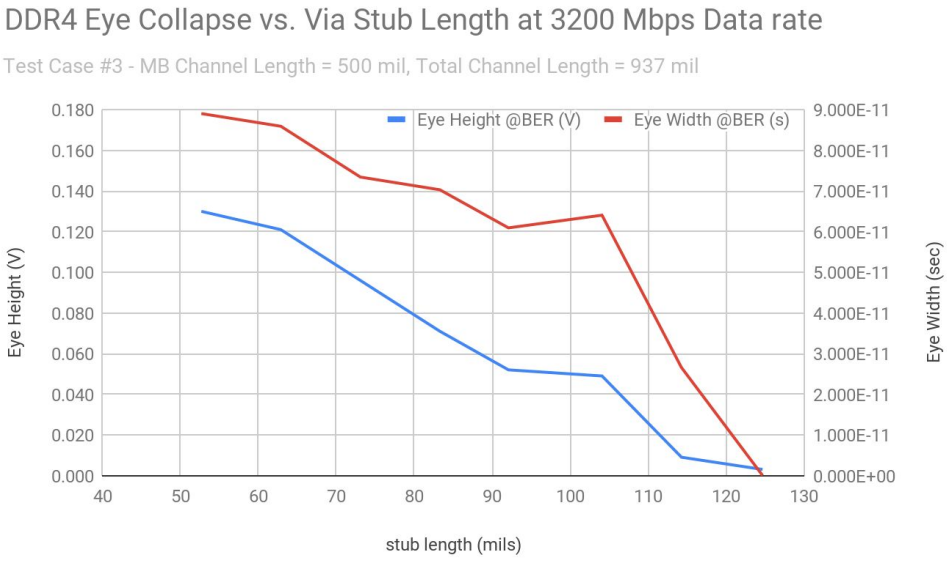

Figure 21 - Test Case #3 - Summary of DDR4 Eye results vs. Stub length with DIMM

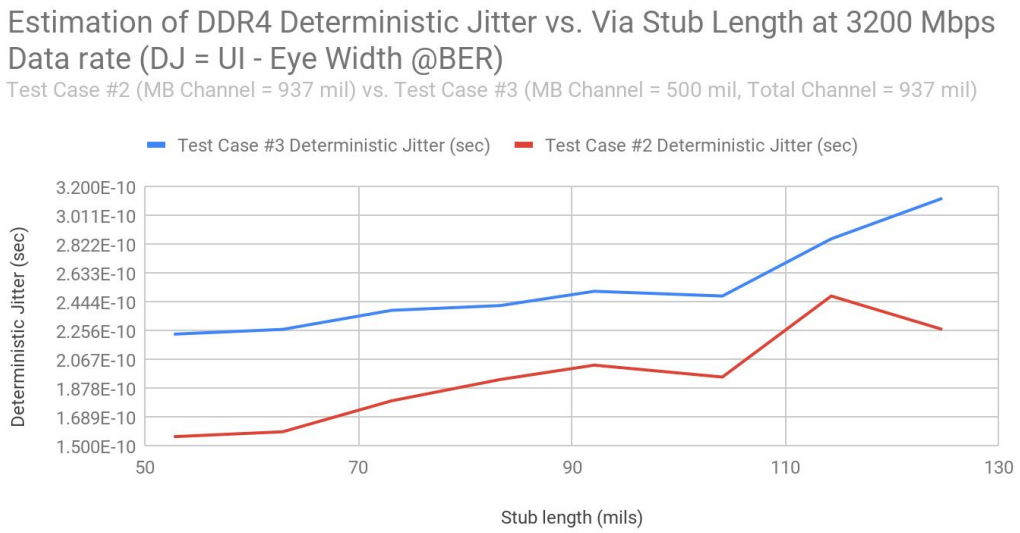

Figure 22 - Deterministic Jitter Estimation vs. Stub length for DDR4 Channel for with and without DIMM

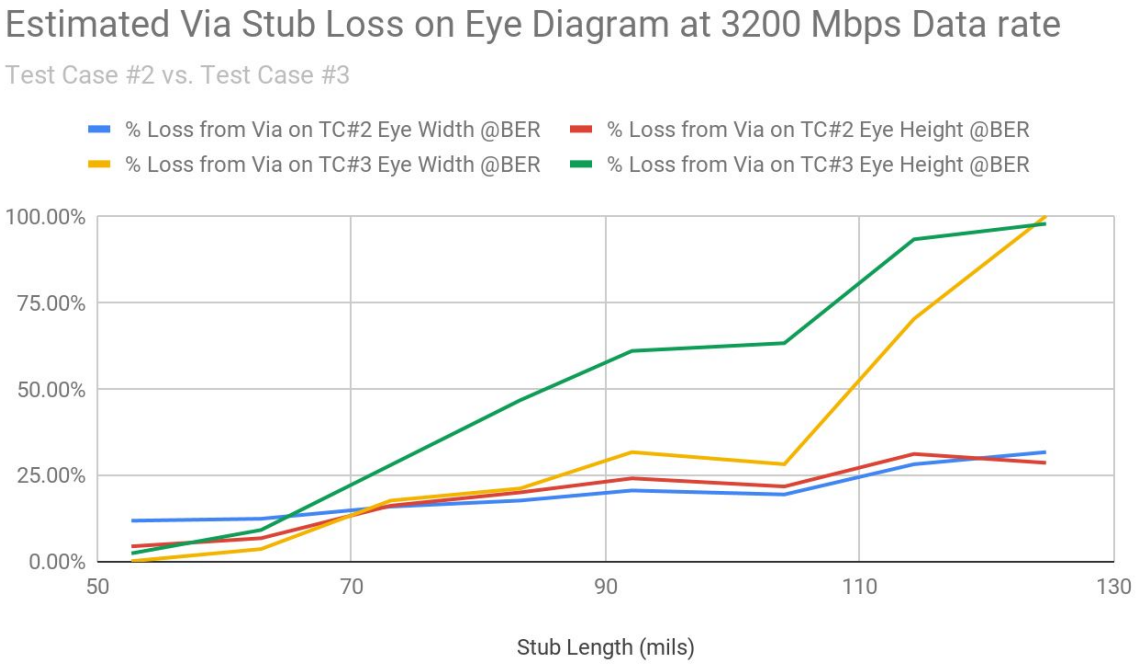

Figure 23 - Estimated Via Stub Loss on Eye Diagram at 32000 Mbps Data Rate with and without DIMM

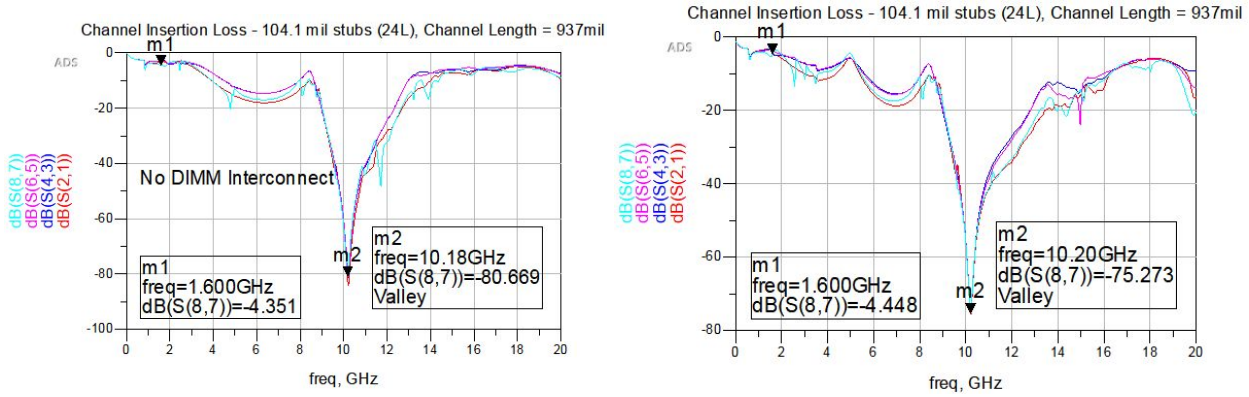

Figure 24 - DQ Channel Insertion Loss with 104.1 mil stubs in channel, with and without DIMM

VI. CONCLUSIONS AND SUMMARY

Bit error rates can often be predicted by two important aspects of eye diagrams: the vertical opening and the horizontal opening [10]. This is demonstrated through simulation of the channel model defined in test case #2. It is not currently feasible to achieve data rates of 3200 Mbps in the DDR4 with a stub length of ~92 mils. In addition, as shown by the channel model defined in test case #3, it is not currently feasible to achieve data rates of 3200 Mbps in the DDR4 with a stub length of ~53 mils. Further work would need to be done to understand where the max stub length in these channel models exists.

As shown by figure 23, the maximum eye diagram loss for test case #2 varies between ~2% to ~30%, depending on the stub length in the channel. When one adds in the DIMM connector and DIMM interconnect, the channel sees a compounding additional amount of loss. With reference to figures 21 and 23, a designer can clearly see that when the stub length becomes greater than ~104 mils, which represents a 24L stack-up, the slope of the loss seen in the channel becomes even steeper for both test cases #2 and #3. When the DQ channel is routed using a 24L stack-up with vias, the channel has a resonant frequency of ~10.2 GHz as shown by figure 24. Although this resonant frequency is more than 5 times greater than the data rate clock frequency, without the additional losses added in the channel from the DIMM, link failures will occur. The next steps of this effort would be to compile simulation data with a memory controller that supports 3200 Mbps, which was not available when this effort was started.

VII. ACKNOWLEDGEMENTS

I would also like to express my appreciation to Bert Simonovich, Lee Ritchey and John Zasio for their support and mentorship.

I would like to thank Amphenol and Jason Ellison for providing me with DDR4 DIMM connector models. I would also like to thank all of the reviewers of this paper, Bruce Magid, Bert Simonovich, Jason Ellison, and John Zasio. In addition, I would like to thank Keysight, for providing me with excellent technical support while I used their ADS software tool for building my simulation models.

Most importantly, I wish to thank my loving wife, Stephanie, for her patience and support, which allowed me to write this paper. You are truly an amazing person.

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IX. APPENDIX

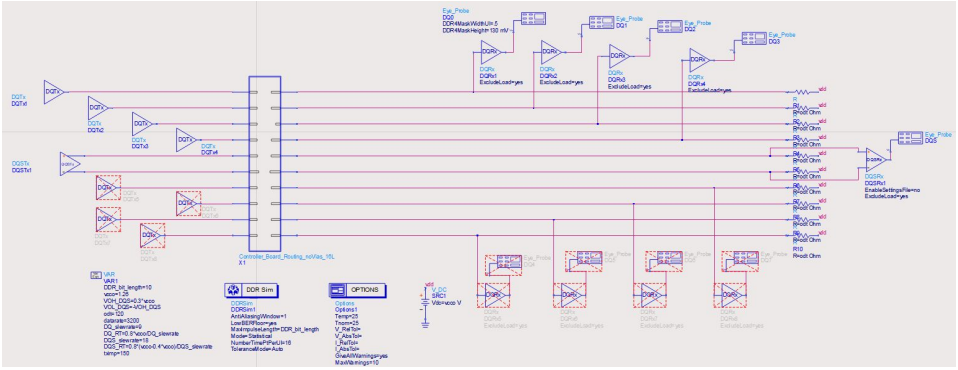

Figure A.1 - Test Case 1 - ADS Channel Model

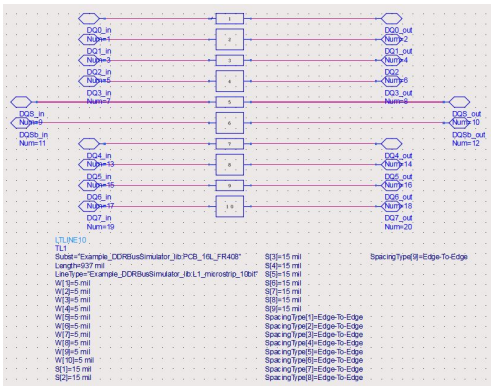

Figure A.2 - Test Case 1 - ADS Motherboard Channel Model

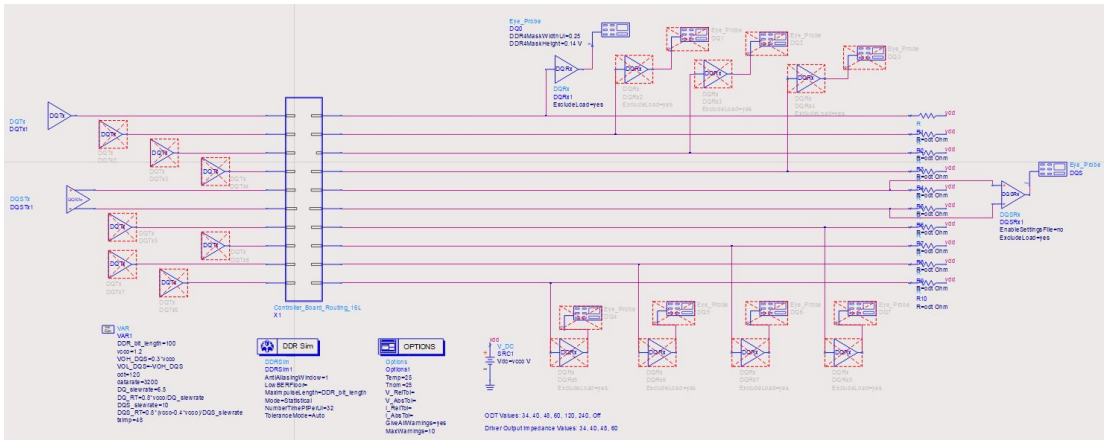

Figure A.3 - Test Case 2 - ADS Channel Model

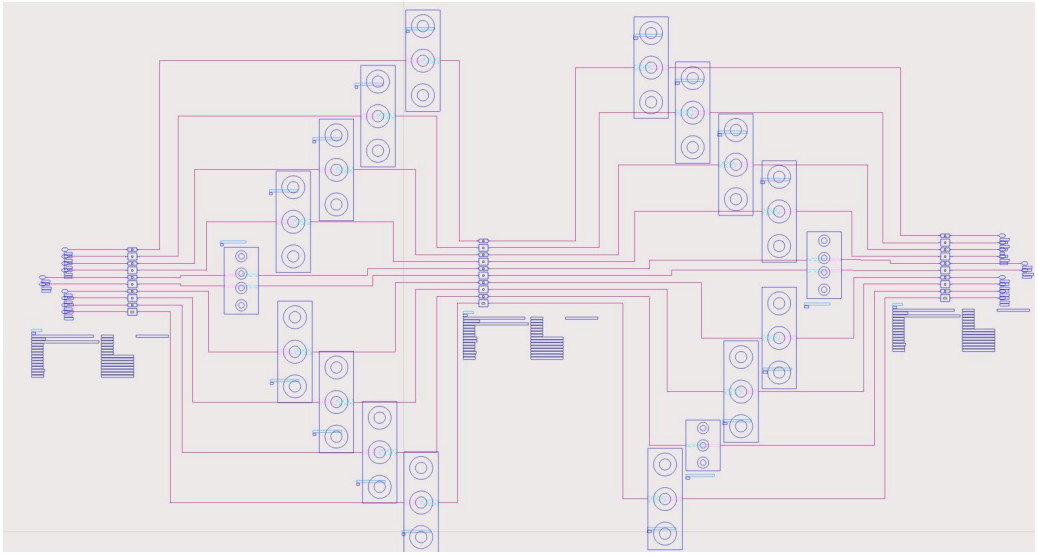

Figure A.4 - Test Case 2 and Test Case 3 - ADS Motherboard Channel Model

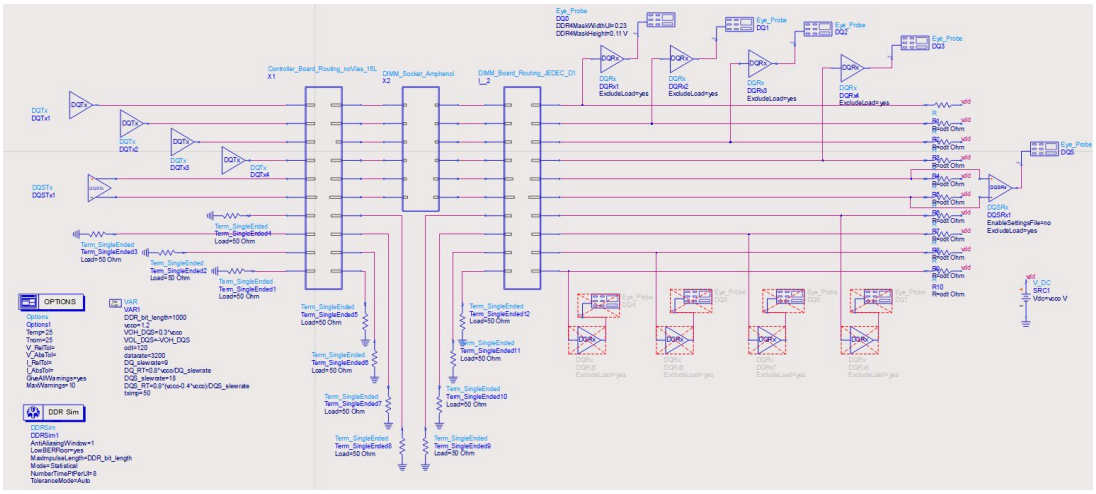

Figure A.5 - Test Case 3 - ADS Channel Model

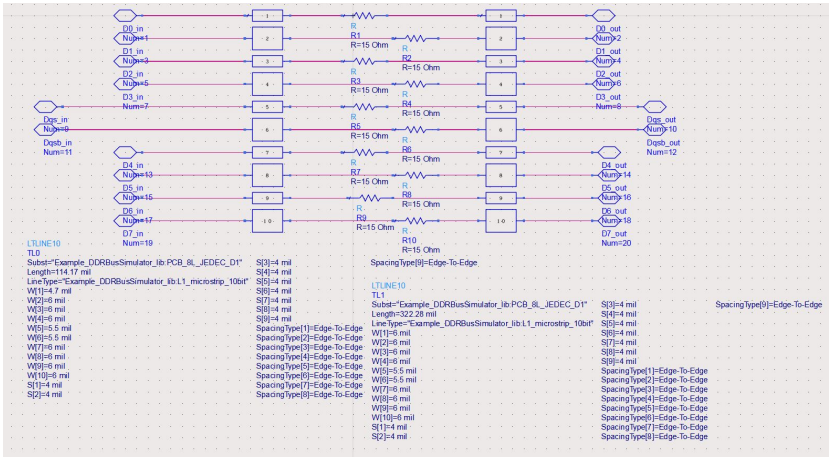

Figure A.6 - Test Case 3 - ADS JEDEC R/C D1 DIMM Channel Model

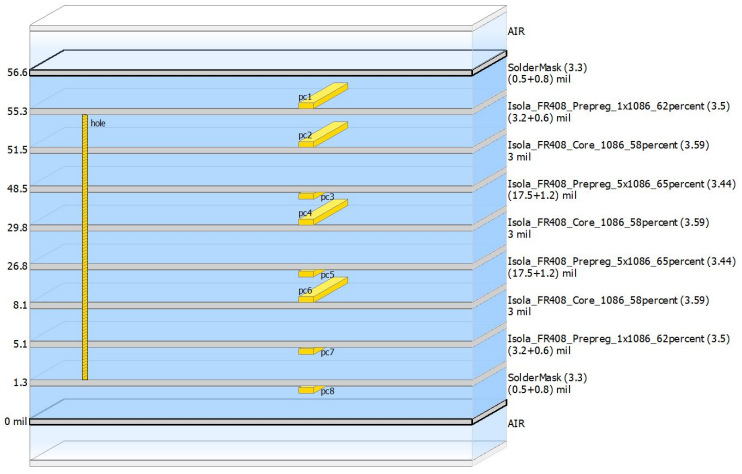

Figure A.7 - ADS JEDEC RDIMM R/C D1 8L PCB Stack-up

Table A.1 - JEDEC RDIMM R/C D1 Transmission Line Impedance Analysis of D1 8L Stack-up shown in figure A.7

PCB Stack-up / T-Line Type - Layer	Impedance (Ω)
8L / Single-ended (Z_c) Microstrip - L1	49.76
8L / Differential (Z_{diff}) Microstrip - L1	86.99

IX.1 DEFINITION OF PCB STACK-UPS

Multiple PCBA stack-ups have been defined and complete models have been developed in ADS. Single ended signals are using impedances on both L1 and L3 based on these stack-ups to meet 50 ohm impedance +/- 10%. Differential signals are using impedances on both layer 1 (L1) and layer (L3) based on these stack-ups to meet 100 ohm differential impedance +/- 10%. The calculated impedances for each respective layer and stack-up are shown below. The impedances are based on the trace width / spacing as defined in section 4.

Table A.2 - Motherboard (MB) Transmission Line Impedance Analysis

PCB Stack-up / T-Line Type - Layer	Impedance (Ω)
16L / 20L / 24L / 28L / Single-ended (Z_c) Microstrip - L1	49.17
16L / 20L / 24L / 28L / Single-ended (Z_c) Stripline - L3	47.16
16L / 20L / 24L / 28L / Differential (Z_{diff}) Microstrip - L1	95.68
16L / 20L / 24L / 28L / Differential (Z_{diff}) Stripline - L3	99.2
14L / 18L / 22L / 26L / Single-ended (Z_c) Microstrip - L1	46.96
14L / 18L / 22L / 26L / Single-ended (Z_c) Stripline - L3	47.16
14L / 18L / 22L / 26L / Differential (Z_{diff}) Microstrip - L1	91.62
14L / 18L / 22L / 26L / Differential (Z_{diff}) Stripline - L3	99.2

Figure A.9 - Definition of 14L PCB Stack-up (left) and 16L PCB Stack-up (right)

Figure A.10 - Definition of 18L PCB stack-up (left) and 20L PCB Stack-up (right)

Figure A.11 - Definition of 22L PCB Stack-up (left) and 24L PCB Stack-up (right)

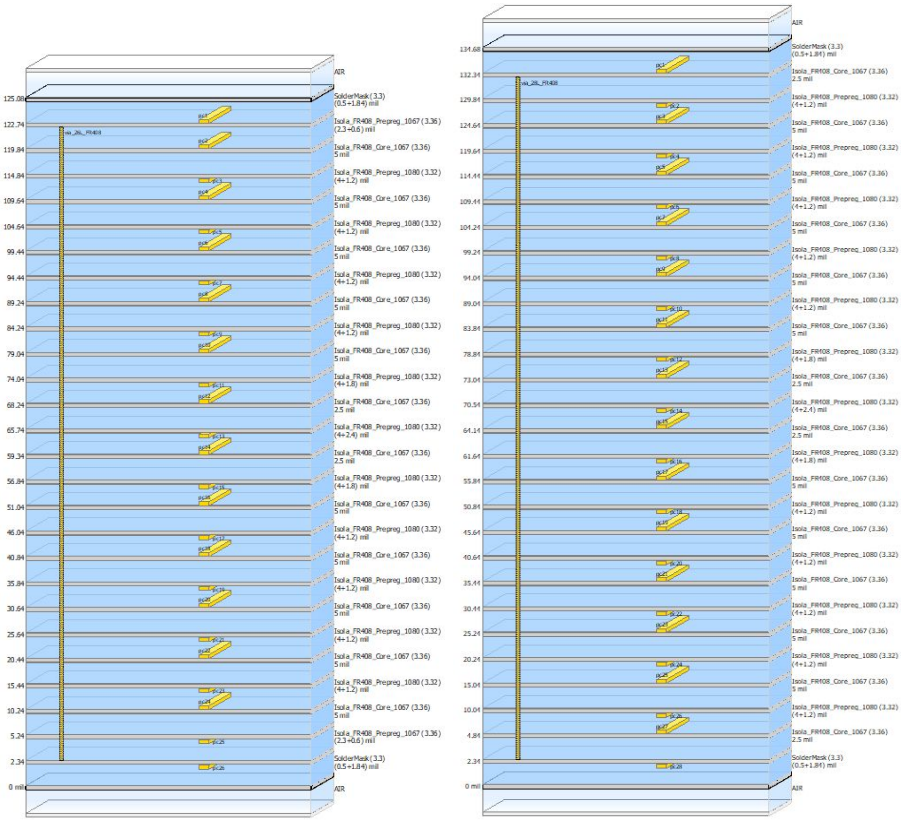

Figure A.12 - Definition of 26L PCB stack-up (left) and 28L PCB Stack-up (right)