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Project X DDR4-2400 Signal Integrity Analysis

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April 8, 2021

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Outline

- Design Assumptions
- System Models
- Single Byte Lane - DQ[7:0] Channel Analysis
- Single Byte Lane - DQ[7:0] Write Results
- 2 Byte Lane - DQ[15:0] + DM[1:0] + DQS1 + DQS0 Read/Write Results
- 4 Byte Lane - DQ[31:0] + DM[3:0] + DQS[3:0] + CLK0 Write Results
- A[7:0] Write Results with UDIMM
- A[7:0] Write Results with RDIMM
- Follow Up Questions

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Design Assumptions

- Simulation Temp: Room Temp (25°C)
- Not Power Aware SI - Power Integrity is not included in any of these models
- No DFE or EQ enabled

Simulation Setup

- Unless otherwise stated, all Models will include 2% RANDOM JITTER (RJ) => 0.02 UI
  - At the memory controller for WRITE cycle – RJ = 8.333 ps for DQ, 4.17 ps for all other nets
  - At the SDRAM for READ cycle - RJ = 8.333 ps for DQ, 4.17 ps for all other nets
- All Simulations shown were done in ADS using Memory Designer
- Using ADS Memory Designer – Statistic based simulation and bit-by-bit simulations
  - Unless otherwise stated
- IBIS Corner setting = MAX
  - Unless stated otherwise models shown are for MAX IBIS corner type
- Unless otherwise stated, all EM extractions for Project X CCA, UDIMM CCA, and MCM model were done using SIPro
- Simulation models as shown include crosstalk as part of simulation as per MCM, Project X CCA, UDIMM CCA EM extraction configurations. Any included crosstalk is limited per connector and socket models.

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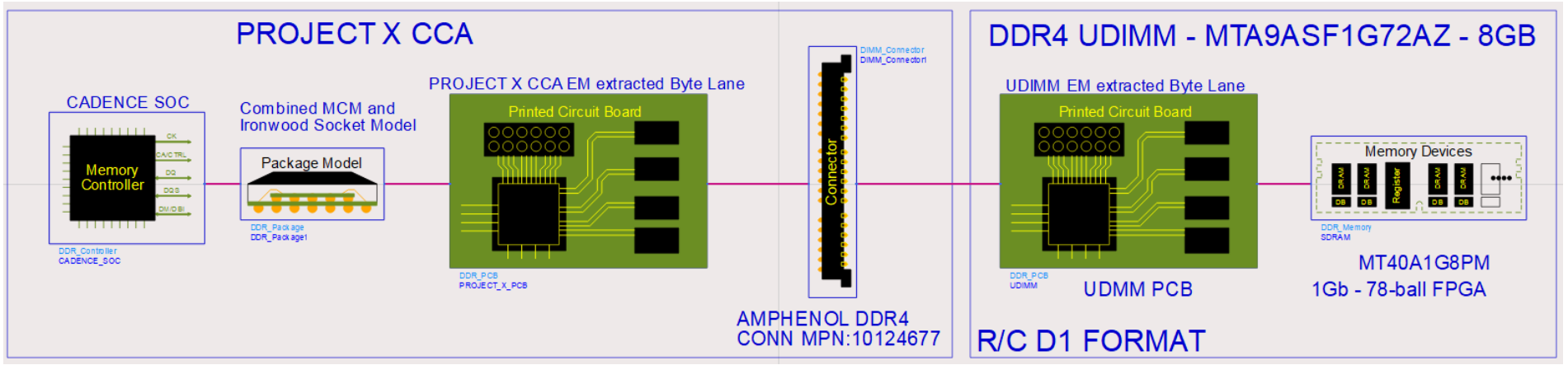
Project X CCA to UDIMM Model



PROJECT X CCA with DIMM CONNECTOR

UDIMM

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System Models - IBIS Models – CADENCE ASIC

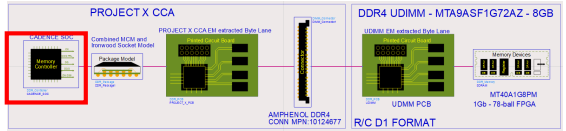
CADENCE MCM (ASIC) MPN: 828RA72

```
|*************************************************************************
| IBIS file created by T2B Version 17.2.9.04121.123020   009
| Cadence Design Systems, Inc. 2011
|*************************************************************************
[IBIS ver] 5.1
[File name]  gf_12lp_ddr4.ibs
[File Rev]  1.0
[Date]   December 4, 2019
```

Original Model had to be edited to include multiple additional pins for simulation

```
|*************************************************************************
| IBIS file created by T2B Version 17.2.9.04121.123020   009
| Cadence Design Systems, Inc. 2011
|*************************************************************************
[IBIS ver] 5.1
[File name]  gf_12lp_ddr4_edited_1v2.ibs
[File Rev]  1.2
[Date]   January 25, 2021
```

Model used for simulation



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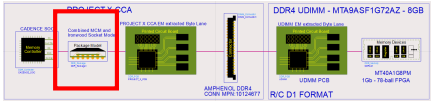
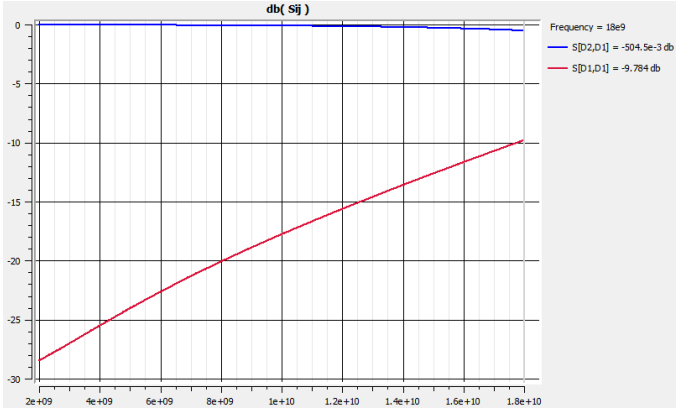
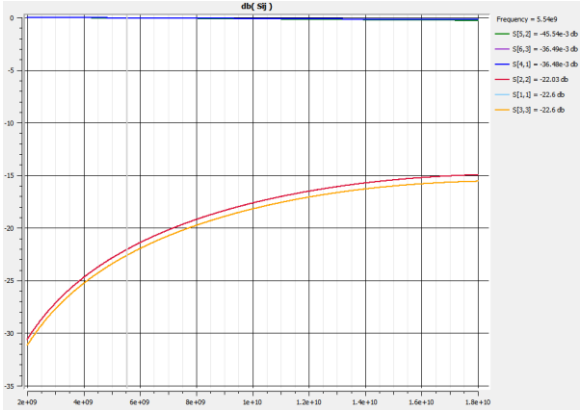
System Models – Socket Model



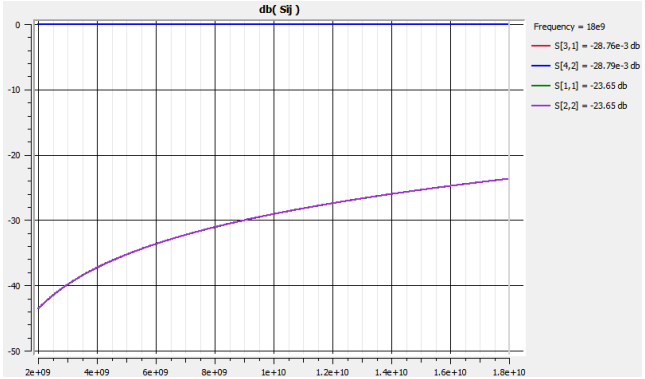
Ironwood_Differential_09-15-2020.s4p



Ironwood_Socket_SSS_07-09-2020.s6p



Ironwood_Socket_SGS_07-09-2020.s4p



- 3 Ironwood Socket Models were used in combination with the respective MCM model for the Package Model

=>MCM model + Socket model = Package Model
*This is shown later

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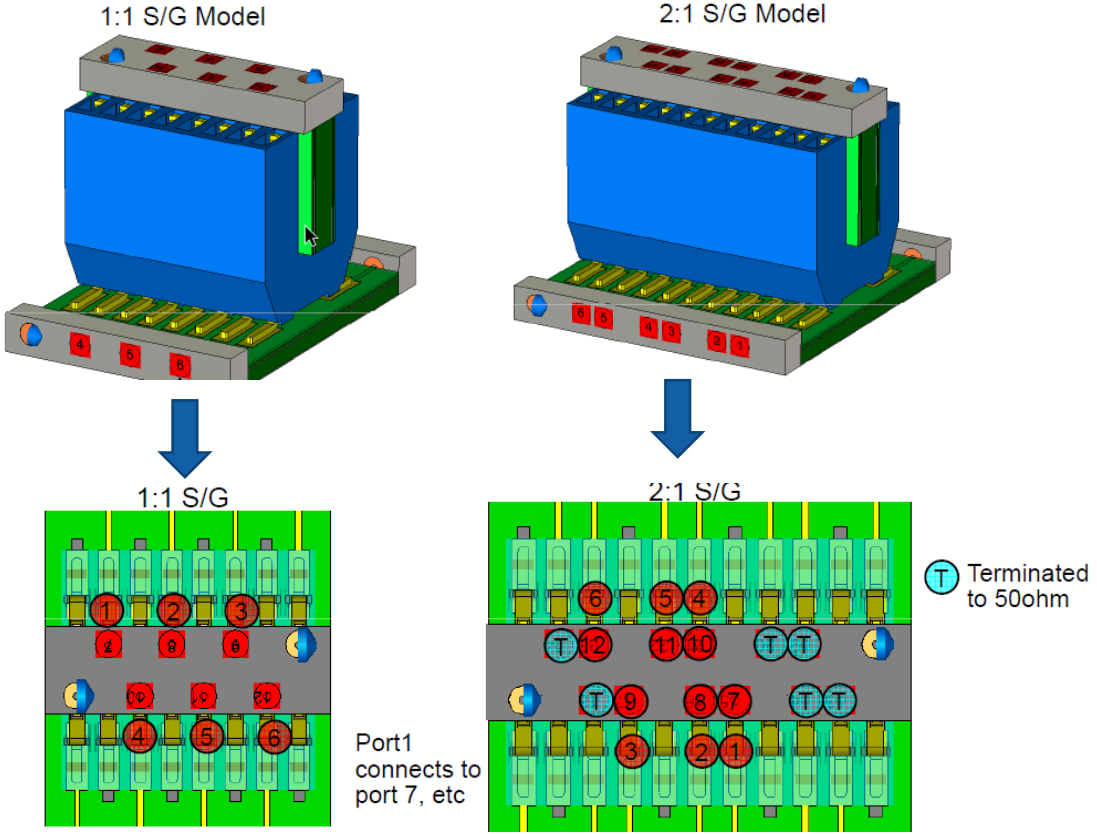
System Models - DDR4 288-pin DIMM Connector Model

AMPHENOL MPN: 10124677

Model Name:
SPa_DDR4_SMT_10124677_v4

DIMM Connector Model extracted from:
SPa_DDR4_SMT_10124677_v4.zip

2 DIMM connector Models were used in combination to form a complete DIMM connector model



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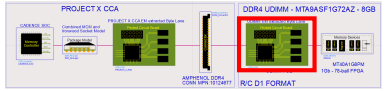
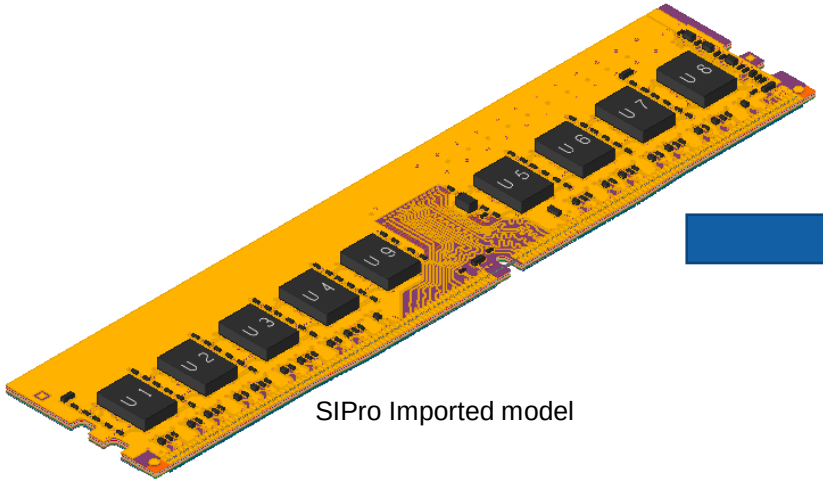
System Models - UDIMM R/C D1 Model & PCB Stack-Up

MICRON UDIMM MPN: [MTA9ASF1G72AZ – 8GB]

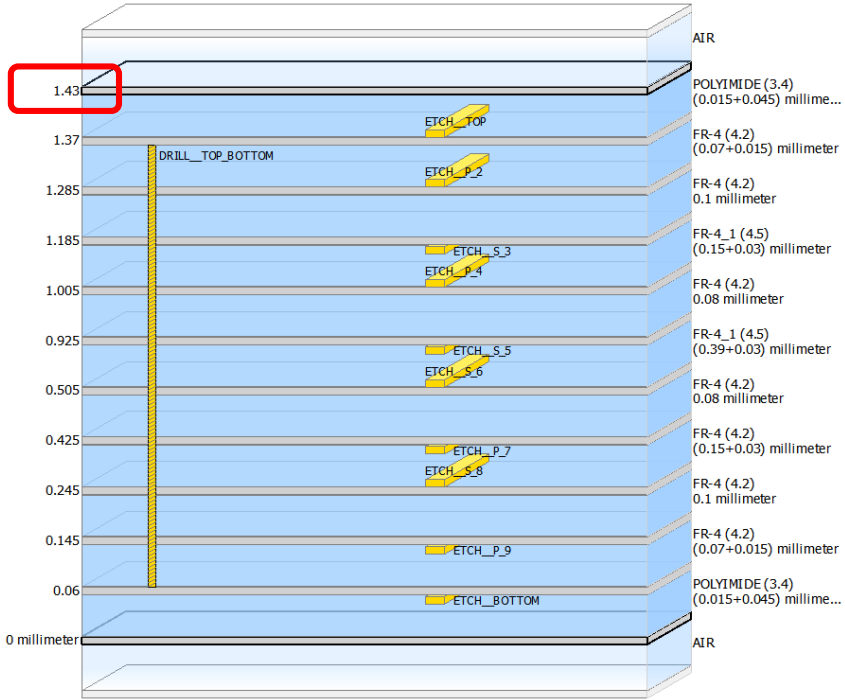
288-pin UDIMM (MO-309 R/C D1)



UDIMM Total PCB thickness: 1.43 mm = 56.3 mils



SIPro Imported model



[JEDEC UDIMM R/C D1] (imported DIMM)

10L Stack-up

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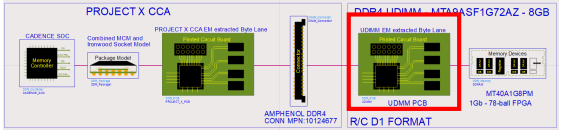
System Models - UDIMM R/C D1 Model & PCB Stack-Up



UDIMM Total Model thickness
= 1.43 mm – Solder mask (0.015*2) = 1.4 mm

=> Meets JEDEC DDR4 SDRAM UDIMM Design Specification (Rev. 1.10 Aug 2015) for 10L stack-up: 1400 um +/- 100 um

6.7 Reference Stackups

This section defines the preferred stackup for 6, 8, and 10 layer UDIMMs. Stackup for specific cards may be different from the preferred stackups in the tables below.

Table 15 — Preferred 10 Layer Stackup for UDIMMs

Layers				
	Solder Mask	15 µm		
1	Cu	45 µm	Signal	3/8 oz + Plating
	Prepreg	70 µm		
2	Cu	15 µm	VDD/VSS	1/2 oz
	Core	100 µm		
3	Cu	15 µm	Signal	1/2 oz
	Prepreg	150 µm		
4	Cu	15 µm	VDD/VSS	1/2 oz
	Core	80 µm		
5	Cu	15 µm	Signal	1/2 oz
	Prepreg	390 µm		
6	Cu	15 µm	Signal	1/2 oz
	Core	80 µm		
7	Cu	15 µm	VDD/VSS	1/2 oz
	Prepreg	150 µm		
8	Cu	15 µm	Signal	1/2 oz
	Core	100 µm		
9	Cu	15 µm	VDD/VSS	1/2 oz
	Prepreg	70 µm		
10	Cu	45 µm	Signal	3/8 oz + Plating
	Solder Mask	15 µm		

Total Thickness: 1400 ± 100 µm as measured across connector contact fingers (without solder mask)

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System Models - IBIS Models – UDIMM MICRON SDRAM

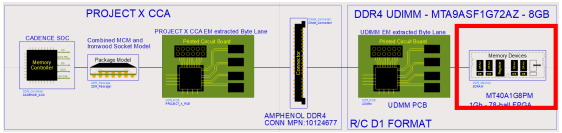
MICRON SDRAM MPN: MT40A1G8

| z91b.ibs * IBIS 4.2 Model
| 8Gb DDR4 SDRAM - Die Revision "A"
| This Model is valid for Commercial Temperature Range 0C<=Tc<=95C
|
| Valid for DDR4-1600/1866/2133/2400/2666 operation
| Models *_2666 are applicable for speed grade 2666 Mbps (-075) and below
|

Part Number	VDD/VDDQ	Architecture	Package
MT40A2G4PM	1.2V/1.2V	2Gb x 4	78-Ball FBGA
MT40A1G8PM	1.2V/1.2V	1Gb x 8	78-Ball FBGA
MT40A512M16HA	1.2V/1.2V	512Mb x 16	96-Ball FBGA
MT40A2G4Z91B	1.2V/1.2V	2Gb x 4	Bare Die
MT40A1G8Z91B	1.2V/1.2V	1Gb x 8	Bare Die
MT40A512M16Z91B	1.2V/1.2V	512Mb x 16	Bare Die

[IBIS Ver] 4.2
[File Name] z91b.ibs
[Date] 09/22/2014
[File Rev] 1.0
[Source] From silicon level SPICE model at Micron Technology, Inc.
For support e-mail modelsupport@micron.com

Model used for simulation



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DDR4-2400 DQ AND DQS ANALYSIS

1 Byte Lane

(Write Only)

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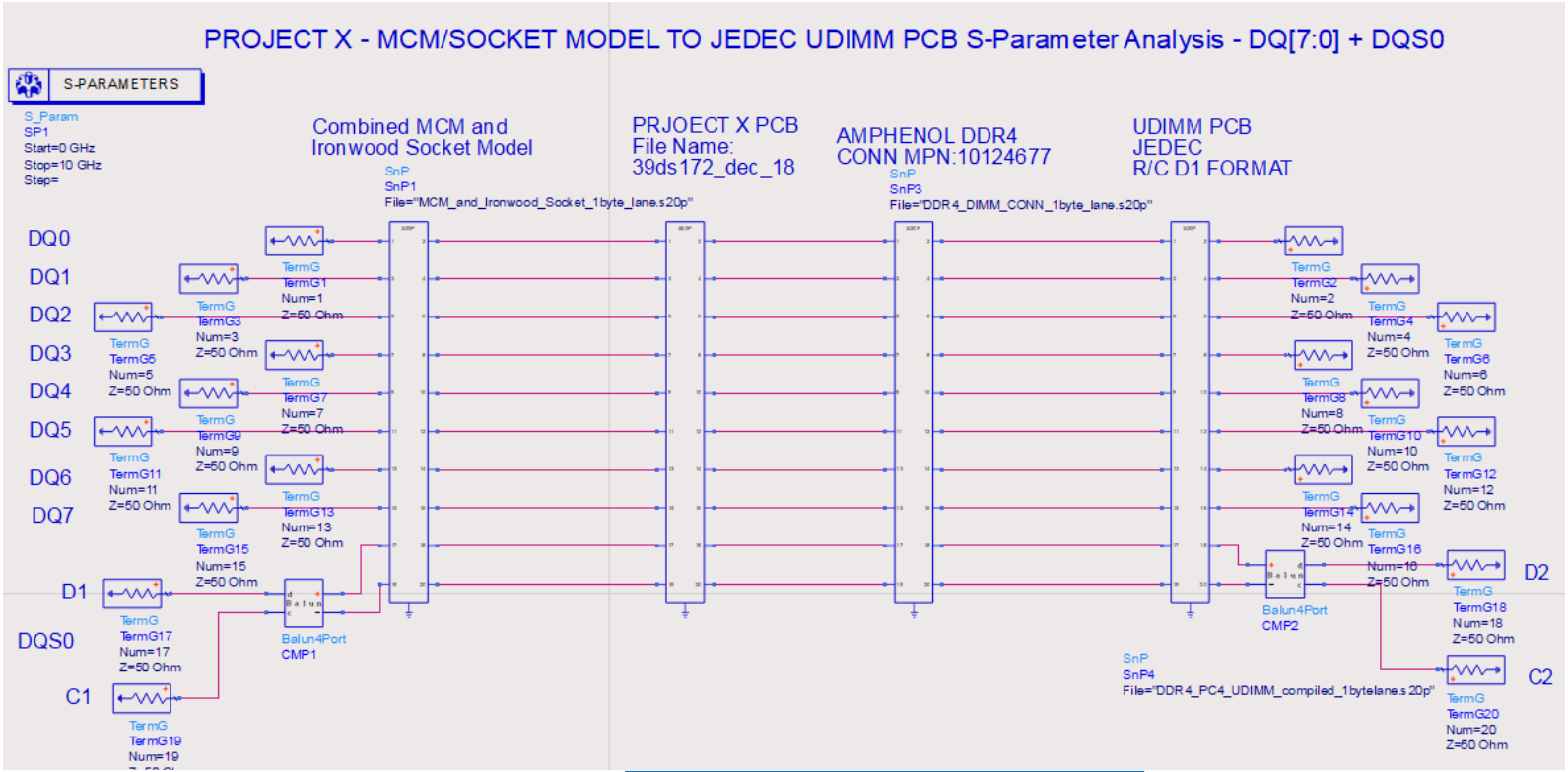
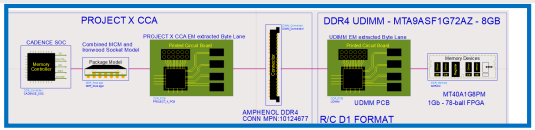
Total Channel S-Parameter Simulation Model – 1 byte Lane - DQ[7:0] + DQS0



Total Channel



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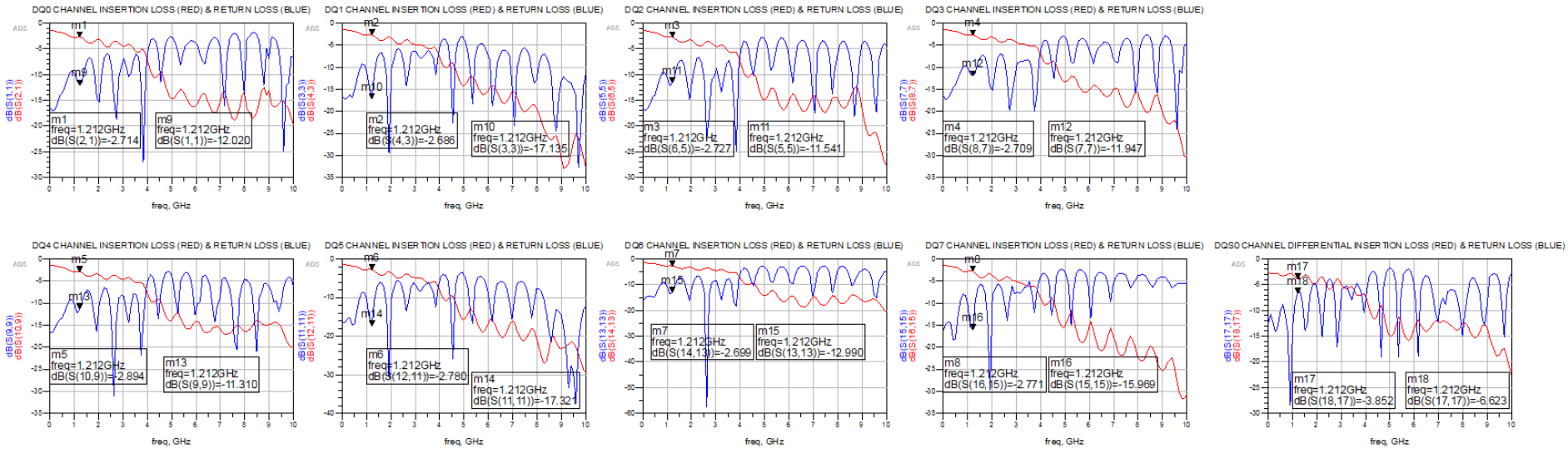
Total Channel S-parameter – 1 byte Lane - DQ[7:0] + DQS0 – Insertion Loss & Return Loss - Results

TOTAL CHANNEL - PROJECT X MCM to UDIMM INSERTION LOSS (RED) and RETURN LOSS (BLUE) - DQ[0:7] + DQS0



*DQ **total** channel insertion loss = ~ (**-2.7 dB**) @ 1.2GHz
*Worst case insertion loss for DQ4 @ (-2.89 dB) @ 1.2GHz
*DQ **total** channel return loss = ~(**-11.5 dB**) @ 1.2GHz
*Worst case return loss for DQ4 @ (-11.3 dB) @ 1.2GHz

*DQS0 **total** channel insertion loss = ~ (**-3.8 dB**) @ 1.2GHz
*DQS0 **total** channel return loss = ~ (**-6.6 dB**) @ 1.2GHz

*Markers shown are placed at DDR4-2400 Nyquist frequency = 1.2GHz

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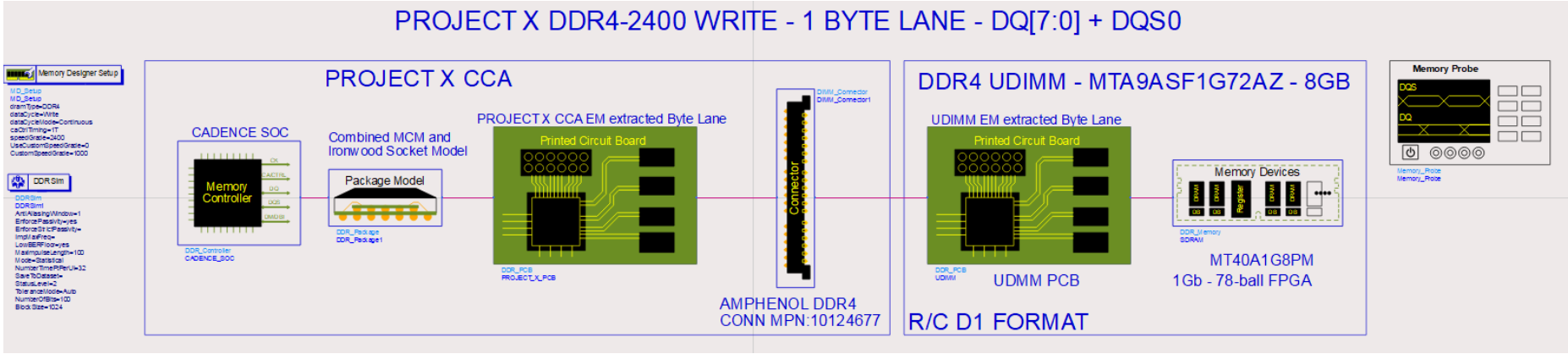
Simulation Model – DDR4-2400 Write – 1 byte Lane – DQ[7:0] + DQS0



PROJECT X CCA with DIMM CONNECTOR

UDIMM

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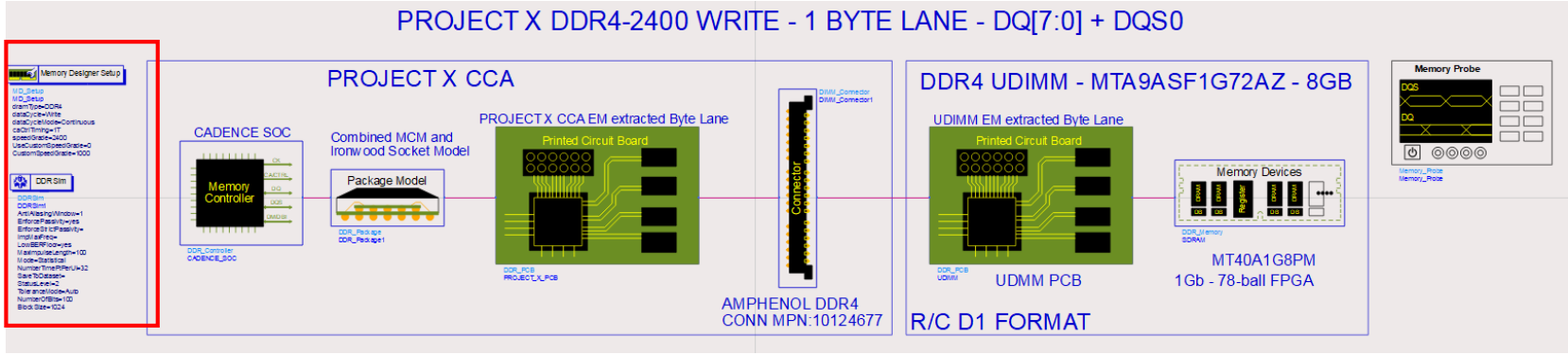
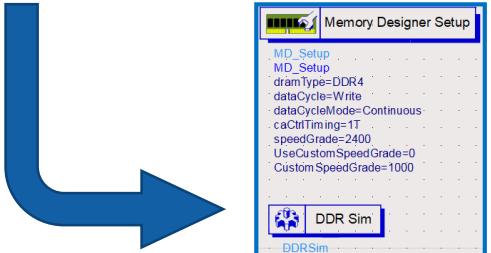
Simulation Model – DDR4-2400 Write – with SIPro EM EXTRACTED MCM Model





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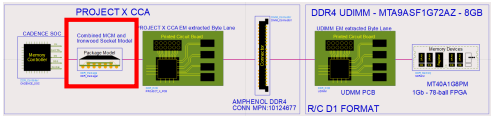
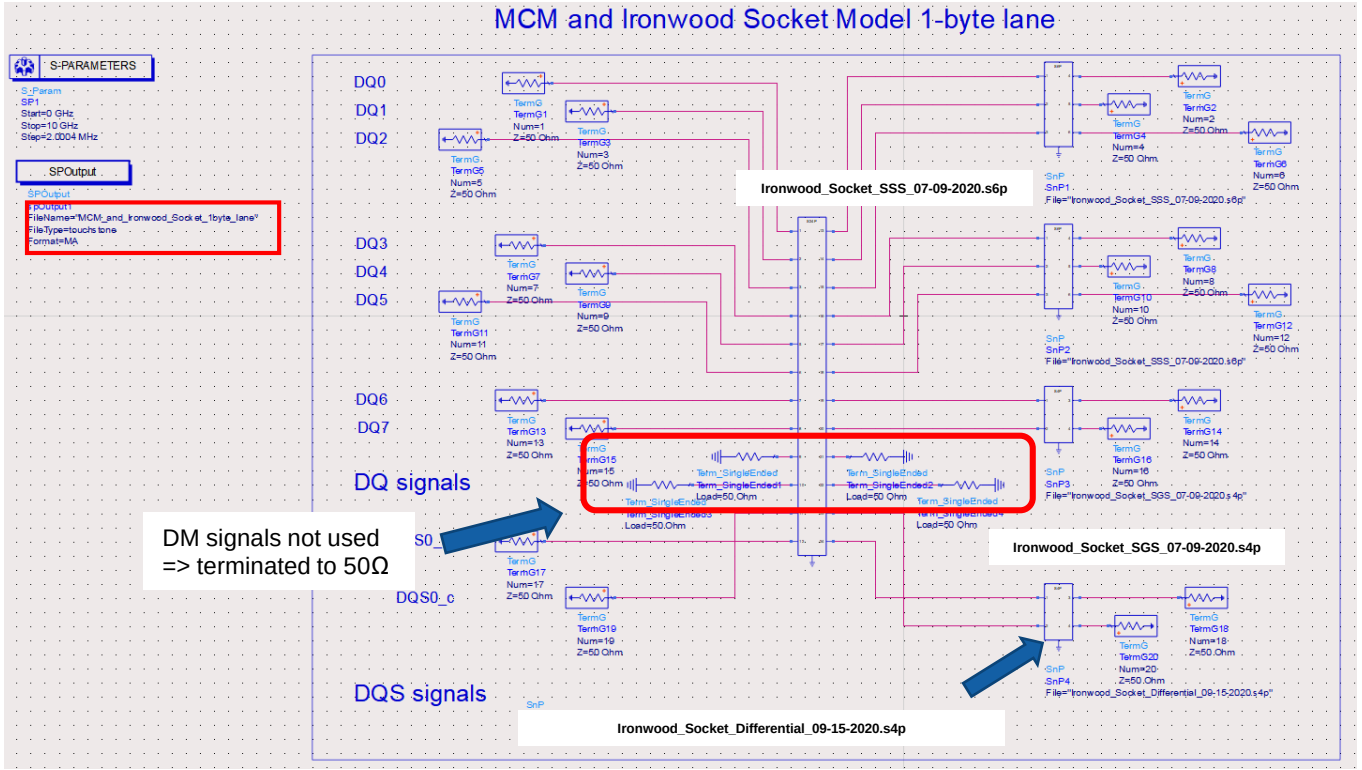
DDR4 MCM + Socket Model – 1 byte lane

MCM_and_Ironwood_Socket_1byte_lane.s20p





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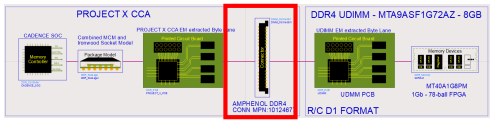
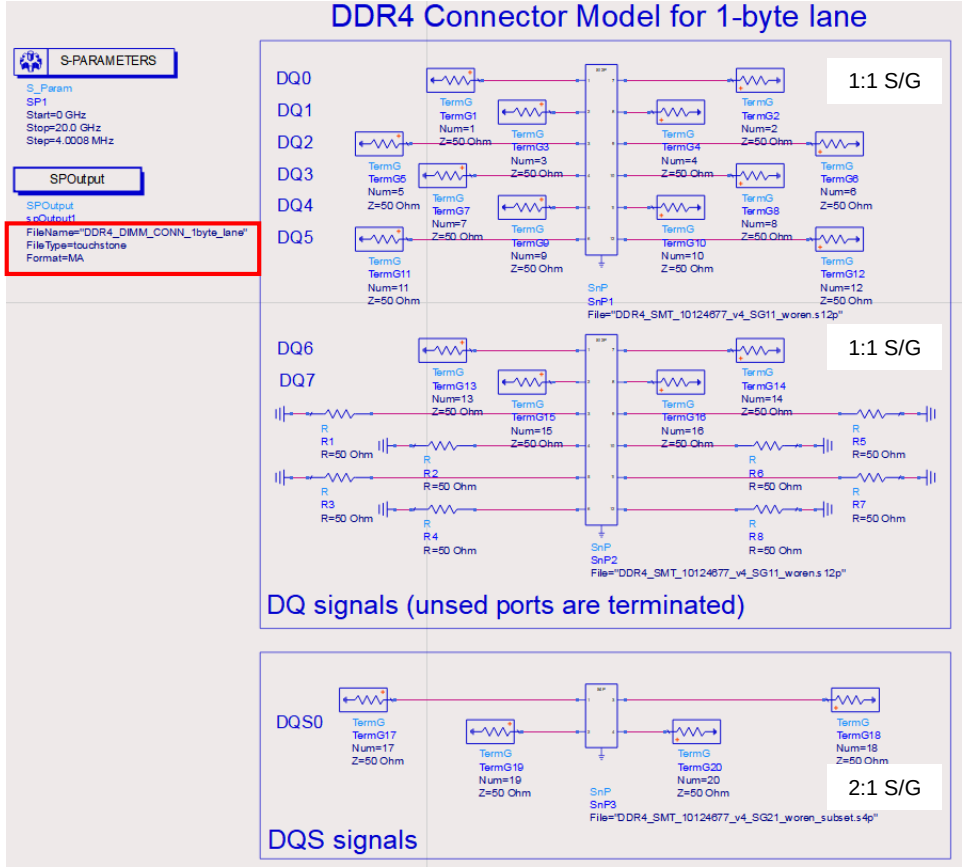
DDR4 DIMM Connector Model – 1 byte lane

DDR4_DIMM_CONN_1byte_lane.s20p





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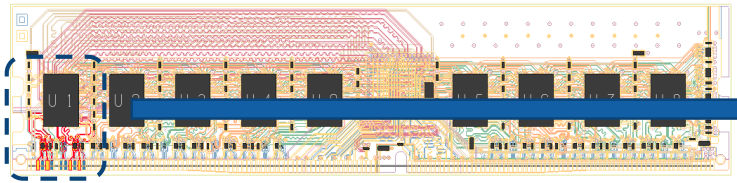
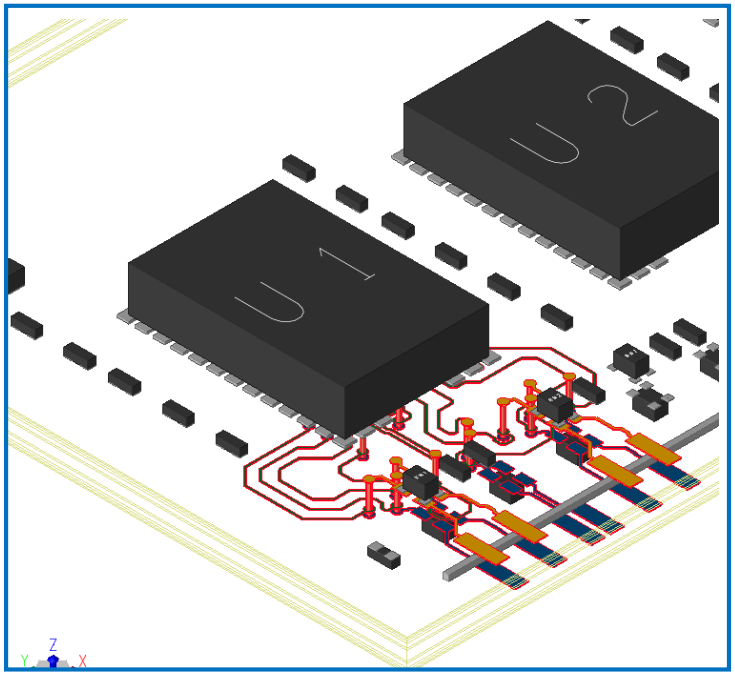
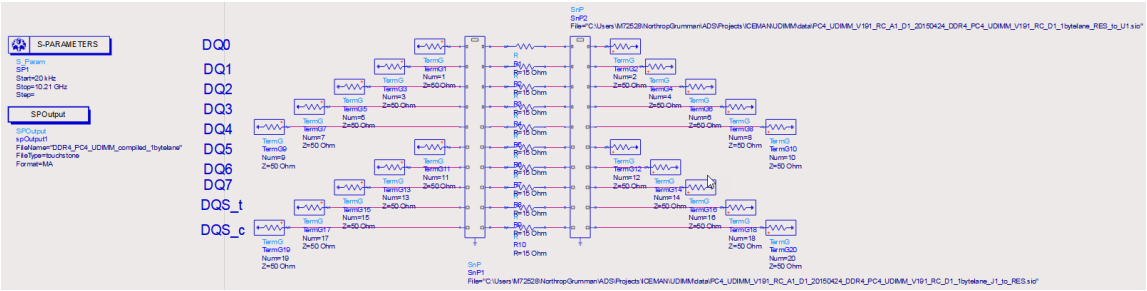
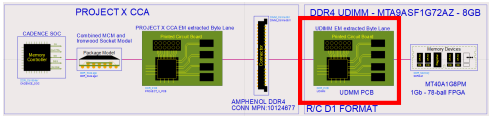
UDIMM EM Extracted Model – 1 byte lane – DQ[7:0] + DQS0







ADS 2020 – prevented complete EM extraction model with in-line component – this is resolved in ADS 2021. => This model consist is two compiled models.



EM Extraction based on UDIMM Layout Data:
PC4-UDIMM_V191_RC_A1_D1_20150424.zip

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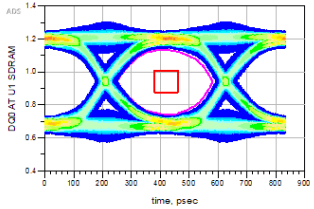
DDR4-2400 Write – DQ[7:0] + DQS0 – Results – No Random Jitter Added

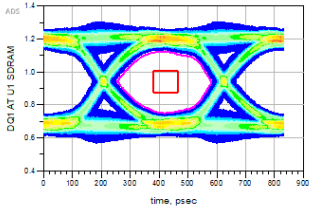
DDR4-2400 WRITE - DQ[0:7] + DQS0
WITH SIPRO EM EXTRACTED MCM MODEL

DQ0



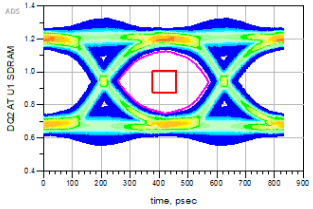
Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.396	WidthAtBER	3.313E-10

DQ1



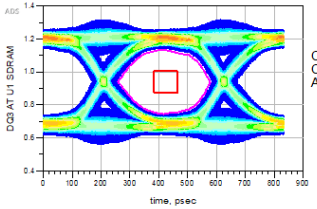
Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.375	WidthAtBER	3.271E-10

DQ2



Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.377	WidthAtBER	3.146E-10

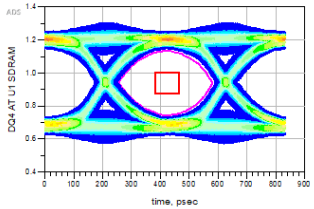
DQ3



Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.389	WidthAtBER	3.229E-10

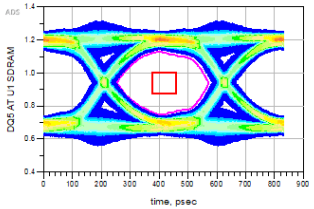
CADENCE SOC IBIS CORNER = MAX
CADENCE SOC DRIVER STRENGTH = 48 OHM
ALL DQ/DQS ODT = 48 OHM

DQ4



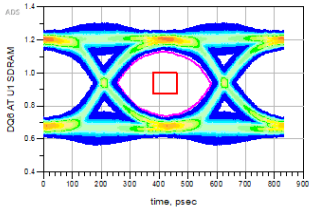
Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.396	WidthAtBER	3.271E-10

DQ5



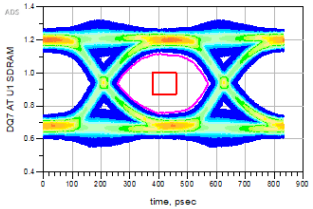
Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.382	WidthAtBER	3.188E-10

DQ6



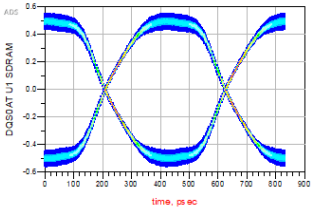
Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.390	WidthAtBER	3.271E-10

DQ7

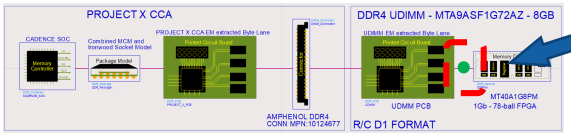


Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.360	WidthAtBER	3.146E-10

DQS0



Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.884	WidthAtBER	4.063E-10



Probe Point

*DQ eye mask shown is for JEDEC DDR4-2400 to achieve BER 1E-16.
*Results shown are for ODT = 48Ω on all DQ signals.

All signals pass Eye mask compliance for DDR4-2400

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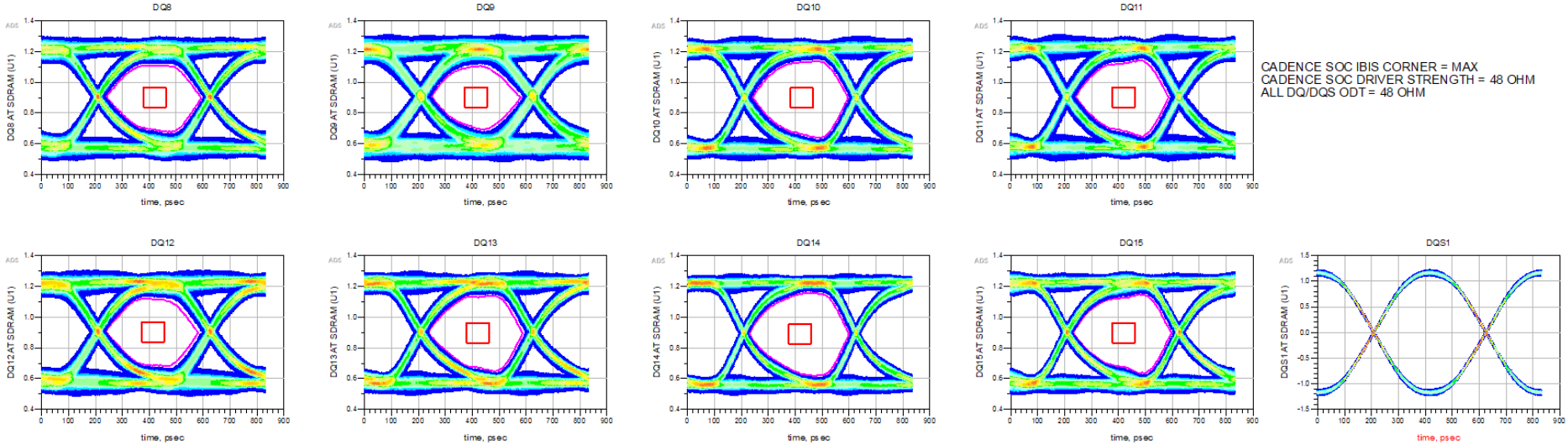
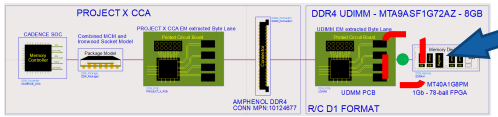
DDR4-2400 Write – DQ[15:8] + DQS1 – Results – No Random Jitter Added

DDR4-2400 WRITE - 1 BYTE LANE - DQ[8:15] + DQS1
WITH SIPRO EM EXTRACTED MCM MODEL





Probe Point

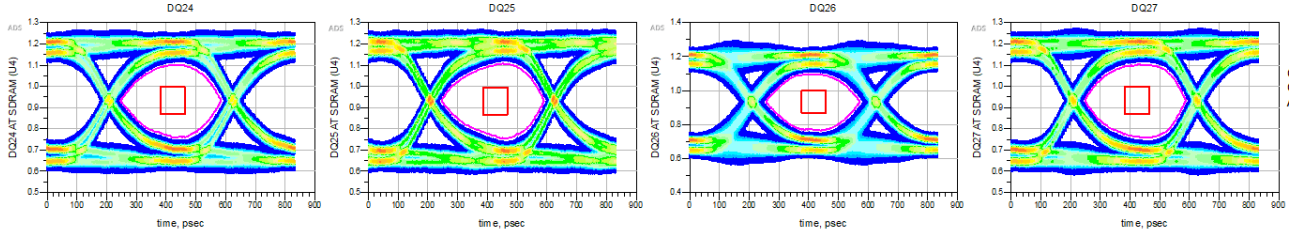
*DQ eye mask shown is for JEDEC DDR4-2400 to achieve BER 1E-16.
EM Extraction based on PROJECT X Layout Data: projectx_39ds172_dec-18.tgz

All signals pass Eye mask compliance for DDR4-2400

NORTHROP GRUMMAN

DDR4-2400 Write – DQ[31:24] + DQS3 – Results – No Random Jitter Added

DDR4-2400 WRITE - 1 BYTE LANE - DQ[24:31] + DQS3
WITH SIPRO EM EXTRACTED MCM MODEL



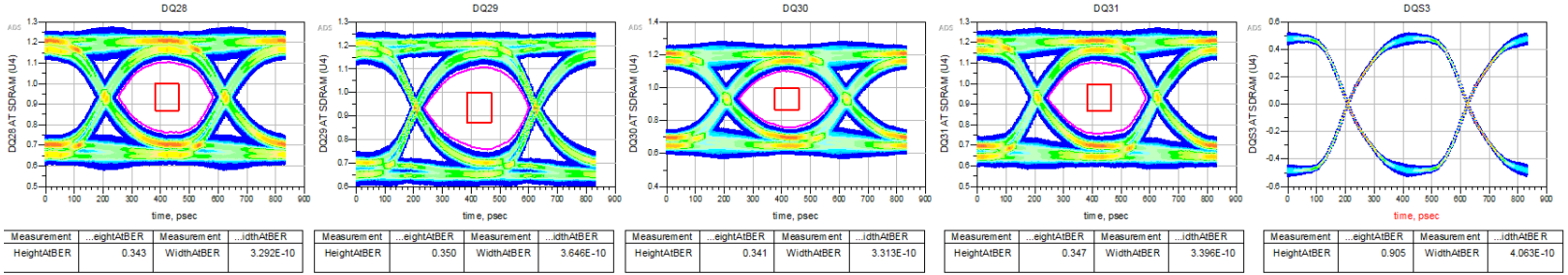
Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.342	WidthAtBER	3.396E-10

Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.353	WidthAtBER	3.458E-10

Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.330	WidthAtBER	3.188E-10

Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.343	WidthAtBER	3.396E-10

CADENCE SOC IBIS CORNER = MAX
CADENCE SOC DRIVER STRENGTH = 48 OHM
ALL DQ/DQS ODT = 48 OHM



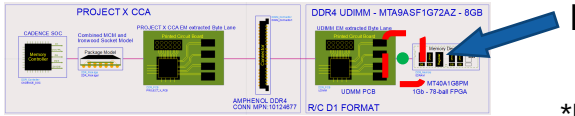
Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.343	WidthAtBER	3.292E-10

Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.350	WidthAtBER	3.646E-10

Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.341	WidthAtBER	3.313E-10

Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.347	WidthAtBER	3.396E-10

Measurement	...eightAtBER	Measurement	...idthAtBER
HeightAtBER	0.905	WidthAtBER	4.063E-10



Probe Point

EM Extraction based on PROJECT X Layout Data: projectx_39ds172_dec-18.tgz

*DQ eye mask shown is for JEDEC DDR4-2400 to achieve BER 1E-16.

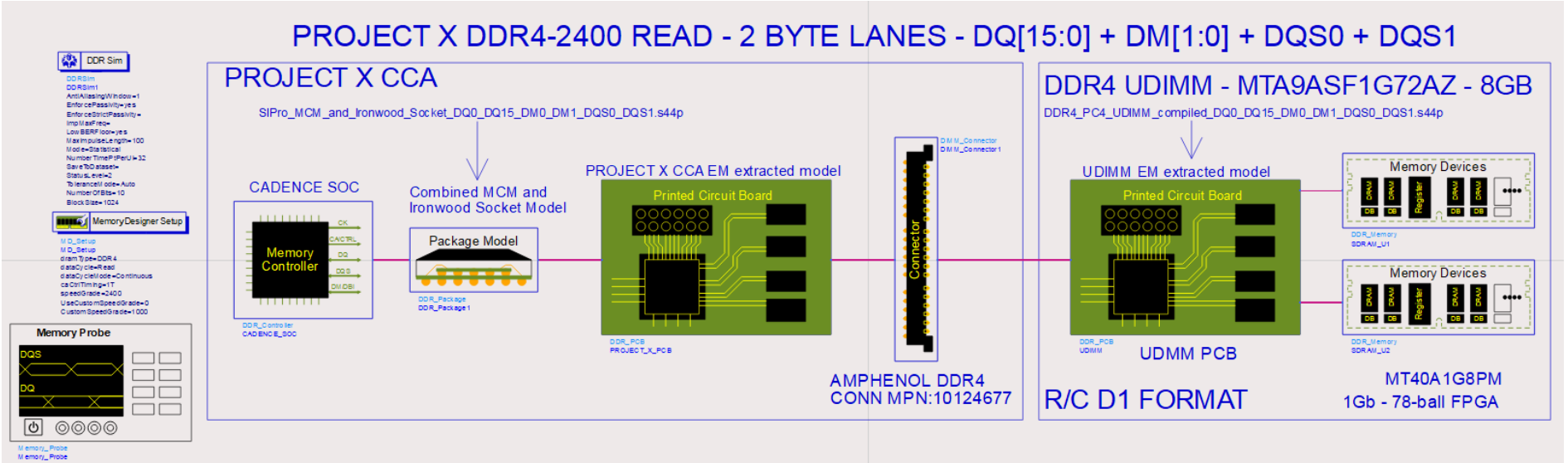
All signals pass Eye mask compliance for DDR4-2400

NORTHROP GRUMMAN

DDR4-2400 DQ[15:0] + DM[1:0] + DQS0 + DQS1 READ AND WRITE ANALYSIS

NORTHROP GRUMMAN

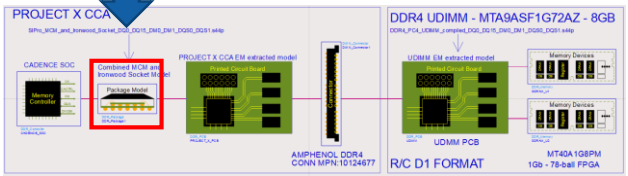
Simulation Model – DDR4-2400 Write/Read – DQ[15:0] + DM[1:0] + DQS0 + DQS1



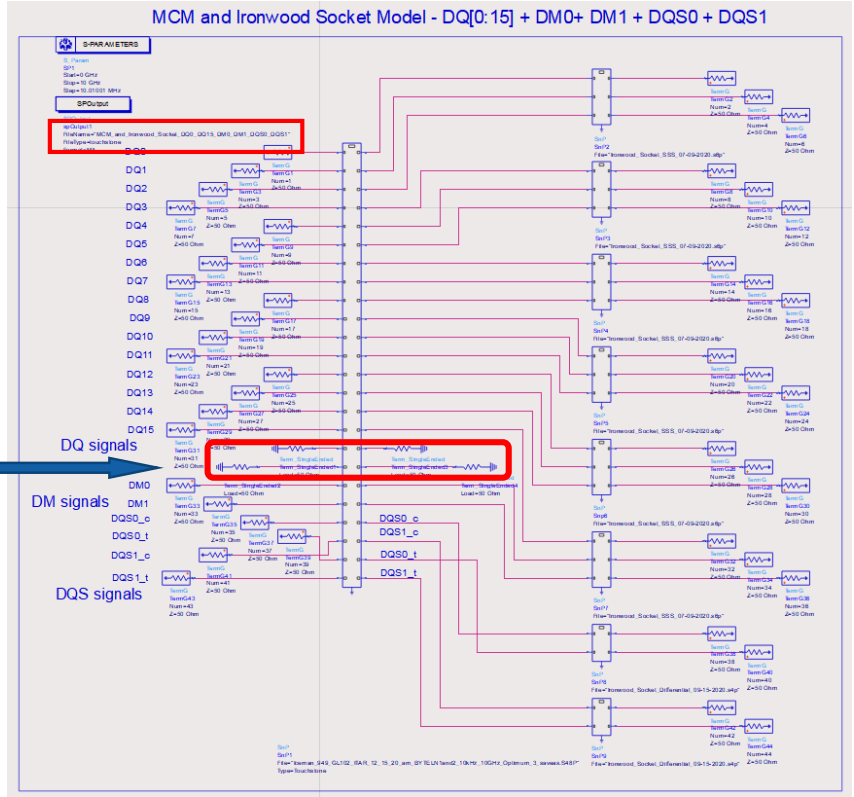
NORTHROP GRUMMAN

DDR4 MCM + Socket Model – DQ[15:0]+DM0+DM1+DQS0+DQS1

MCM_and_Ironwood_Socket_DQ0_DQ15_DM0_DM1_DQS0_DQS1.s44p



DM_Nx signals not used
=> terminated to 50Ω



Ironwood_Socket_SSS_07-09-2020.s6p

Ironwood_Socket_SSS_07-09-2020.s6p

Ironwood_Socket_SSS_07-09-2020.s6p

Ironwood_Socket_SSS_07-09-2020.s6p

Ironwood_Socket_SSS_07-09-2020.s6p

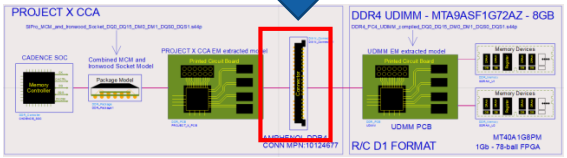
Ironwood_Socket_Differential_09-15-2020.s4p

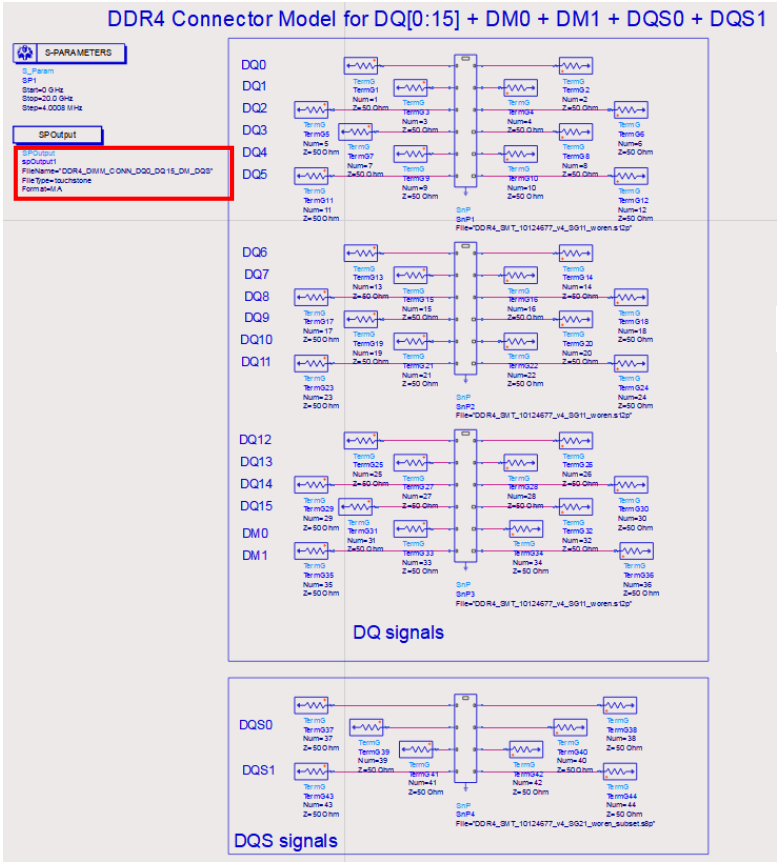
Ironwood_Socket_Differential_09-15-2020.s4p

NORTHROP GRUMMAN

DDR4 DIMM Connector Model – DQ[15:0] + DM[1:0] + DQS0 + DQS1

DDR4_DIMM_CONN_DQ0_DQ15_DM_DQS.s44p





1:1 S/G

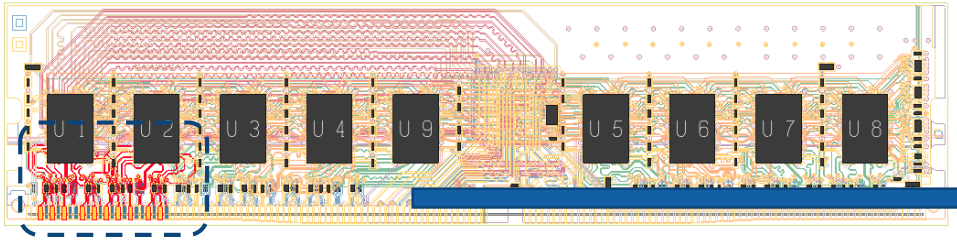
1:1 S/G

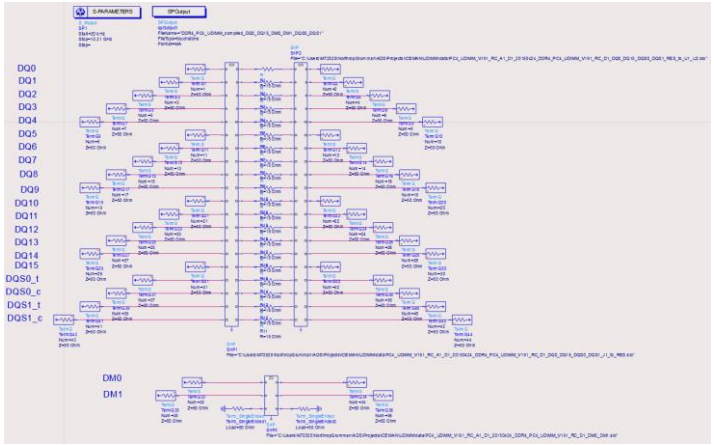
1:1 S/G

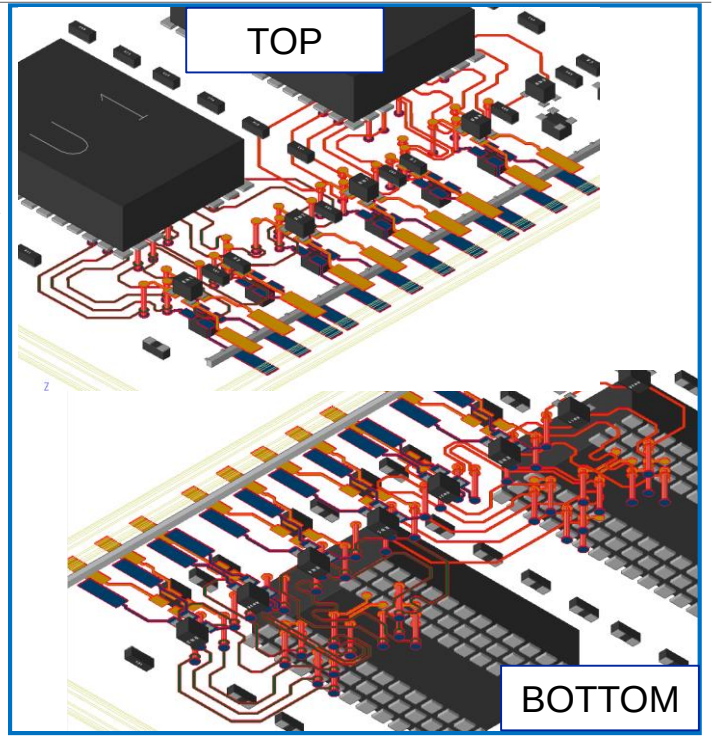
2:1 S/G

NORTHROP GRUMMAN

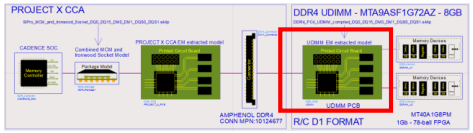
UDIMM EM Extracted Model – DQ[15:0]+DM0+DM1+DQS0+DQS1







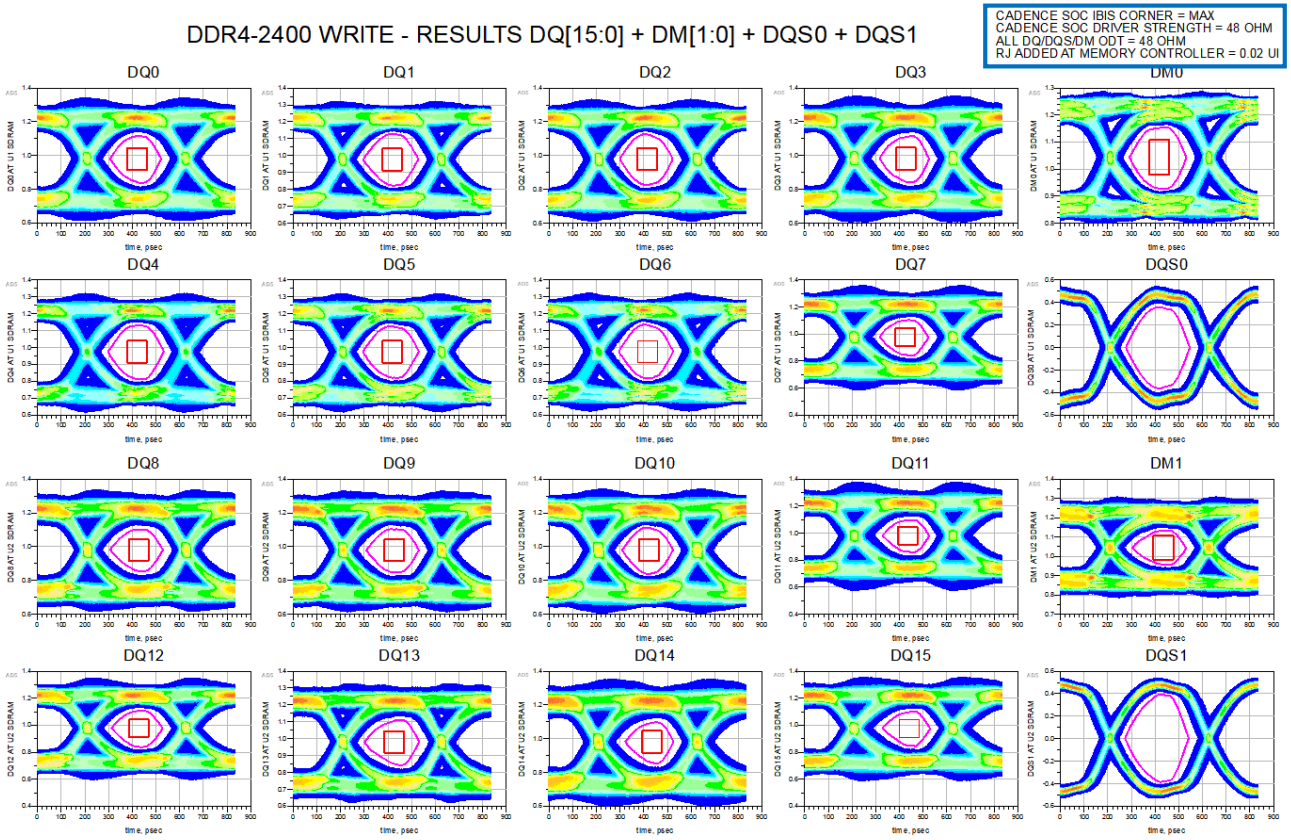
ADS 2020 – prevented complete EM extraction model with in-line component – this is resolved in ADS 2021. => This model consist is two compiled models.



EM Extraction based on UDIMM Layout Data:
PC4-UDIMM_V191_RC_A1_D1_20150424.zip

NORTHROP GRUMMAN

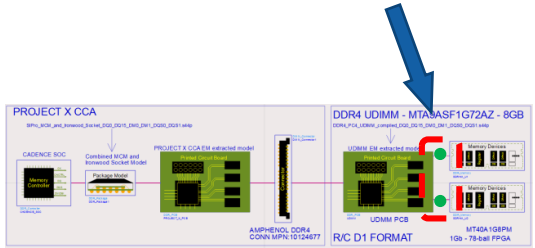
DDR4-2400 Write – 2 byte lane Results – DQ[15:0] + DM[1:0] + DQS0 + DQS1



Sim settings

*Includes 2% Random Jitter injected at Memory Controller

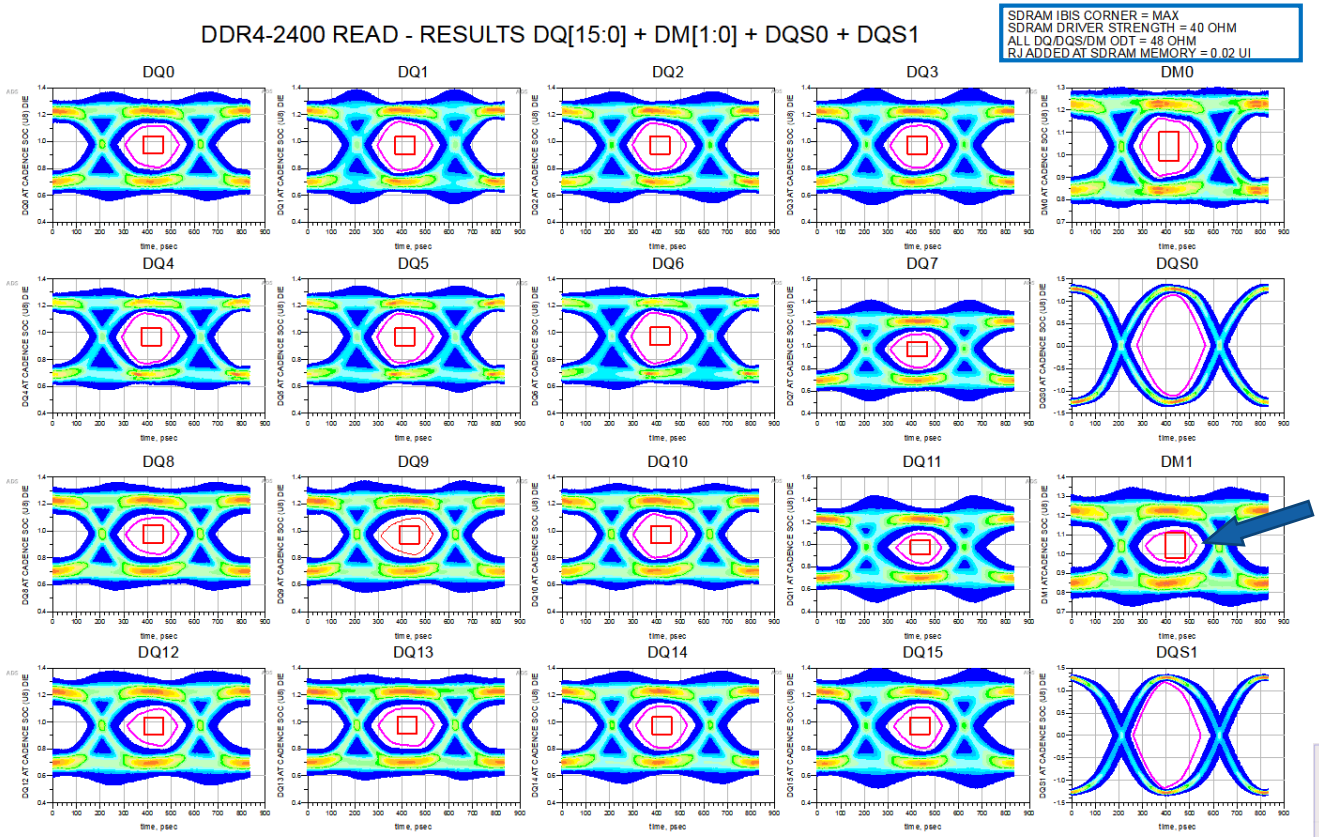
Probe Point



DQ [15:0] + DM[1:0] ALL PASSED BER @ DDR4-2400

NORTHROP GRUMMAN

DDR4-2400 Read – 2 byte lane Results – DQ[15:0] + DM[1:0] + DQS0 + DQS1

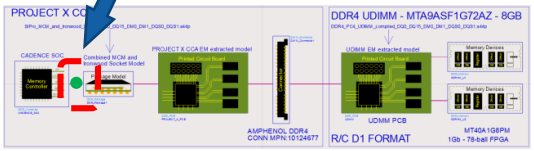


Sim settings

*Includes 2% Random Jitter injected at Memory

BER is passing Eye Mask

Probe Point



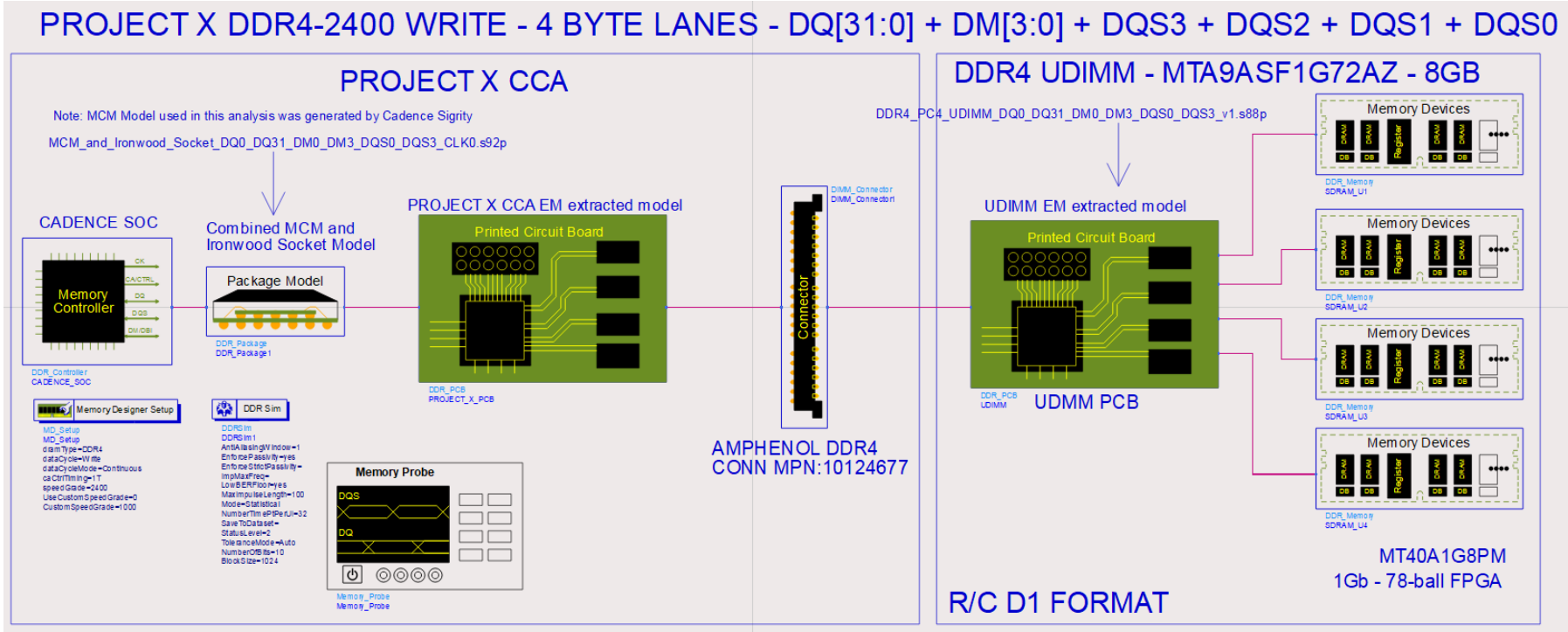
DQ [15:0] + DM[1:0] ALL PASSED BER @ DDR4-2400

NORTHROP GRUMMAN

DDR4-2400 Write DQ[31:0] + DM[3:0] +DQS[3:0] Results

NORTHROP GRUMMAN

Simulation Model – DDR4-2400 Write – DQ[31:0] + DM[3:0] + DQS[3:0]



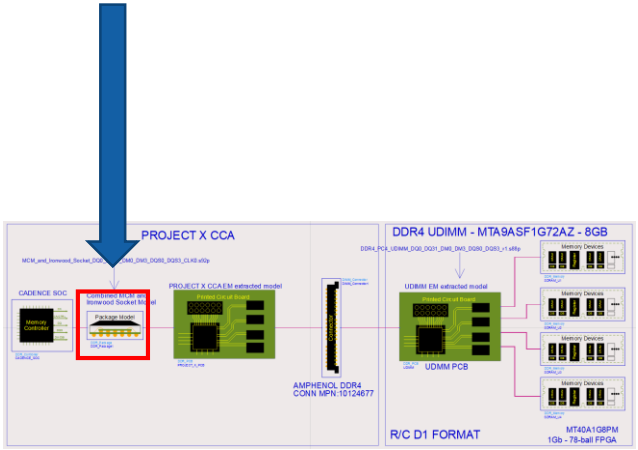
NORTHROP GRUMMAN

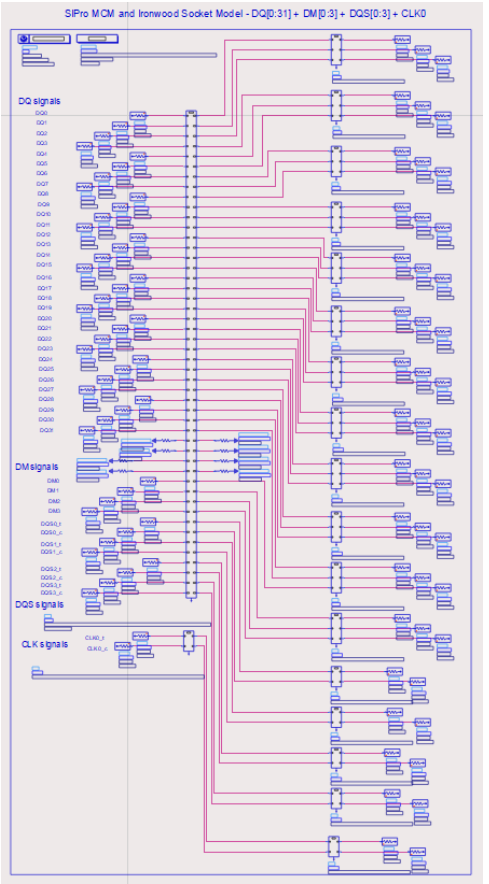
DDR4 MCM + Socket Model – 4 byte lanes

Due to memory limitation on local machine in SIPro, a single 4 byte lane MCM model was not able to be extracted.

=> Cadence Sigrity MCM extracted model was used for MCM in the combined MCM + Socket model

MCM_and_Ironwood_Socket_DQ0_DQ31_DM0_DM3_DQS0_DQS3_CLK0.s92p

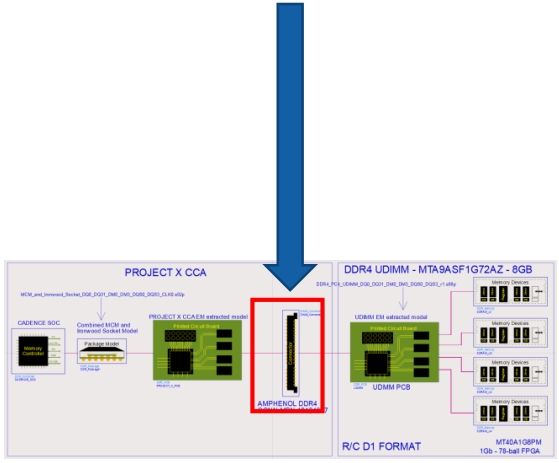


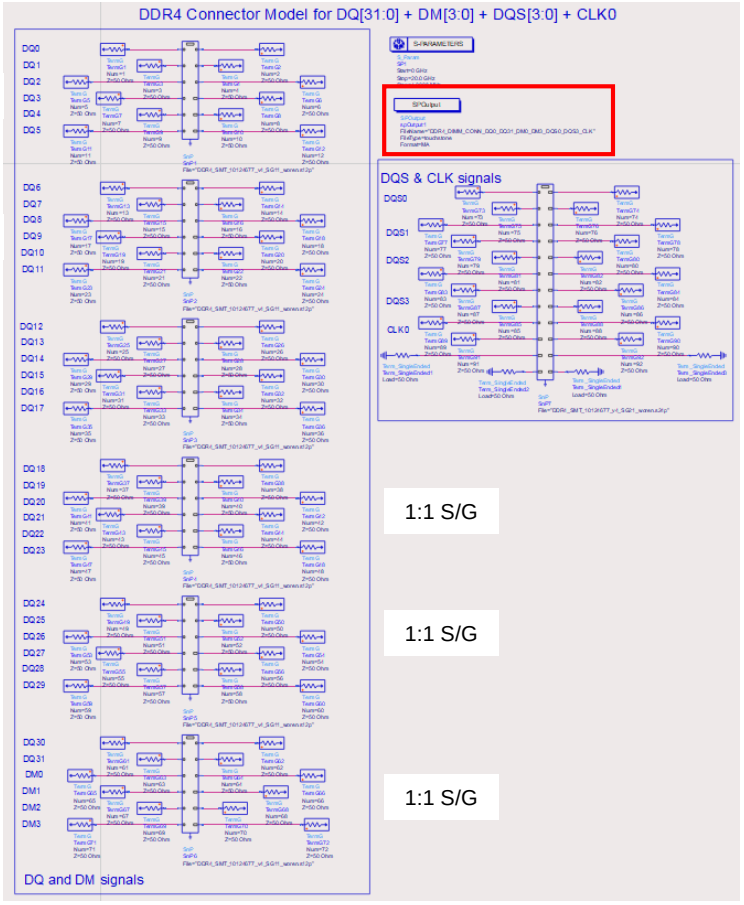


NORTHROP GRUMMAN

DDR4 DIMM Connector Model – DQ[31:0] + DM[3:0] + DQS[3:0]

DDR4_DIMM_CONN_DQ0_DQ31_DM0_DM3_DQS0_DQS3_CLK.s92p





1:1 S/G

1:1 S/G

2:1 S/G

1:1 S/G

1:1 S/G

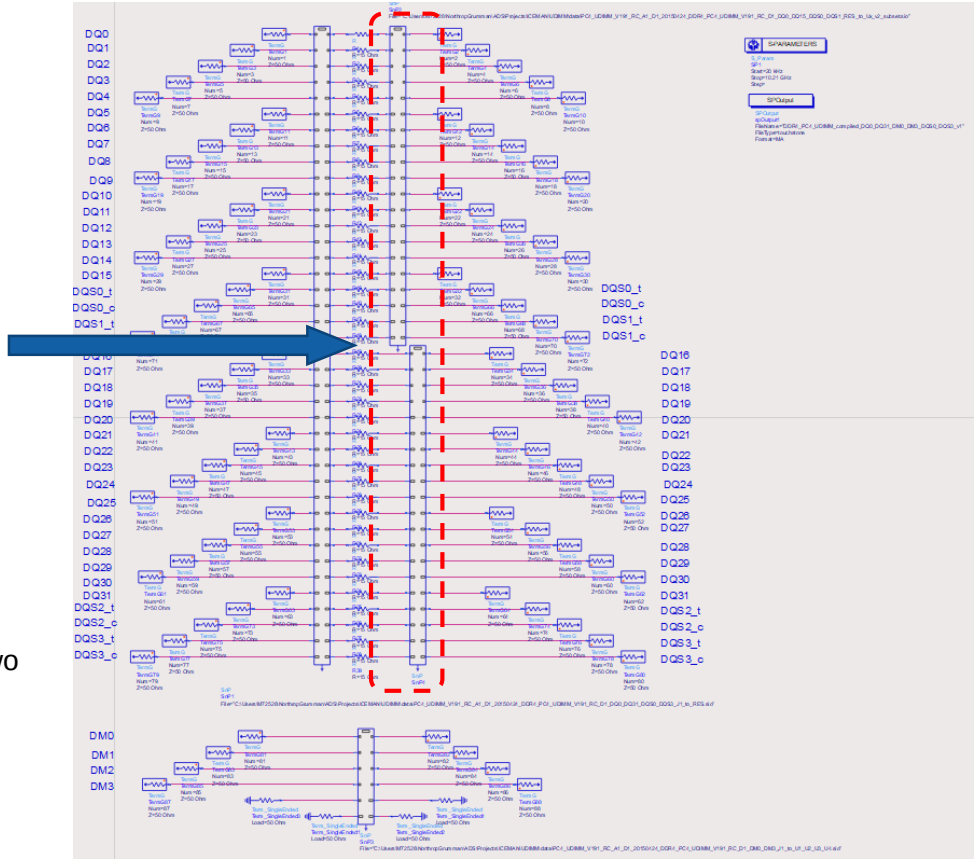
1:1 S/G

NORTHROP GRUMMAN

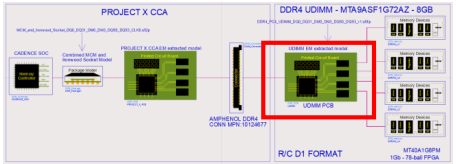
UDIMM EM Extracted Model – DQ[31:0] + DM[3:0] + DQS[3:0]

EM Extraction based on UDIMM Layout Data:
PC4-UDIMM_V191_RC_A1_D1_20150424.zip

In SIPro, EM extraction would output incorrect results for random DQ nets. The solution was to break up the extraction from 4 byte lanes into 2 byte lanes. This could have been a convergence issue in SIPro with ADS 2020U1.

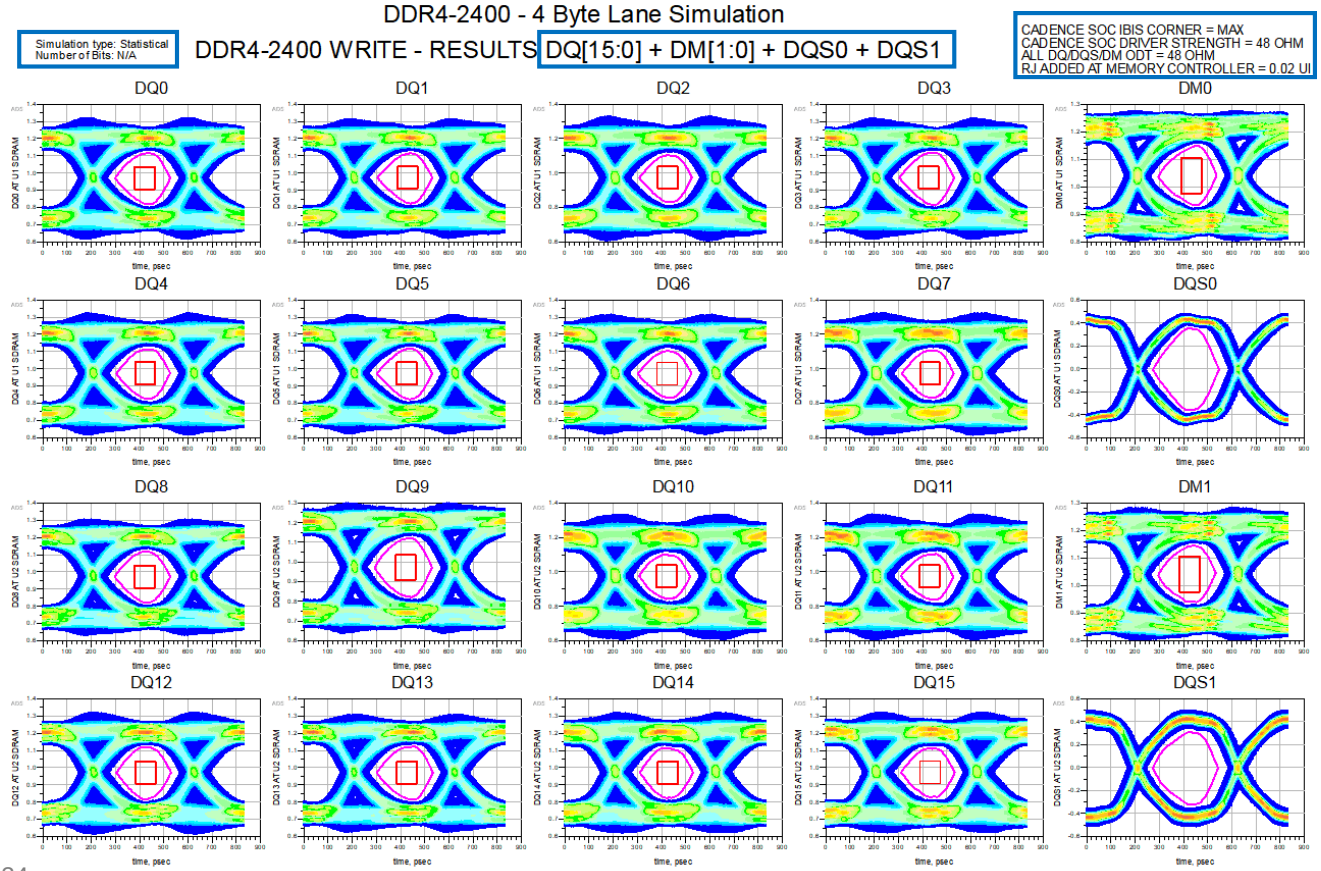


*ADS 2020 – prevented complete EM extraction model with in-line component – this is resolved in ADS 2021. => This model consist is two compiled models.



NORTHROP GRUMMAN

DDR4-2400 Write – 4 byte lane Results – DQ[31:0] + DM[3:0] + DQS[3:0]

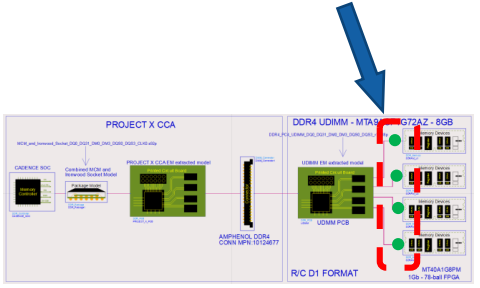


Sim settings

*Includes 2% Random Jitter injected at Memory Controller

DQ [15:0] + DM[1:0] ALL PASSED BER @ DDR4-2400

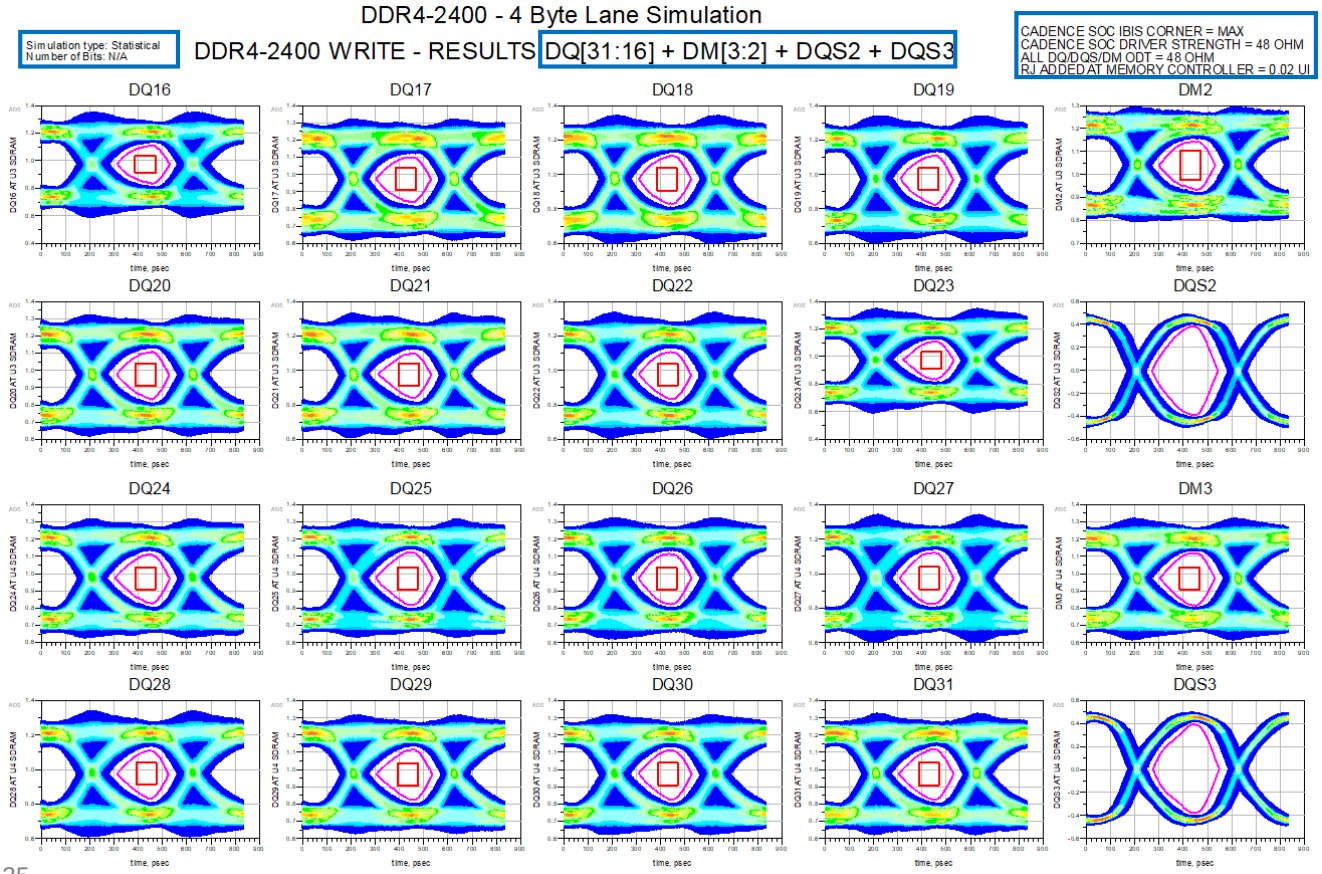
Probe Point



Note: Results shown are for MCM model which was generated by Cadence Sigrity

NORTHROP GRUMMAN

DDR4-2400 Write – 4 byte lane Results – DQ[31:0] + DM[3:0] + DQS[3:0]



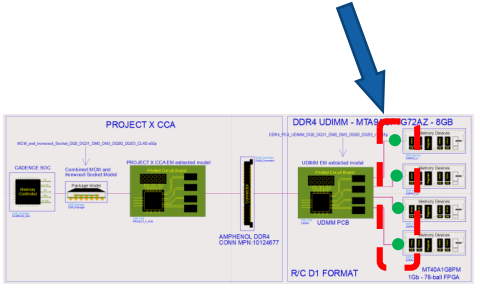
CADENCE SOC IBIS CORNER = MAX
CADENCE SOC DRIVER STRENGTH = 48 OHM
ALL DQ/DQS/DM ODT = 48 OHM
RJ ADDED AT MEMORY CONTROLLER = 0.02 UI

Sim settings

*Includes 2% Random Jitter injected at Memory Controller

DQ [31:16] + DM[3:2] ALL PASSED BER @ DDR4-2400

Probe Point



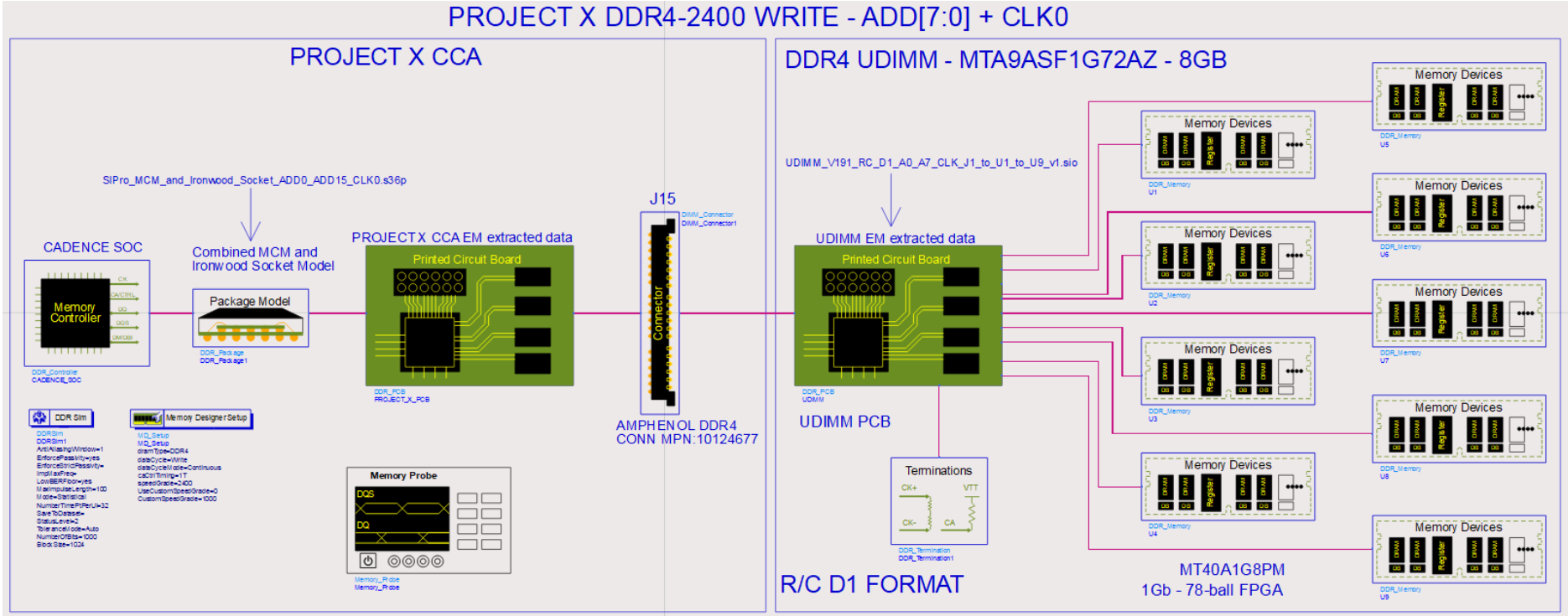
Note: Results shown are for MCM model which was generated by Cadence Sigrity

NORTHROP GRUMMAN

DDR4-2400 Write ADD[7:0] + CLK0 Results with UDIMM (R/C D1)

NORTHROP GRUMMAN

Simulation Model – DDR4-2400 Write – ADD[7:0] + CLK0



NORTHROP GRUMMAN

DDR4 Memory Controller Package Delay Settings - ADD[7:0] + CLK0

Select IBIS/ EBD File C:/Users/M72528/NorthropGrumman/ADS/Projects/[redacted]_DDR4_wrk/data/gf_12lp_ddr4_EDITED_1v2.ibs Browse... View...

Component DDR4

Assign signal property by: IBIS Signal Name ☐ Enable Channel ID Matching ☑ Collapse Power Node

☐ Use Delay File Browse... View...

Enable DBI ○ DBIdc ○ DBIac ◉ None

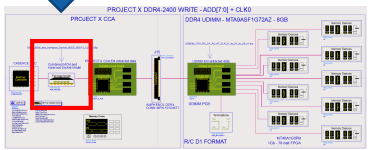
Assign Signal Property and Enable Pins for Simulation

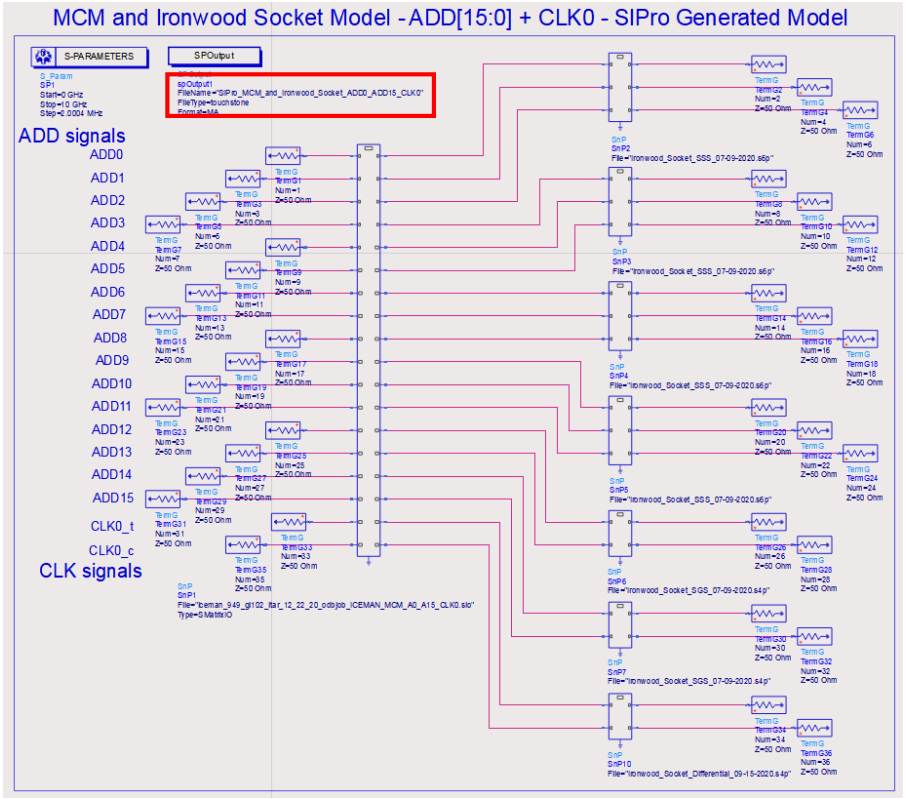
Reference Designator and IBIS Table			Signal Property Table				
Search	Search	Search	Search	Search	Y	Search	Search
Ref Des	IBIS Pin Name	IBIS Signal Name	Signal Type	Signal Index	Simulate	Delay (sec)	Channel ID
U8_ADS_DIE	48	ADD0	A	0	Y	115e-12	0
U8_ADS_DIE	49	ADD1	A	1	Y	96e-12	0
U8_ADS_DIE	50	ADD2	A	2	Y	105.6e-12	0
U8_ADS_DIE	51	ADD3	A	3	Y	100.7e-12	0
U8_ADS_DIE	52	ADD4	A	4	Y	111.6e-12	0
U8_ADS_DIE	53	ADD5	A	5	Y	118.8e-12	0
U8_ADS_DIE	54	ADD6	A	6	Y	122.6e-12	0
U8_ADS_DIE	55	ADD7	A	7	Y	124.4e-12	0
U8_ADS_DIE	65	CLKN0	CK_c	0	Y	99.6e-12	0
U8_ADS_DIE	64	CLKP0	CK_t	0	Y	98.9e-12	0

NORTHROP GRUMMAN

DDR4 MCM + Socket Model – ADD[15:0] + CLK0

SIPro_MCM_and_Ironwood_Socket_ADD0_ADD15_CLK0.s36p





Ironwood_Socket_SSS_07-09-2020.s6p

Ironwood_Socket_SSS_07-09-2020.s6p

Ironwood_Socket_SSS_07-09-2020.s6p

Ironwood_Socket_SSS_07-09-2020.s6p

Ironwood_Socket_SSS_07-09-2020.s6p

Ironwood_Socket_SGS_07-09-2020.s4p

Ironwood_Socket_SGS_07-09-2020.s4p

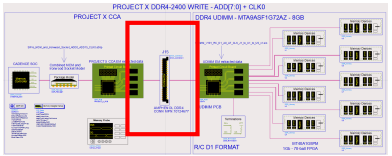
Ironwood_Socket_Differential_09-15-2020.s4p

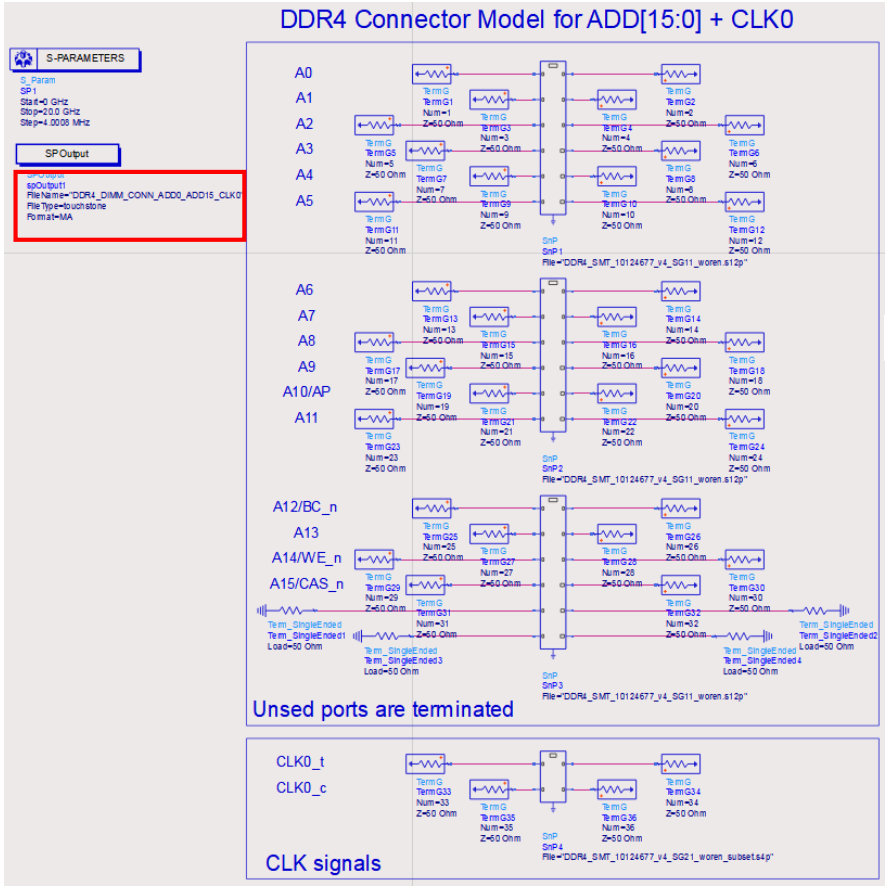
MCM Model: **projectX_MCM_A0_A15_CLK0.sio**

NORTHROP GRUMMAN

DDR4 DIMM Connector Model – ADD[15:0] + CLK0

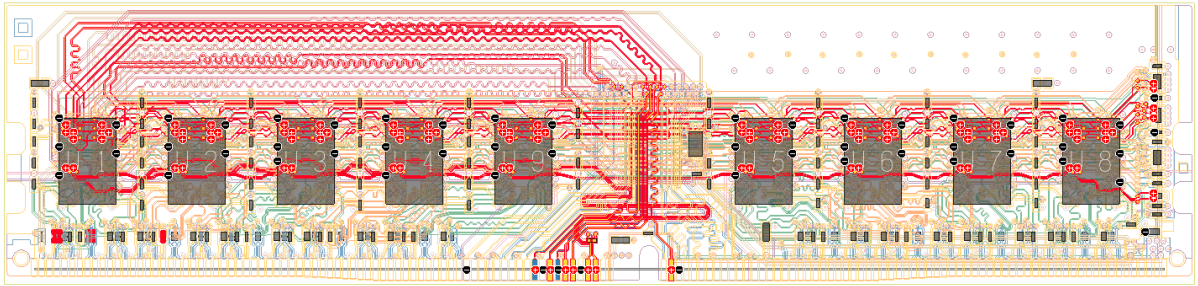
DDR4_DIMM_CONN_ADD0_ADD15_CLK0.s36p





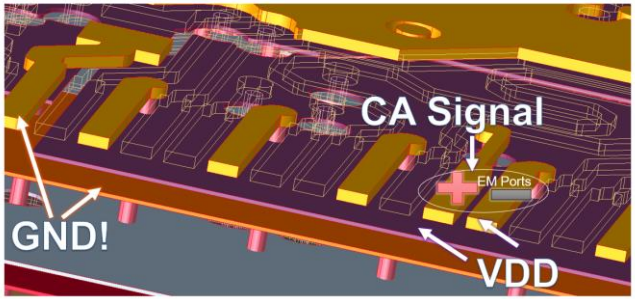
NORTHROP GRUMMAN

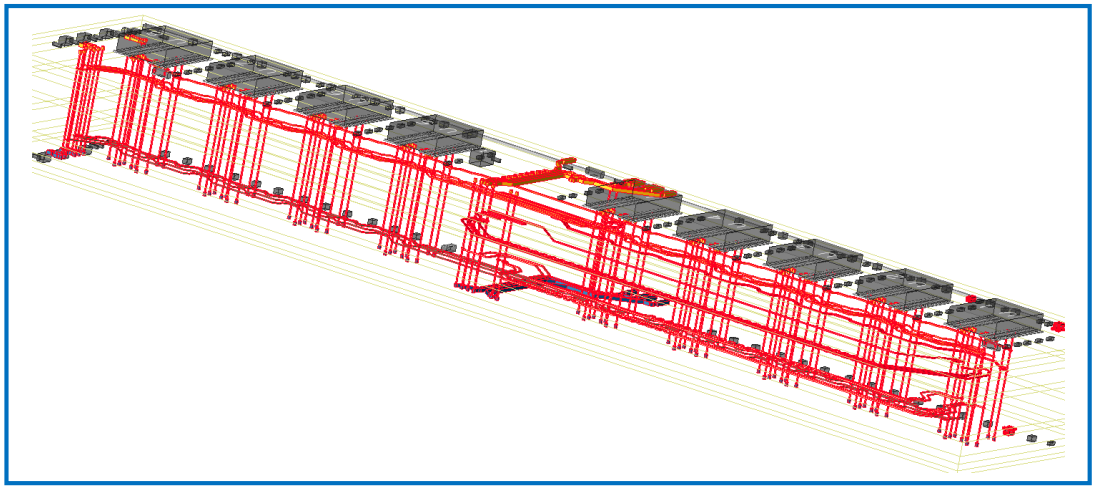
UDIMM EM Extracted Model – ADD[7:0] + CLK0

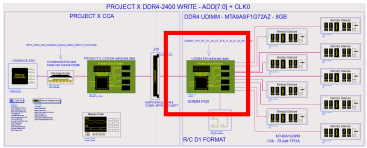


**Important Note: All CAC nets & CLK0 had return port set to VDD on UDIMM.

DDR4 Command Address Signals Reference VDD not GND!



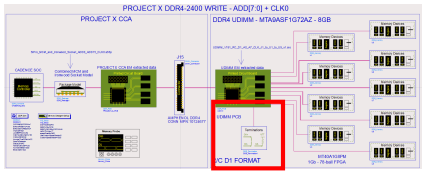




EM Extraction based on UDIMM Layout Data: PC4-UDIMM_V191_RC_A1_D1_20150424.zip

NORTHROP GRUMMAN

DDR4 ADD & CLK Termination Settings – ADD[7:0] + CLK0



Edit DDR Termination Parameters:5

ads_simulation:DDR_Termination Instance Name

DDR_Termination1

Termination for CA and Control Signals

VTT (Volts) 0.6 | R_CA (Ohms) 39.0 | Rs_Control (Ohms) 39.0

Termination for Clock Signals

- Termination Topology 1
  - R_CK_diff (Ohms) 75
- Termination Topology 2
  - R_CK_SE (Ohms) 50.0 | VTT_CK (Volts) 1.0
- Termination Topology 3 (selected)
  - R_CK_SE (Ohms) 39.0 | C_CK (pFs) 10 | VTT_CK (Volts) 0.6

Search	Search	Search	Search	Search	y
Port Name	Ref Des	Signal Type	Signal Index	Channel ID	Simulate
CLK0_B_RN47	RN47	CK_c	0	0	Y
CLK0_RN47	RN47	CK_t	0	0	Y
A7_RN51	RN51	A	7	0	Y
A6_RN49	RN49	A	6	0	Y
A5_RN53	RN53	A	5	0	Y
A4_RN53	RN53	A	4	0	Y
A3_RN53	RN53	A	3	0	Y
A2_RN51	RN51	A	2	0	Y
A1_RN49	RN49	A	1	0	Y
A0_RN49	RN49	A	0	0	Y

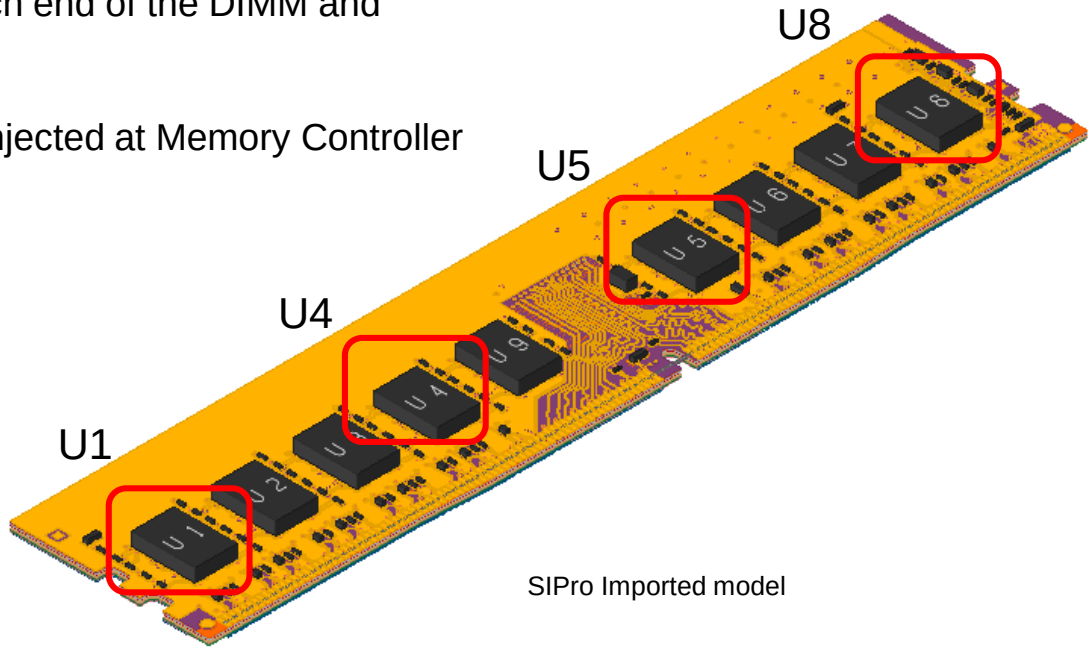
< Back | Next > | Finish | Cancel | Help

NORTHROP GRUMMAN

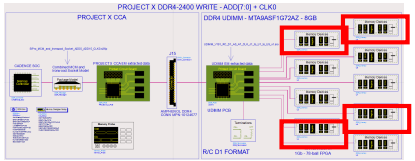
ADDRESS Signal SI Analysis on UDIMM

MICRON UDIMM MPN: MTA9ASF1G72AZ – 8GB
288-pin UDIMM (MO-309 R/C D1)

- Analysis shown will only include analysis at the following SDRAMs at the UDIMM for A[7:0] + CLK0 due to fly-by topology on UDIMM for CAC nets
  - This allows analysis to be done at each end of the DIMM and middle points on DIMM
- Results shown include 2% Random Jitter injected at Memory Controller with BER = 1E-16



SIPro Imported model



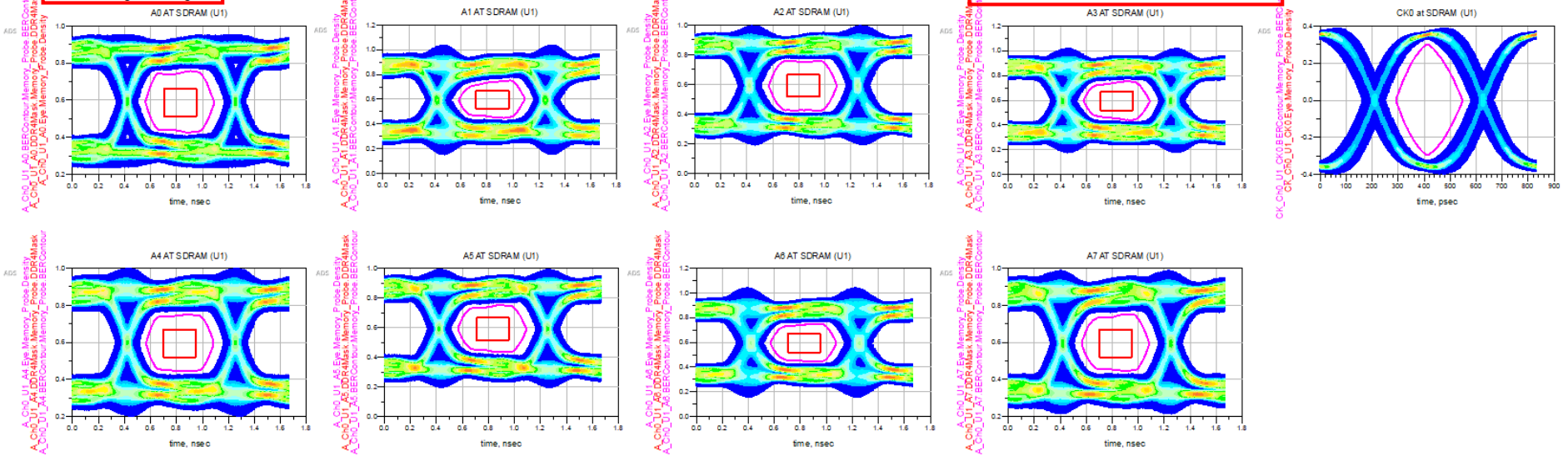
NORTHROP GRUMMAN

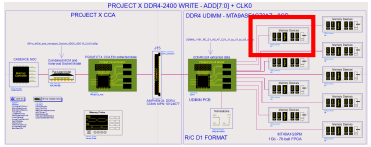
Results DDR4-2400 ADD[7:0] at SDRAM (U1) on UDIMM – TYP IBIS Corner

Simulation type: Statistical
Number of Bits: NA
CaCtrl Timing: 1T Timing

DDR4-2400 WRITE - ADD[7:0] AT SDRAM (U1)

CADENCE SOC IBIS CORNER = TYP
CADENCE SOC DRIVER STRENGTH = 40 OHM
RJ ADDED AT MEMORY CONTROLLER = 0.02 UI





A[7:0] ALL PASSED BER @ DDR4-2400

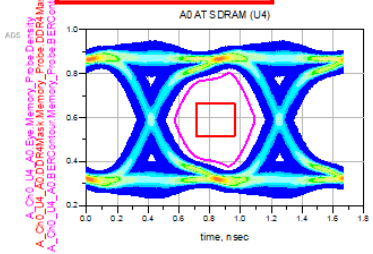
NORTHROP GRUMMAN

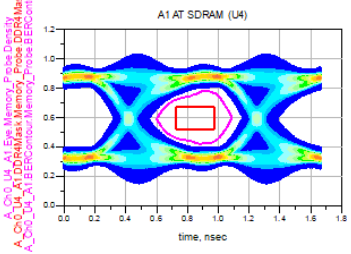
Results DDR4-2400 ADD[7:0] at SDRAM (U4) on UDIMM – TYP IBIS Corner

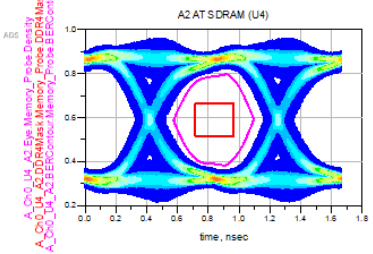
Simulation type: Statistical
Number of Bits: NA
CaCtrl Timing: 1T Timing

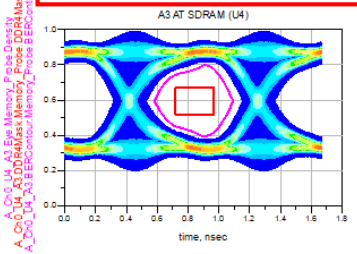
DDR4-2400 WRITE - ADD[7:0] AT SDRAM (U4)

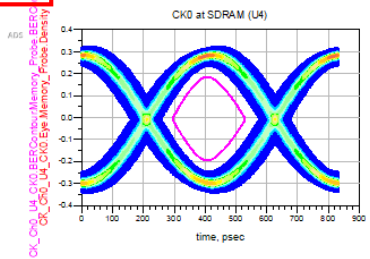
CADENCE SOC IBIS CORNER = TYP
CADENCE SOC DRIVER STRENGTH = 40 OHM
RJ ADDED AT MEMORY CONTROLLER = 0.02 UI

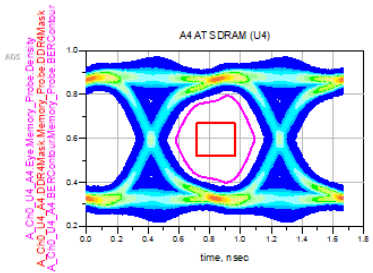


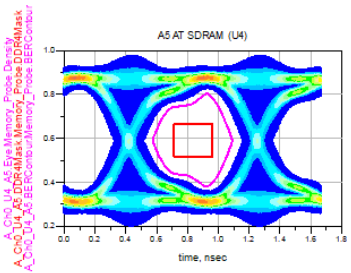


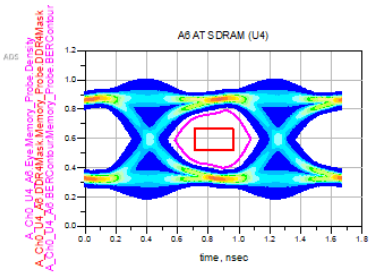


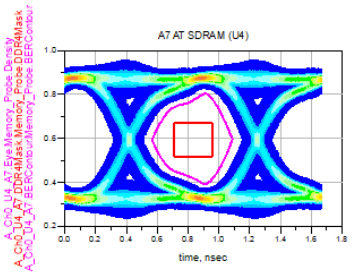


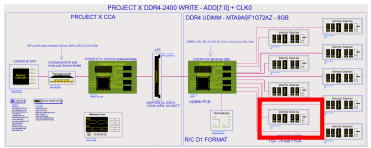












A[7:0] ALL PASSED BER @ DDR4-2400

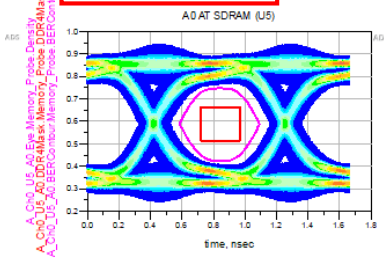
NORTHROP GRUMMAN

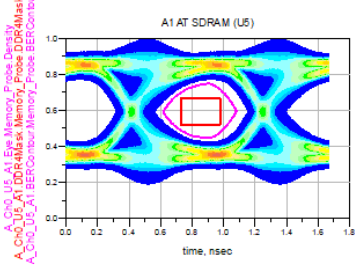
Results DDR4-2400 ADD[7:0] at SDRAM (U5) on UDIMM – TYP IBIS Corner

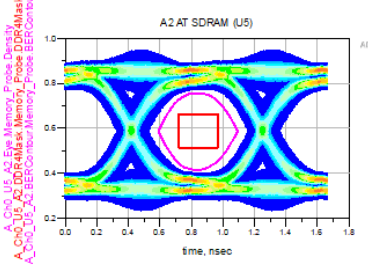
Simulation type: Statistical
Number of Bits: NA
CaCtrl Timing: 1T Timing

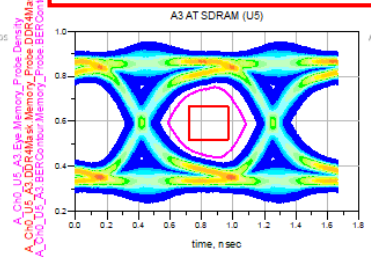
DDR4-2400 WRITE - ADD[7:0] AT SDRAM (U5)

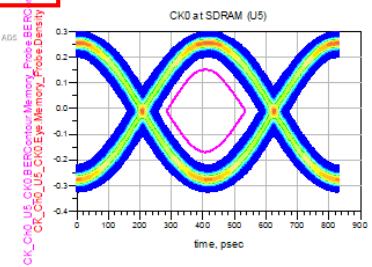
CADENCE SOC IBIS CORNER = TYP
CADENCE SOC DRIVER STRENGTH = 40 OHM
RJ ADDED AT MEMORY CONTROLLER = 0.02 UI

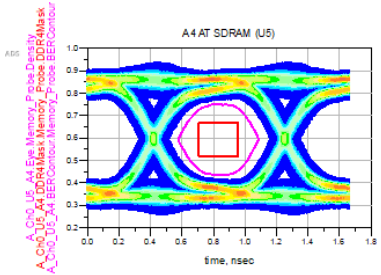


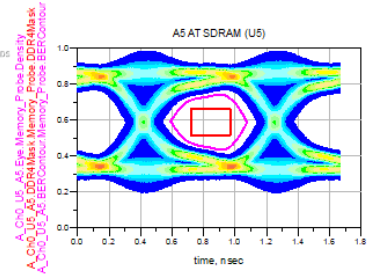


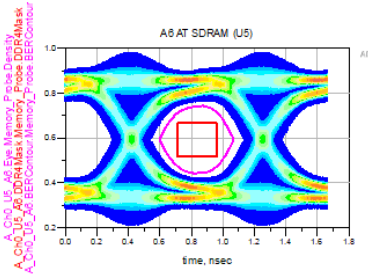


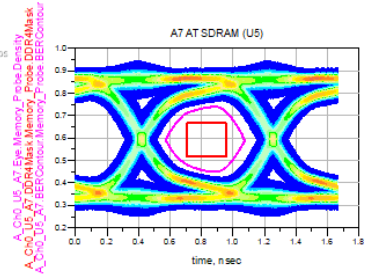


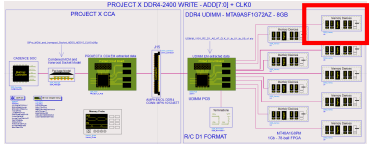












A[7:0] ALL PASSED BER @ DDR4-2400

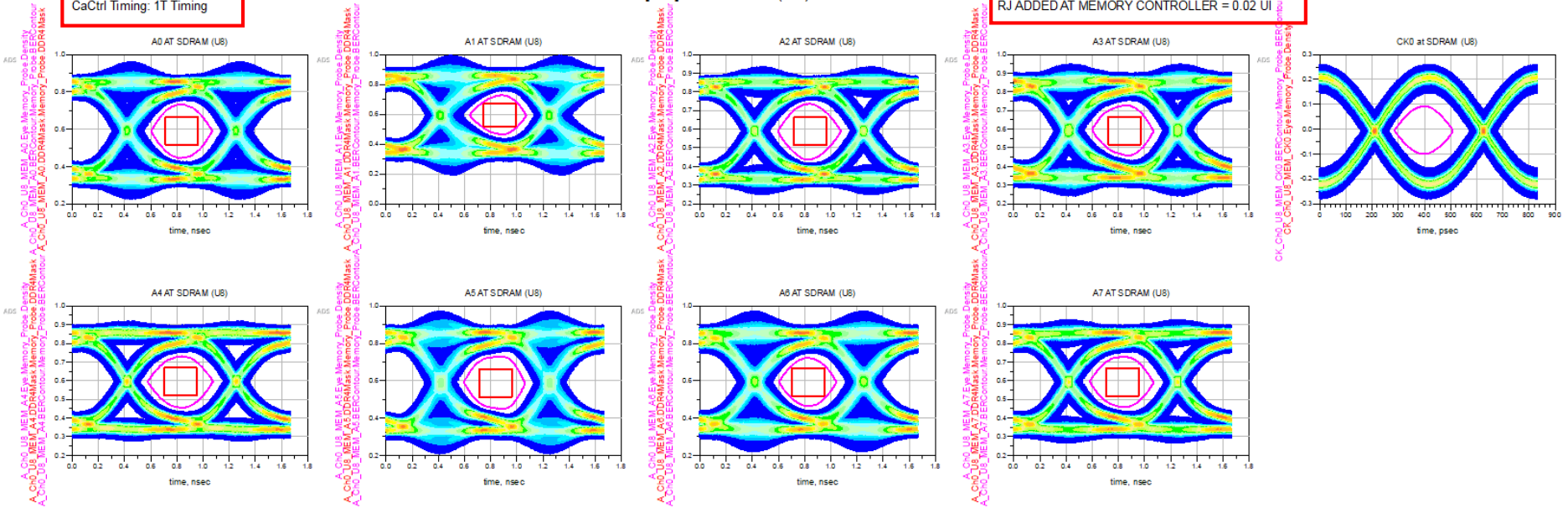
NORTHROP GRUMMAN

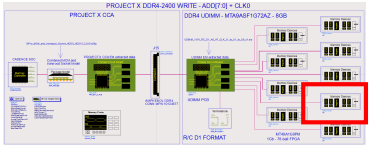
Results DDR4-2400 ADD[7:0] at SDRAM (U8) on UDIMM – TYP IBIS Corner

Simulation type: Statistical
Number of Bits: NA
CaCtrl Timing: 1T Timing

DDR4-2400 WRITE - ADD[7:0] AT SDRAM (U8)

CADENCE SOC IBIS CORNER = TYP
CADENCE SOC DRIVER STRENGTH = 40 OHM
RJ ADDED AT MEMORY CONTROLLER = 0.02 UI





A[7:0] ALL PASSED BER @ DDR4-2400

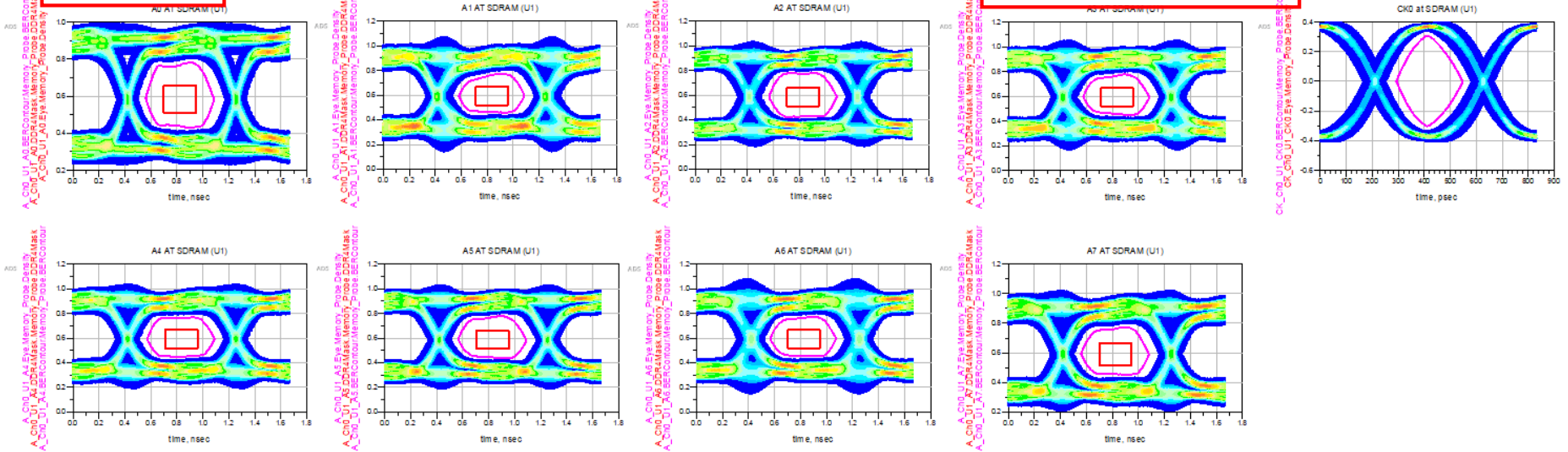
NORTHROP GRUMMAN

Results DDR4-2400 ADD[7:0] at SDRAM (U1) on UDIMM – FAST IBIS Corner

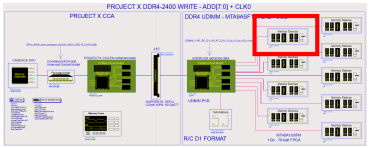
Simulation type: Statistical
Number of Bits: NA
CaCtrl Timing: 1T Timing

DDR4-2400 WRITE - ADD[7:0] AT SDRAM (U1)

CADENCE SOC IBIS CORNER = FAST
CADENCE SOC DRIVER STRENGTH = 40 OHM
RJ ADDED AT MEMORY CONTROLLER = 0.02 UI

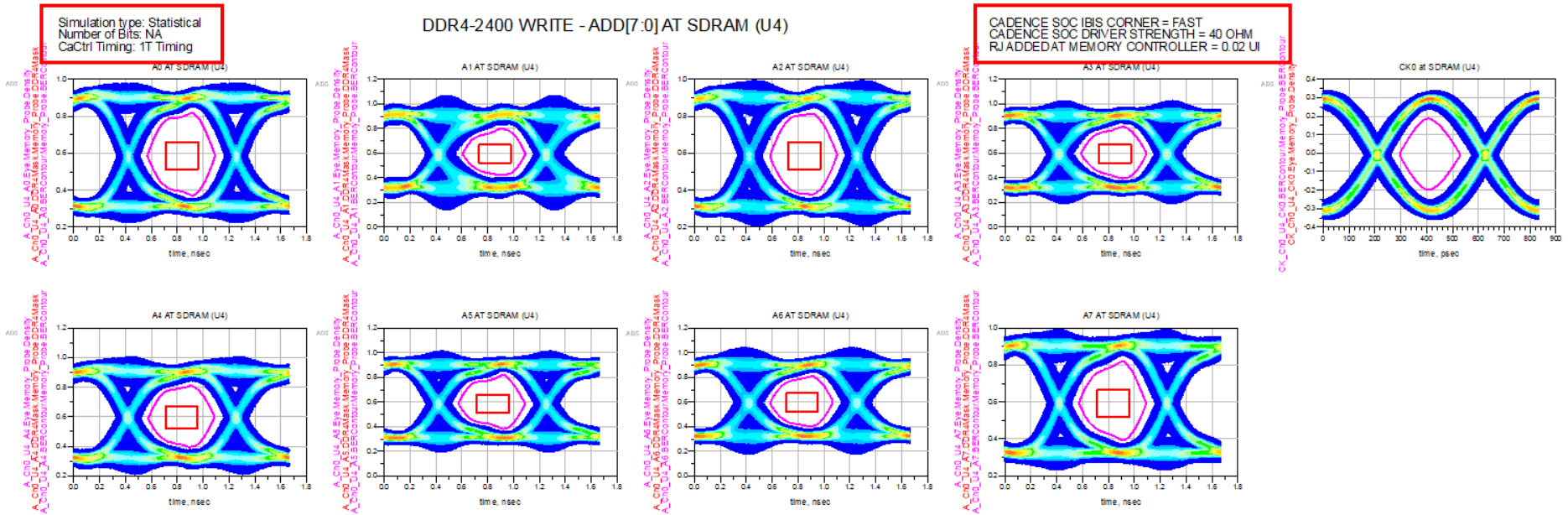


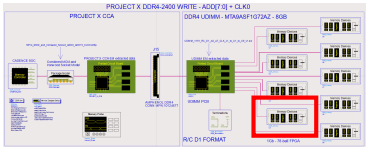
A[7:0] ALL PASSED BER @ DDR4-2400



NORTHROP GRUMMAN

Results DDR4-2400 ADD[7:0] at SDRAM (U4) on UDIMM – FAST IBIS Corner





A[7:0] ALL PASSED BER @ DDR4-2400

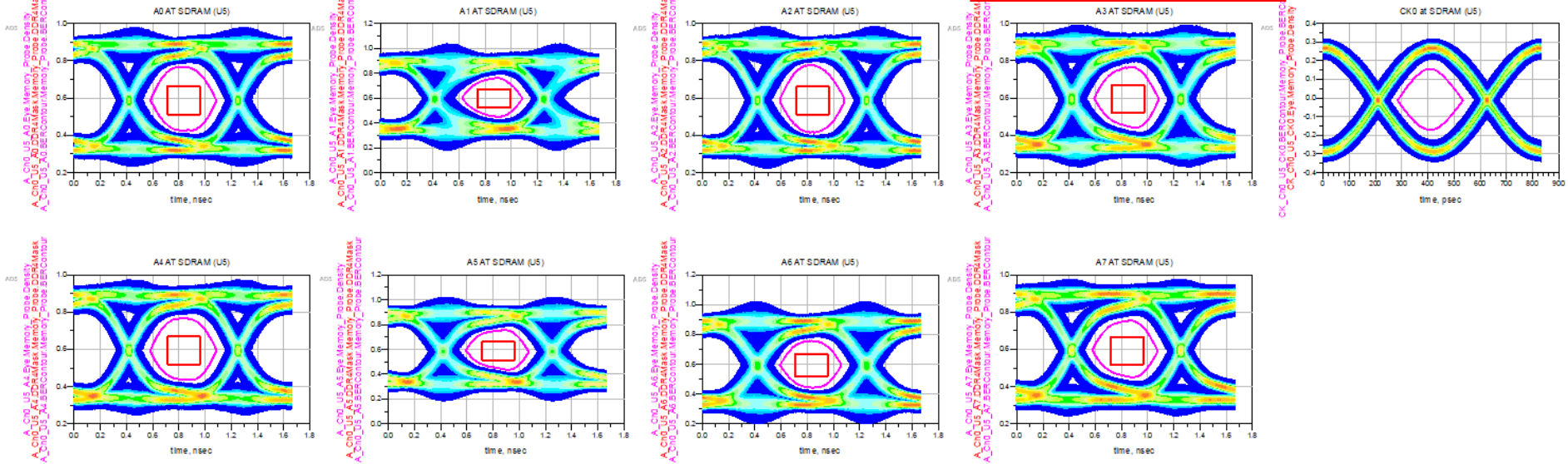
NORTHROP GRUMMAN

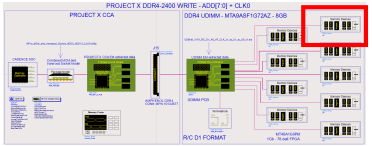
Results DDR4-2400 ADD[7:0] at SDRAM (U5) on UDIMM – FAST IBIS Corner

Simulation type: Statistical
Number of Bits: NA
CaCtrl Timing: 1T Timing

DDR4-2400 WRITE -ADD[7:0] AT SDRAM (U5)

CADENCE SOC IBIS CORNER = FAST
CADENCE SOC DRIVER STRENGTH = 40 OHM
RJ ADDED AT MEMORY CONTROLLER = 0.02 UI





A[7:0] ALL PASSED BER @ DDR4-2400

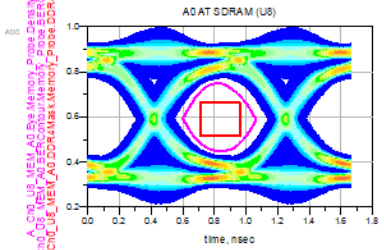
NORTHROP GRUMMAN

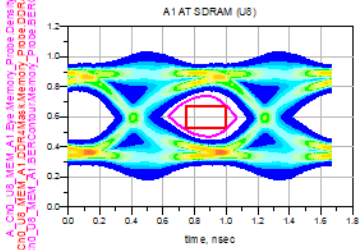
Results DDR4-2400 ADD[7:0] at SDRAM (U8) on UDIMM – FAST IBIS Corner

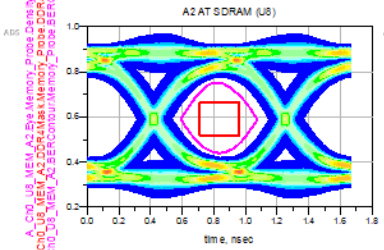
Simulation type: Statistical
Number of Bits: NA
CaCtrl Timing: 1T Timing

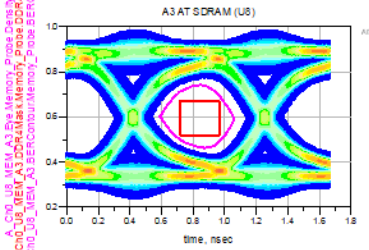
DDR4-2400 WRITE - ADD[7:0] AT SDRAM (U8)

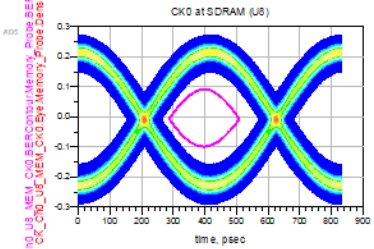
CADENCE SOC IBIS CORNER = FAST
CADENCE SOC DRIVER STRENGTH = 40 OHM
RJ ADDED AT MEMORY CONTROLLER = 0.02 UI

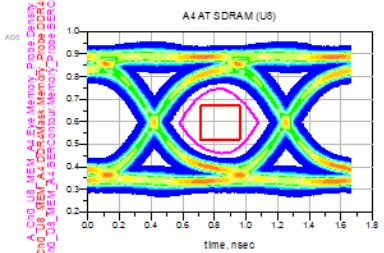


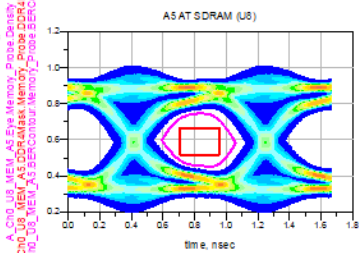


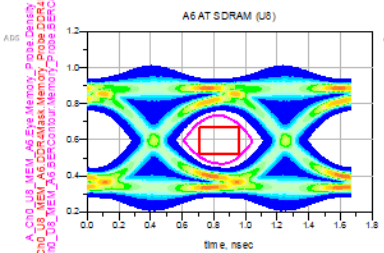


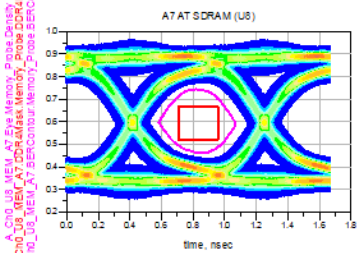


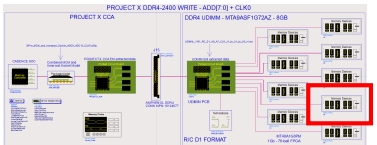












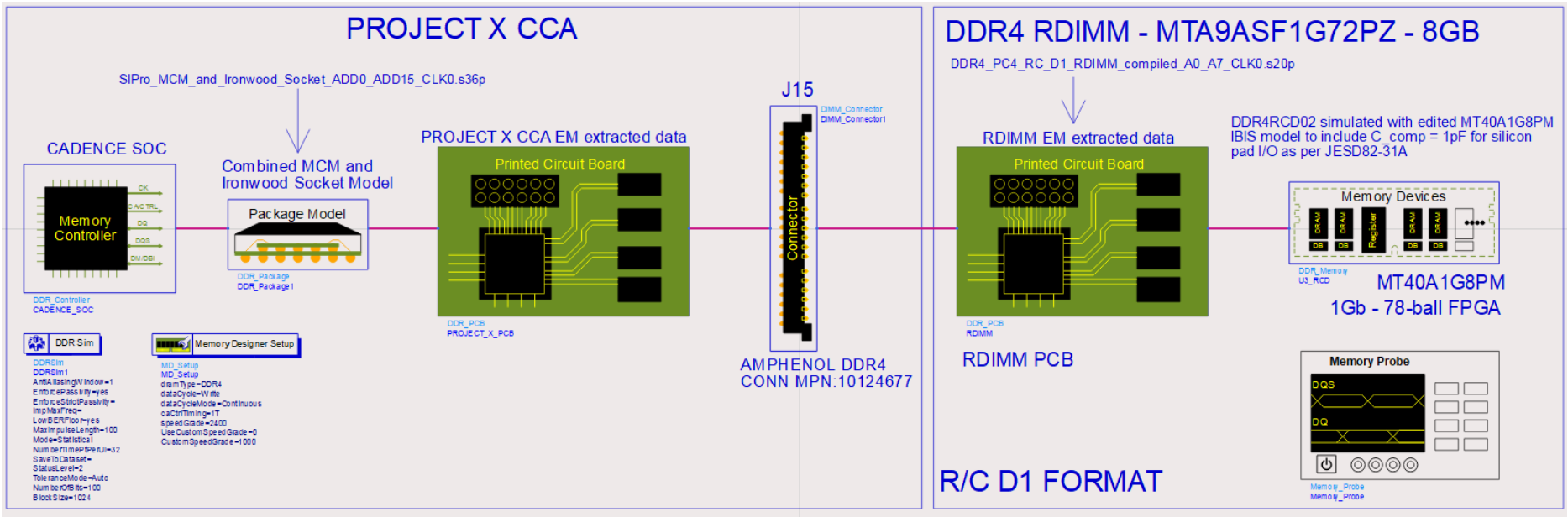
A[7:0] ALL PASSED BER @ DDR4-2400

NORTHROP GRUMMAN

DDR4-2400 Write ADD[7:0] + CLK0 Results with RDIMM (R/C D1)

NORTHROP GRUMMAN

Simulation Model – DDR4-2400 Write – ADD[7:0] + CLK0 with RDIMM



NORTHROP GRUMMAN

System Models - IBIS Models – RDIMM RCD

MICRON SDRAM MPN: MT40A1G8

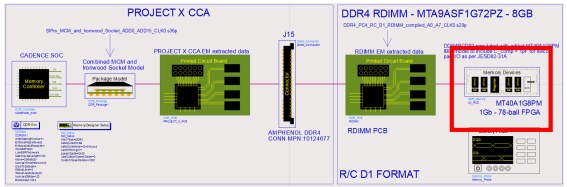
| z91b.ibs * IBIS 4.2 Model
| 8Gb DDR4 SDRAM - Die Revision "A"
| This Model is valid for Commercial Temperature Range 0C<=Tc<=95C
|
| Valid for DDR4-1600/1866/2133/2400/2666 operation
| Models *_2666 are applicable for speed grade 2666 Mbps (-075) and below
|

Part Number	VDD/VDDQ	Architecture	Package
MT40A2G4PM	1.2V/1.2V	2Gb x 4	78-Ball FBGA
MT40A1G8PM	1.2V/1.2V	1Gb x 8	78-Ball FBGA
MT40A512M16HA	1.2V/1.2V	512Mb x 16	96-Ball FBGA
MT40A2G4Z91B	1.2V/1.2V	2Gb x 4	Bare Die
MT40A1G8Z91B	1.2V/1.2V	1Gb x 8	Bare Die
MT40A512M16Z91B	1.2V/1.2V	512Mb x 16	Bare Die

[IBIS Ver] 4.2
[File Name] z91b.ibs
[Date] 09/22/2014
[File Rev] 1.0
[Source] From silicon level SPICE model at Micron Technology, Inc.
For support e-mail modelsupport@micron.com

MICRON SDRAM ibis model (z91b.ibs) was edited by setting the C_comp = 1pF as per the min, typ, & max allowed input/output pad capacitance for CAC and CLK pins, this is defined in the JEDEC JESD82-31A standard, Table 139

Model used for simulation



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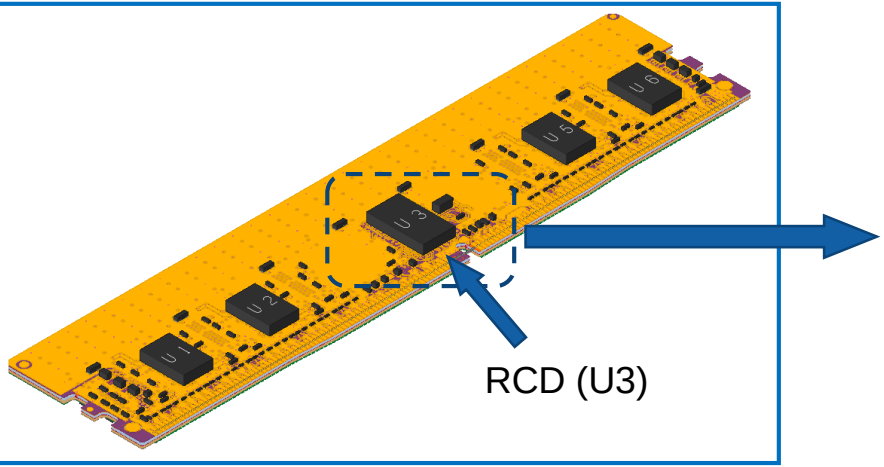
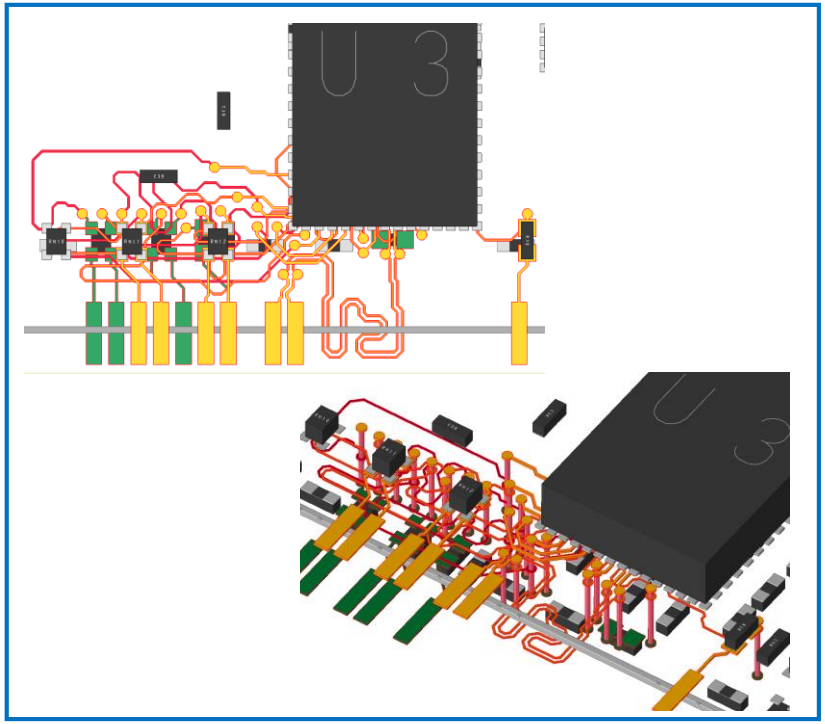
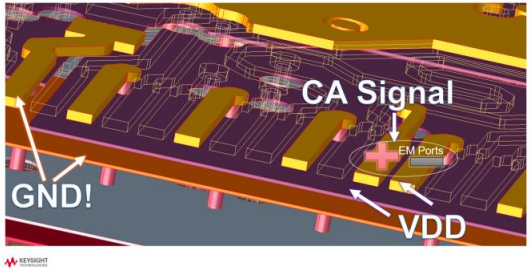
RDIMM EM Extracted Model – ADD[7:0] + CLK0





DDR4 Command Address Signals Reference VDD not GND!



**ALL CAC net return ports reference VDD not GND.
CLK0_t/ CLK0_c return port does reference GND

EM Extraction based on UDIMM Layout Data: PC4-RDIMM_RC_D1_R100_V200_20160408.zip

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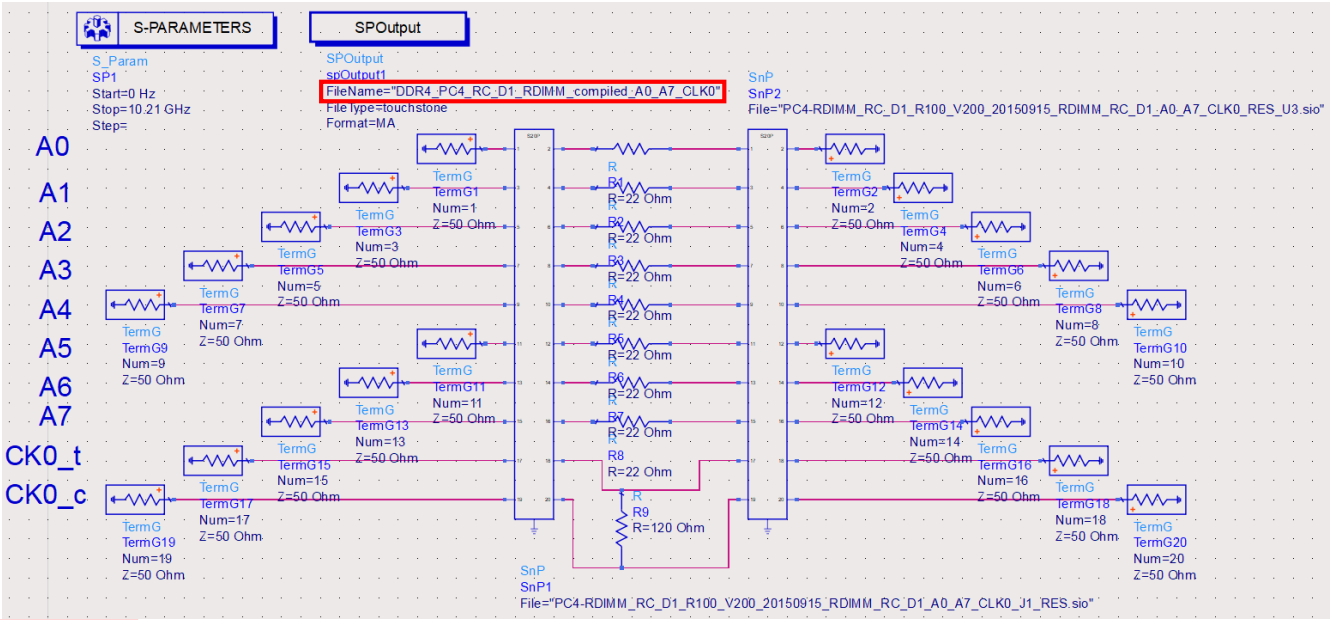
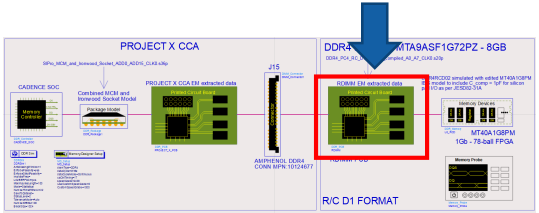
RDIMM EM Extracted Model – ADD[7:0] + CLK0



DDR4_PC4_RC_D1_RDIMM_compiled_A0_A7_CLK0.s20p



*All CAC nets shown include ideal 22Ω series resistors model to RCD
*CLK0 include ideal 120Ω termination added in this model to RCD

EM Extraction based on UDIMM Layout Data: PC4-RDIMM_RC_D1_R100_V200_20160408.zip

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RDIMM Receiver Eye Mask at Registered Clock Driver (RCD)

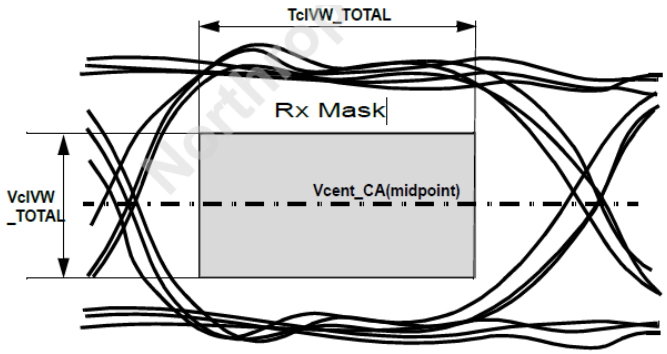

Figure 39 — CA Receiver(Rx) mask

DDR4RCD02 input receiver to successfully capture a valid input
signal with BER < 1e-18

*Table 109 is from JEDEC JESD82-31A

Table 109 — CA Input Receiver Voltage Margin and AC Timing by Speed Bin for DDR4-1600 -3200

Speed		DDR4-1600/ 1866/2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	NOTE
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
VcIVW_TOTAL	Rx Mask p-p voltage total	-	150	-	120	-	120	-	110	-	100	mV	1,2,3,4
TcIVW_TOTAL	Rx timing window total	-	0.2	-	0.15	-	0.15	-	0.135	-	0.135	UI	1,4
VIHL_AC	CA AC input pulse amplitude pk-pk	180	-	150	-	140	-	130	-	120	-	mV	5
TcIPW	CA input pulse width	0.5	-	0.4	-	0.3	-	0.3	-	0.3	-	UI	6
tCK2CA	CK to CA offset	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	UI	7
tCACA	CA to CA offset	-	0.04	-	0.04	-	0.04	-	0.04	-	0.04	UI	8
SRIN_cIVW	Input Slew Rate over VcIVW_TOTAL	1	5	1	5	1	5	1	5	1	5	V/ns	9

* UI=tck(avg)min

NOTE 1: CA Rx mask voltage and timing total input valid window where VcIVW is centered around Vcent_CA(midpoint). The data Rx mask is applied per bit and includes voltage and temperature drift terms. The design specification is BER ≤1e-18.
NOTE 2: Rx mask voltage AC swing peak-peak requirement over TcIVW_TOTAL with at least half of VcIVW_TOTAL(max) above Vcent_CA(midpoint) and at least half of VcIVW_TOTAL(max) below Vcent_CA(midpoint).
NOTE 3: The VcIVW voltage levels are centered around Vcent_CA(midpoint).
NOTE 4: Overshoot and Undershoot Specifications see Table 117 and Figure 50.
NOTE 5: CA input pulse signal swing into the receiver must meet or exceed VIHL_AC for at least one point over the duration of TcIPW for any UI during which there is a signal transition. No timing requirement above level. VIHL_AC is the peak to peak voltage centered around Vcent_CA(midpoint), which is defined in Figure 40.
NOTE 6: CA minimum input pulse width defined at the Vcent_CA(midpoint).
NOTE 7: CK to CA offset defined within all ADD/CMD and CTRL inputs at DDR4RCD02 balls. Includes all DDR4RCD02 process, voltage and temperature variation.
NOTE 8: CA to CA offset is defined as the magnitude of the difference between the min and max CK to CA offset at DDR4RCD02 balls for a given component. Includes all DDR4RCD02 voltage and temperature variation.
NOTE 9: Input slew rate over VcIVW Mask centered at Vcent_CA(midpoint). . This single-ended slew rate also applies to CK_t and CK_c.

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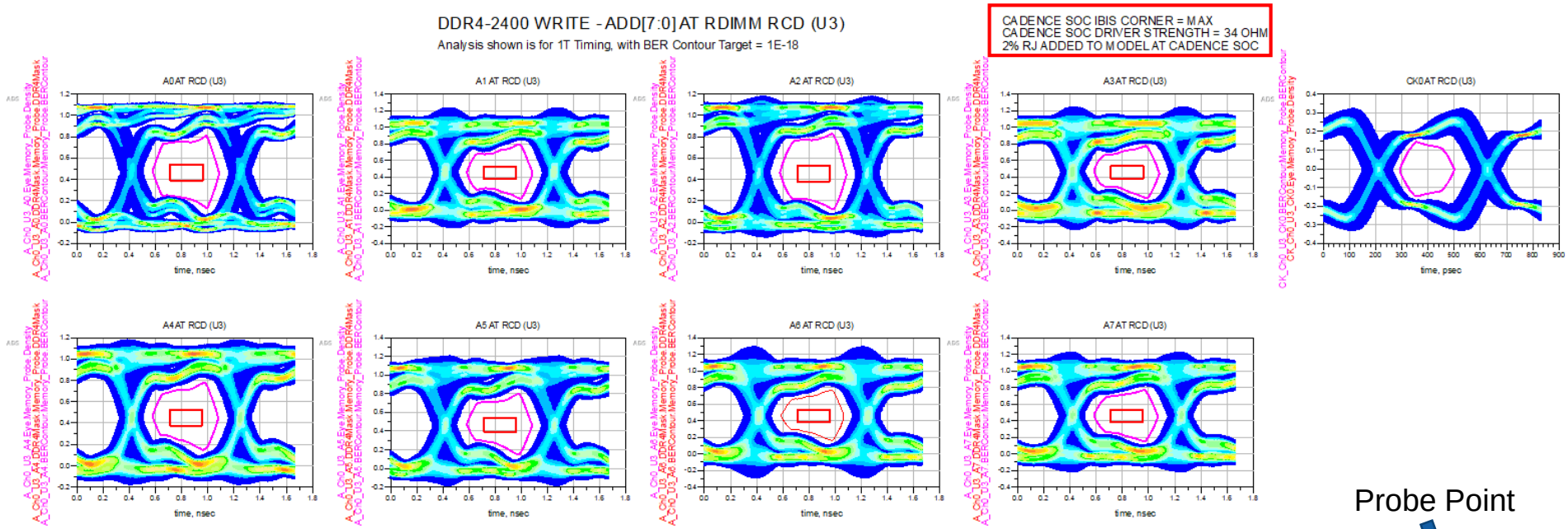
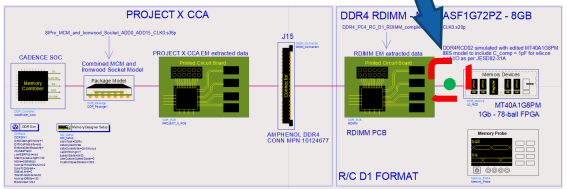
DDR4-2400 Write Results – A[7:0] + CLK0 on RDIMM – MAX IBIS Corner



Probe Point



*Eye mask shown is as per JEDEC JESD82-31A, Table 109 for DDR4-2400 with BER TARGET = 1E-18.

*Results shown include 2% Random Jitter injected at Memory Controller

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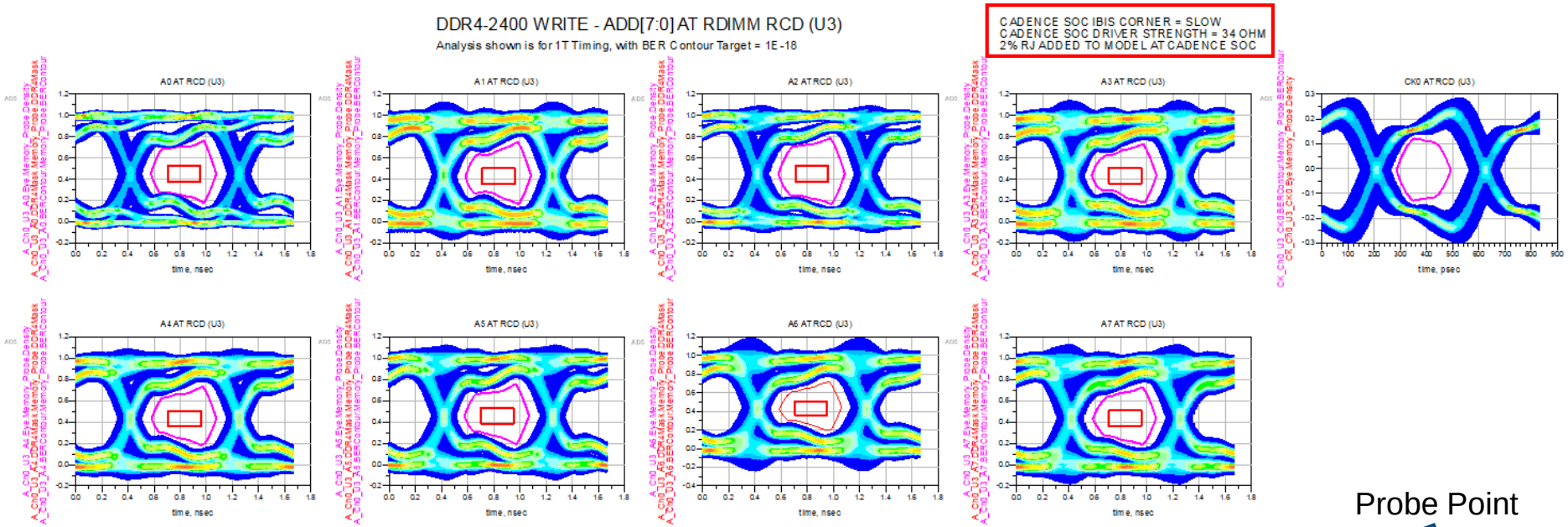
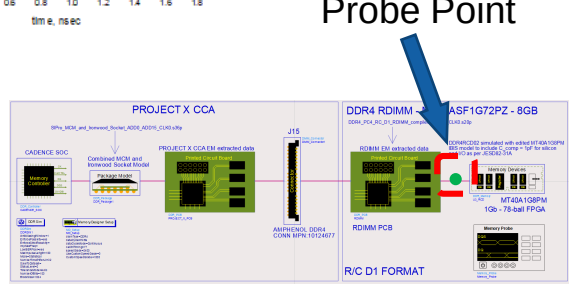
DDR4-2400 Write Results – A[7:0] + CLK0 on RDIMM – SLOW IBIS Corner



*Eye mask shown is as per JEDEC JESD82-31A, Table 109 for DDR4-2400 with BER TARGET = 1E-18.

*Results shown include 2% Random Jitter injected at Memory Controller



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