Welcome to

DESIGNCON® 2024

WHERE THE CHIP MEETS THE BOARD

Conference

January 30 – February 1, 2024

Expo

January 31 – February 1, 2024

Santa Clara Convention Center

Unmasking Voltage Regulator Instability: What Vendor Reference Designs Aren't Telling You

Speaker: Will McCaffrey, Northrop Grumman

Authors: Will McCaffrey, Northrop Grumman, Benjamin Dannan, Signal Edge Solutions

Author Bios

William McCaffrey

Digital Hardware Engineer, Northrop Grumman
William.McCaffrey@ngc.com

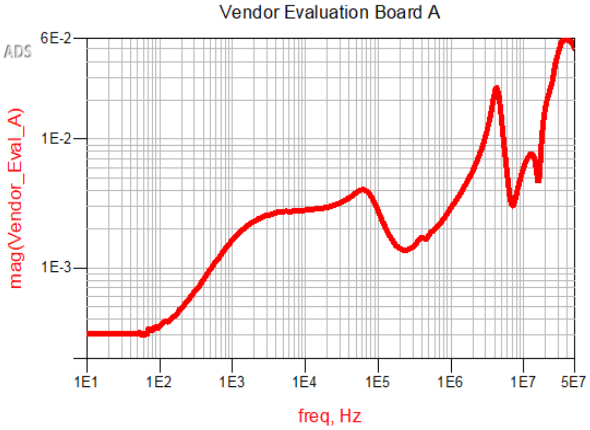
Will McCaffrey is a Digital Hardware Engineer at Northrop Grumman Mission Systems. He holds a BSEE from Rochester Institute of Technology in Rochester NY, and a MSEE from Johns Hopkins University. His interest is in high-speed digital design, SI/PI simulation and measurement. He has authored peer-reviewed journal publications to Signal Integrity Journal and has co-authored a peer-reviewed publication to DesignCon 2022.

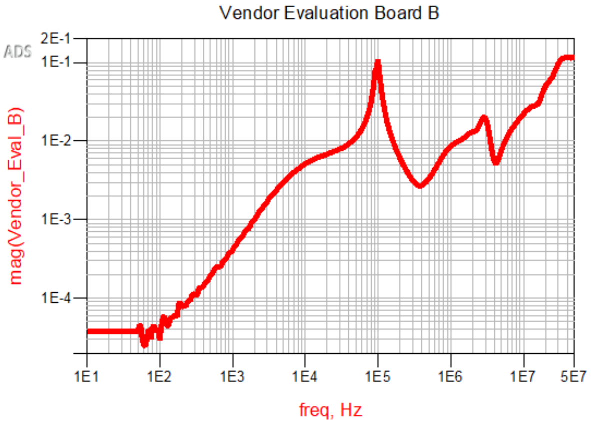
Benjamin Dannan

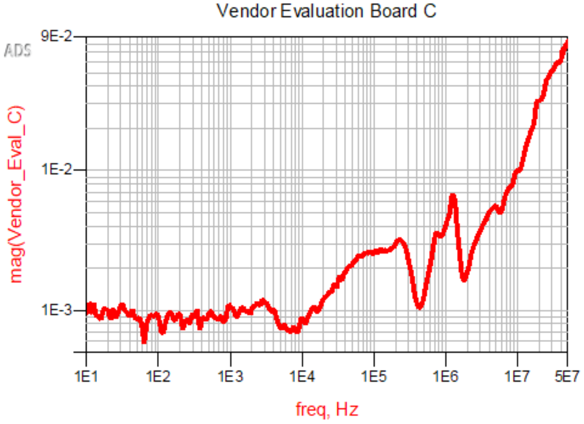
Chief Technologist, Signal Edge Solutions
ben@signaledgesolutions.com

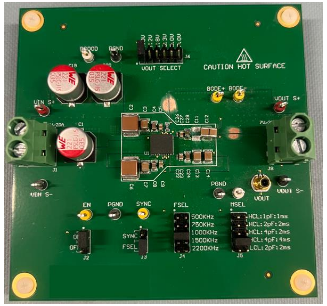
Benjamin holds a certification in cybersecurity, has a BSEE from Purdue University, a Master of Engineering in Electrical Engineering from The Pennsylvania State University, and graduated from the USAF Undergraduate Combat Systems Officer training school with an aeronautical rating. Benjamin is a trained Electronic Warfare Officer in the USAF with deployments on the EC-130J Commando Solo in Afghanistan and Iraq totaling 47 combat missions, as well as a trained USAF Cyber Operations Officer. In addition, he has co-authored multiple peer-reviewed journal publications and has received the prestigious DesignCon 2020 best paper award, given to authors leading as practitioners in semiconductor and electronic design.

What Do All of These VRM Eval Boards Have in Common?


Vendor Evaluation Board A


Vendor Evaluation Board B


Vendor Evaluation Board C



They are ALL Unstable!

Eval Board Regulator	Resonance Frequency	Q Factor	Phase Margin
ISL70002SEHD	4.46 MHz	3.21	17.7^o
LTM4637	109 kHz	7.15	7.9^o
TPSM843B22	1.44 MHz	3	19^o

Q < 2 is always 30^o of phase margin!

What Makes These Regulators Unstable?

- **There are resonances in the output impedance on the PDN**
- **A Bode Plot of the plant will show if you regulator is stable or not, but it will not tell you if you PDN is stable!**
- **Definition of Target Impedance**
  - Voltage allowed set by the load
  - Imax set by the load, and the current is both dynamic and frequency independent
  - Impedance is the only term the designer has control over! A poorly placed resonance could be devastating

$$Z_{Target} = \frac{\Delta V_{Allowed}}{\Delta I_{Max}}$$

How Do We Measure Stability

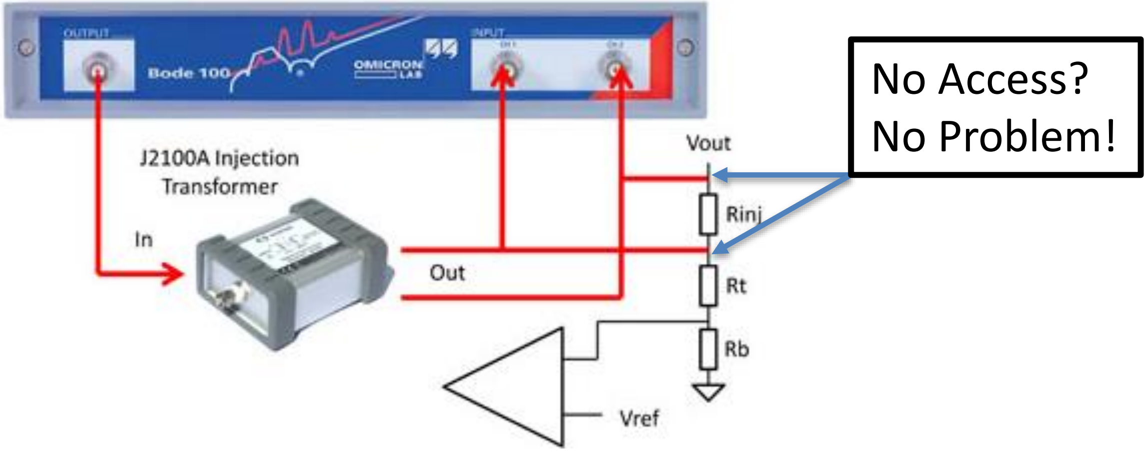
- **Stability is the most essential measurement to ensure closed loop performance**

$$\boldsymbol{Closed\ Loop = \frac{Open\ Loop}{1 + T}}$$

- **Historically stability was measured through Bode plots**
  - Requires injecting a signal into the loop
  - Does not consider the PDN impact in stability assessment

What if we don’t have access to the feedback network?

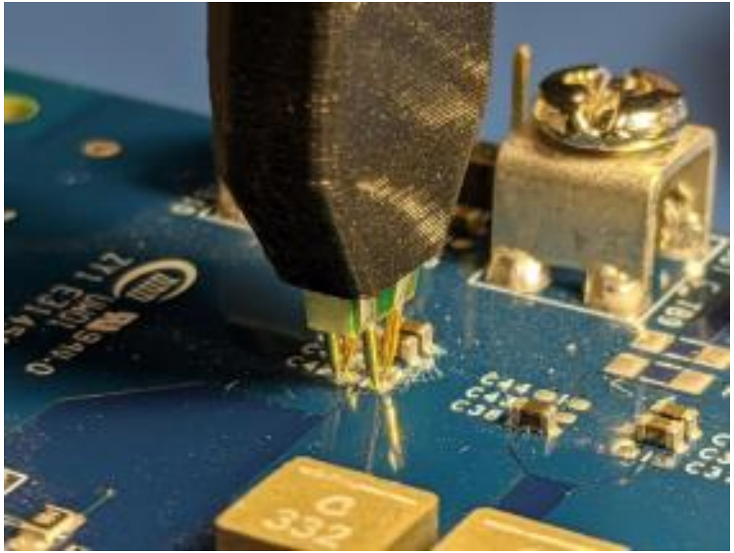
- **To measure stability with a bode plot, we need to cut traces and inject a signal**
- **Sometimes all you have is a capacitor pad on the output voltage rail**
- **That is all you need!**



Source: https://www.picotest.com/wemeasurepower2012/28-slide.html

How do we practically measure NISM?

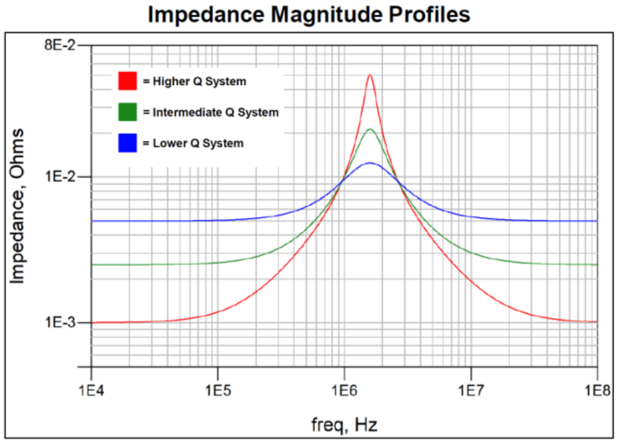
- **Impedance Measurement provides three data points**
  - Impedance Magnitude, Phase, Group Delay
  - NISM takes it from there!
- **NISM shows the systems stability, measures overall PDN**
- **NISM is available on all VNA and FRAs**
  - Omicron Bode 100
  - Keysight E5061B
  - And many more!



Source: Picotest.com

Wanted: Flat Impedance and Low Q-Points

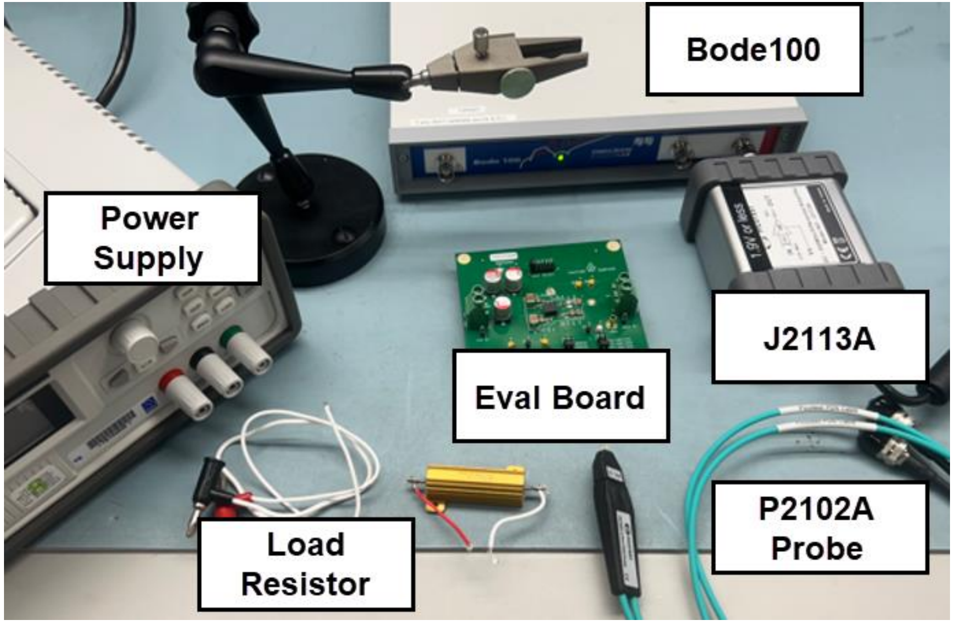
- **Flat impedance is relative, and difficult to pull off**
- **Low Q PDN**
  - Lower reaction to transient changes, minimal ringing present
- **Impedance and high Q resonances look similar, but have different causes**
  - Impedance resonance due to passive resonance of system, present at power on and off
  - High Q resonance due to VRM feedback loop, only present with power on



Source: Witcher, S., Sandler, S., DesignCon (2023). *A New Power Integrity Requirement to Supplement Target Impedance: Quantifying PDN Impedance Flatness from Sandler NISM* Santa Clara, CA; *DesignCon.*

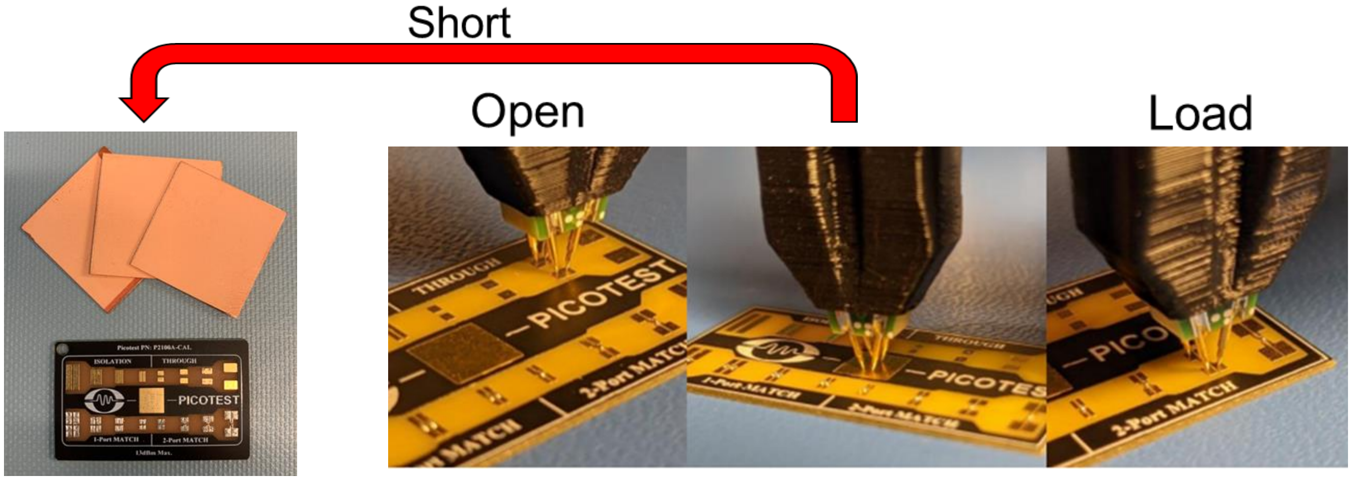
Demo 1, TPSM843B22

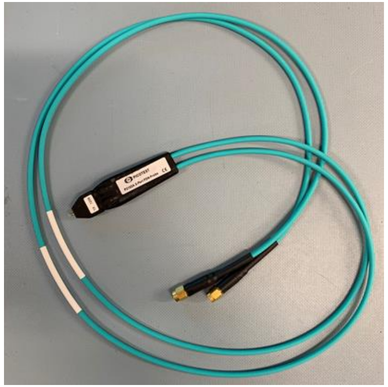
- **TPSM843B22 Evaluation Board, TPSM843B22EVM**
  - VIN: 4V to 18V
  - VOUT: 0.5V to 7V
  - Max Current: 20A
- **Equipment Used**
  - Omicron Bode100
  - J2113A Semi-Floating Differential Amplifier
  - P2101A 2-Port Probe
  - Keysight N2787A Probe Holder



Demo 1, Setup and Calibration

- The effects of cables, connectors, and probe tips must be zeroed-out before measurements can be taken
- A short, open, load (SOL) calibration helps us set the reference point of our measurement to the device under test (DUT)

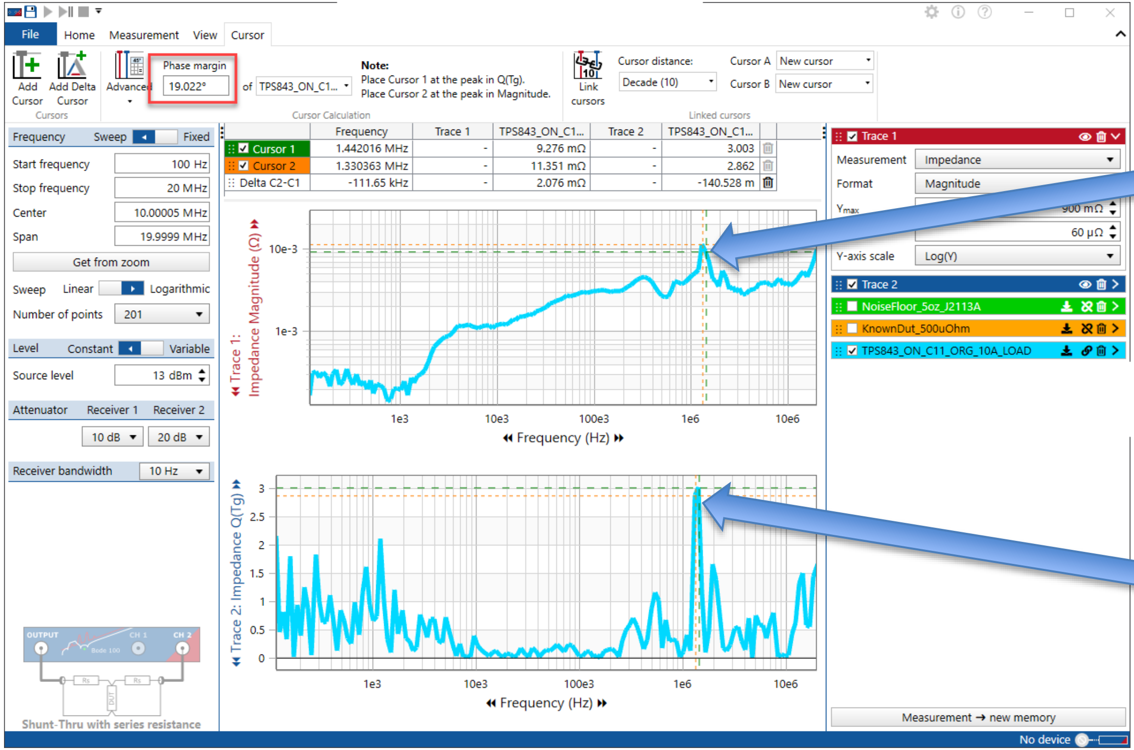




Picotest P2102A Probe

*Short calibration with 5oz copper reduces noise floor of measurement setup.

Measurement of Output Impedance (Zo)



Phase margin 19.022° of TPS843_ON_C1...

Note:
Place Cursor 1 at the peak in Q(Tg).
Place Cursor 2 at the peak in Magnitude.

Cursor distance: Decade (10)
Cursor A: New cursor
Cursor B: New cursor

Frequency Sweep ◂ Fixed

Start frequency: 100 Hz
Stop frequency: 20 MHz
Center: 10.00005 MHz
Span: 19.9999 MHz
Sweep: Linear ▸ Logarithmic
Number of points: 201
Level: Constant ◂ Variable
Source level: 13 dBm
Attenuator: Receiver 1 10 dB, Receiver 2 20 dB
Receiver bandwidth: 10 Hz

	Frequency	Trace 1	TPS843_ON_C1...	Trace 2	TPS843_ON_C1...
☑ Cursor 1	1.442016 MHz	-	9.276 mΩ	-	3.003
☑ Cursor 2	1.330363 MHz	-	11.351 mΩ	-	2.862
Delta C2-C1	-111.65 kHz	-	2.076 mΩ	-	-140.528 m

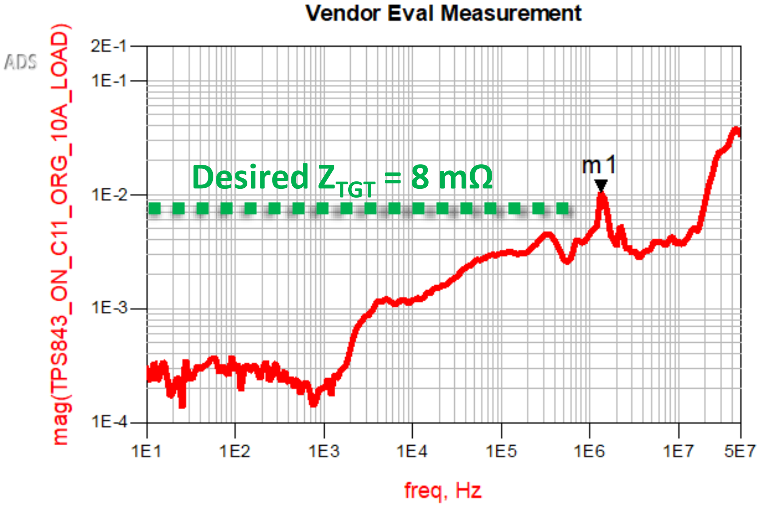
☑ Trace 1
Measurement: Impedance
Format: Magnitude
Y_{max}: 900 mΩ
60 µΩ
Y-axis scale: Log(Y)

☑ Trace 2
☐ NoiseFloor_5oz_J2113A
☐ KnownDut_500uOhm
☑ TPS843_ON_C11_ORG_10A_LOAD

Resonance Point
1.44 MHz, PM of 19⁰

Q Factor of 3!

What can fix this resonance point?



m1
freq=1.316 MHz
mag(TPS843_ON_C11_ORG_10A_LOAD)=0.011

Step 1: Determine peak inductance (from Z)

$$L_{peak} = \frac{X_L}{2\pi f} = \frac{11 m\Omega}{2\cdot\pi\cdot 1.316\ MHz} = 1.33 nH$$

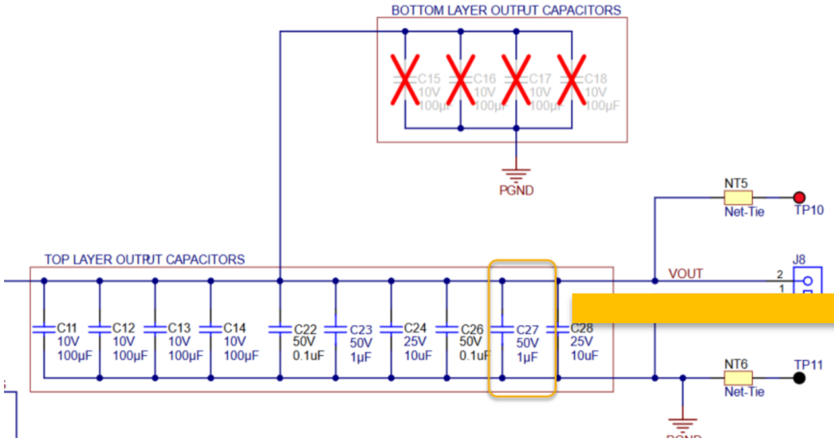
Step 2: Determine Z_{TGT} and solve for C.

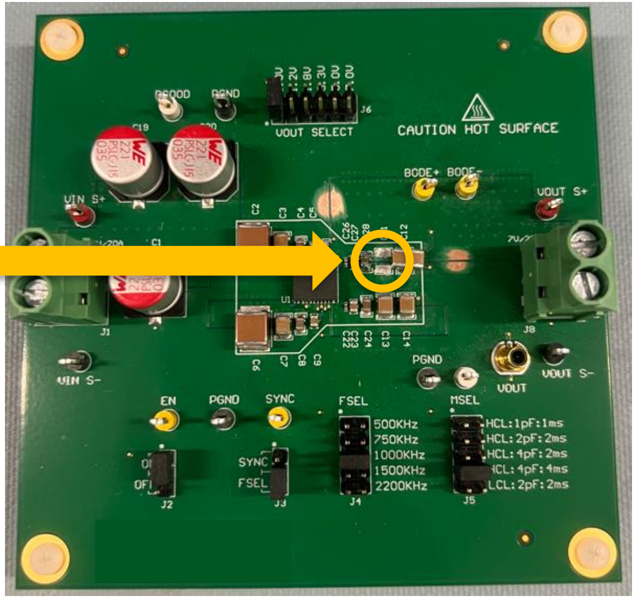
$$C = \frac{L_{peak}}{R^2} = \frac{1.33\ nH}{(8\ m\Omega)^2} = 21\ \mu F$$

Step 3: Find equivalent capacitor, set capacitor ESR ≤ Z_{TGT} and update design

Select -> 22 μF capacitor with ESR ≤ 8 mΩ

Adding a 22 µF Capacitor to the Eval Board





- Swapped a 1uF Capacitor, with a resonance frequency of 10 MHz with a 22uF capacitor, with an ESR of 4 mΩ, as $Z_o < Z_{TGT}$ at 10MHz

C27 Original: GCM21BR71H105KA03L
C27 New: 885012107011

Measurement of Zo with Updated Capacitor

Phase margin: 33.613° of TPS843_ON_C1...

Note:
Place Cursor 1 at the peak in Q(Tg).
Place Cursor 2 at the peak in Magnitude.

Cursor distance: Decade (10)
Cursor A: New cursor
Cursor B: New cursor

	Frequency	Trace 1	TPS843_ON_C1...	Trace 2	TPS843_ON_C1...
☑ Cursor 1	659.611 kHz	-	4.145 mΩ	-	1.458
☑ Cursor 2	688.509 kHz	-	4.206 mΩ	-	1.411
Delta C2-C1	28.898 kHz	-	60.867 µΩ	-	-46.624 m

Frequency Sweep Fixed
Start frequency: 100 Hz
Stop frequency: 20 MHz
Center: 10.00005 MHz
Span: 19.9999 MHz
Sweep: Linear / Logarithmic
Number of points: 201
Level: Constant / Variable
Source level: 13 dBm
Attenuator: Receiver 1: 10 dB; Receiver 2: 20 dB
Receiver bandwidth: 10 Hz

☑ Trace 1
Measurement: Impedance
Format: Magnitude
Ymax:
Ymin: 60 µΩ
Log(Y)

☑ Trace 2
☐ NoiseFloor_5oz_J2113A
☐ KnownDut_500uOhm
☐ TPS843_ON_C11_ORG_10A_LOAD
☑ TPS843_ON_C11_UPD_10A_LOAD

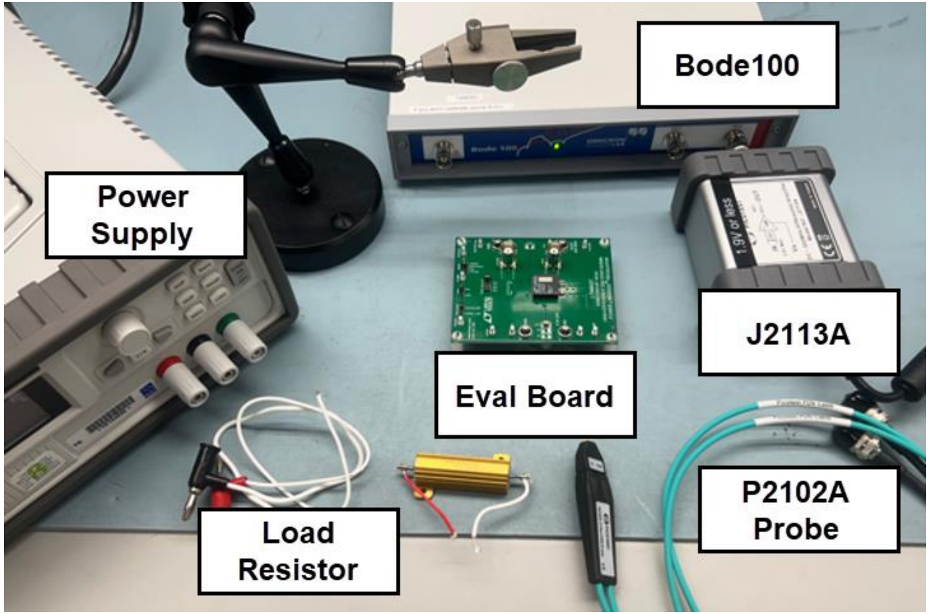
Resonance Point 659.6MHz, PM of 33.6^{o}
A 14.6^{o} PM improvement, just with a BOM change!

Highlights PDN capacitor selection not optimized!

Q Factor of 1.45, reduced by over ½!

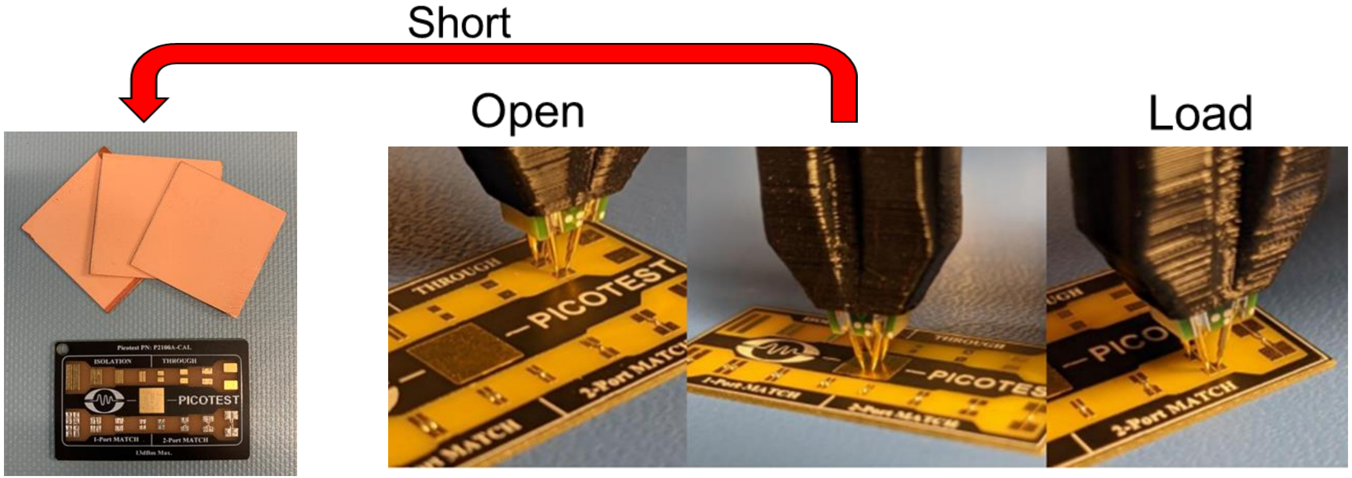
Demo 2, LTM4637

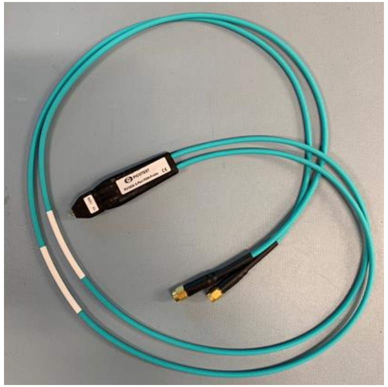
- **LTM4637 Evaluation Board, DC1872A**
  - VIN: 4.5V to 20V
  - VOUT: 1V to 1.8V
  - Max Current: 20A
- **Equipment Used**
  - Omicron Bode100
  - J2113A Semi-Floating Differential Amplifier
  - P2101A 2-Port Probe
  - Keysight N2787A Probe Holder



Demo 2, Setup and Calibration

- The effects of cables, connectors, and probe tips must be zeroed-out before measurements can be taken
- A short, open, load (SOL) calibration helps us set the reference point of our measurement to the device under test (DUT)





Picotest P2102A Probe

*Short calibration with 5oz copper reduces noise floor of measurement setup.

Demo 2, Meas. of Zo at C13

Phase margin 7.949° of LTM4637_ON_C...

Note:
Place Cursor 1 at the peak in Q(Tg).
Place Cursor 2 at the peak in Magnitude.

Cursor distance: Decade (10)
Cursor A New cursor
Cursor B New cursor

	Frequency	Trace 1	LTM4637_ON_C...	Trace 2	LTM4637_ON_C...
☑ Cursor 1	109.388 kHz	-	142.304 mΩ	-	7.145
☑ Cursor 2	109.388 kHz	-	142.304 mΩ	-	7.145
Delta C2-C1	0 Hz	-	0 Ω	-	0

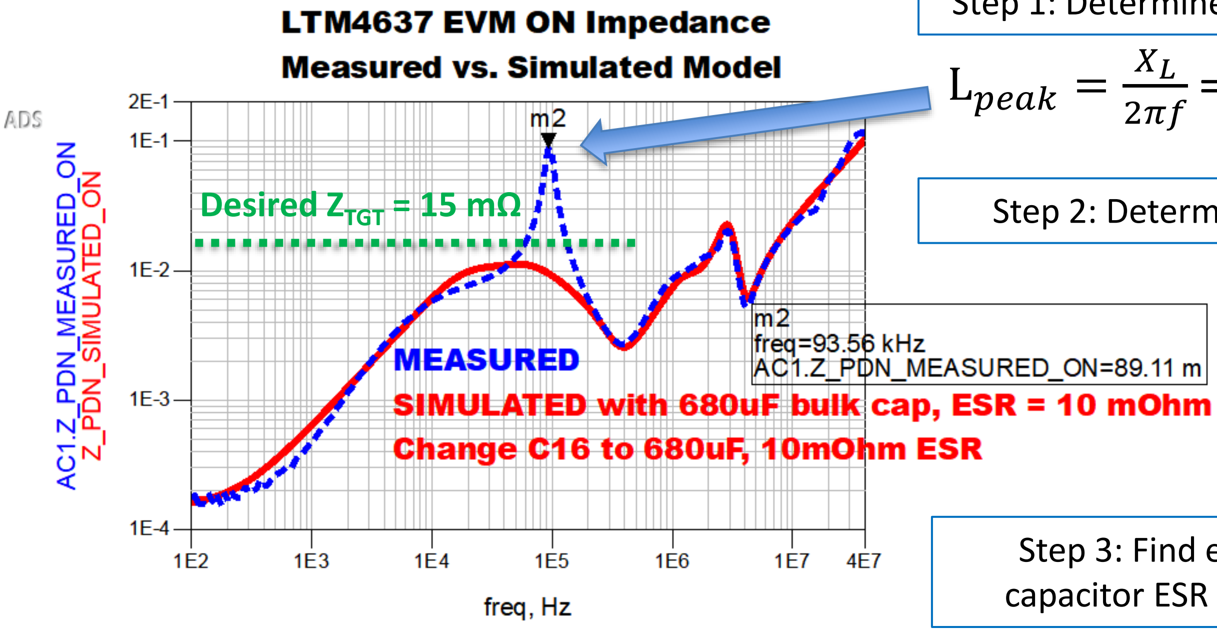
Frequency Sweep Fixed
Start frequency 20 Hz
Stop frequency 20 MHz
Center 10.00001 MHz
Span 19.99998 MHz
Sweep Linear Logarithmic
Number of points 201
Level Constant Variable
Source level 13 dBm
Attenuator Receiver 1 10 dB Receiver 2 20 dB
Receiver bandwidth 10 Hz

☑ Trace 1
Measurement Impedance
Format Magnitude
Y_{max} 900 mΩ
Y_{min} 60 µΩ
Y-axis scale Log(Y)
☑ Trace 2
☐ NoiseFloor_5oz_J2113A
☐ KnownDut_500uOhm
☑ LTM4637_ON_C13_ORG_10A_LOAD
Measurement → new memory
No device

Resonance Point 109kHz, PM of 7.9^{o}

Q Factor of 7.15!

What can fix this resonance point?



*Simulated model is based off State-Space Average VRM Model

Step 1: Determine peak inductance (from Z)

$$\mathrm{L}_{peak} = \frac{X_L}{2\pi f} = \frac{89.11 m\Omega}{2 \cdot \pi \cdot 93.56\ kHz} = 151.6\, nH$$

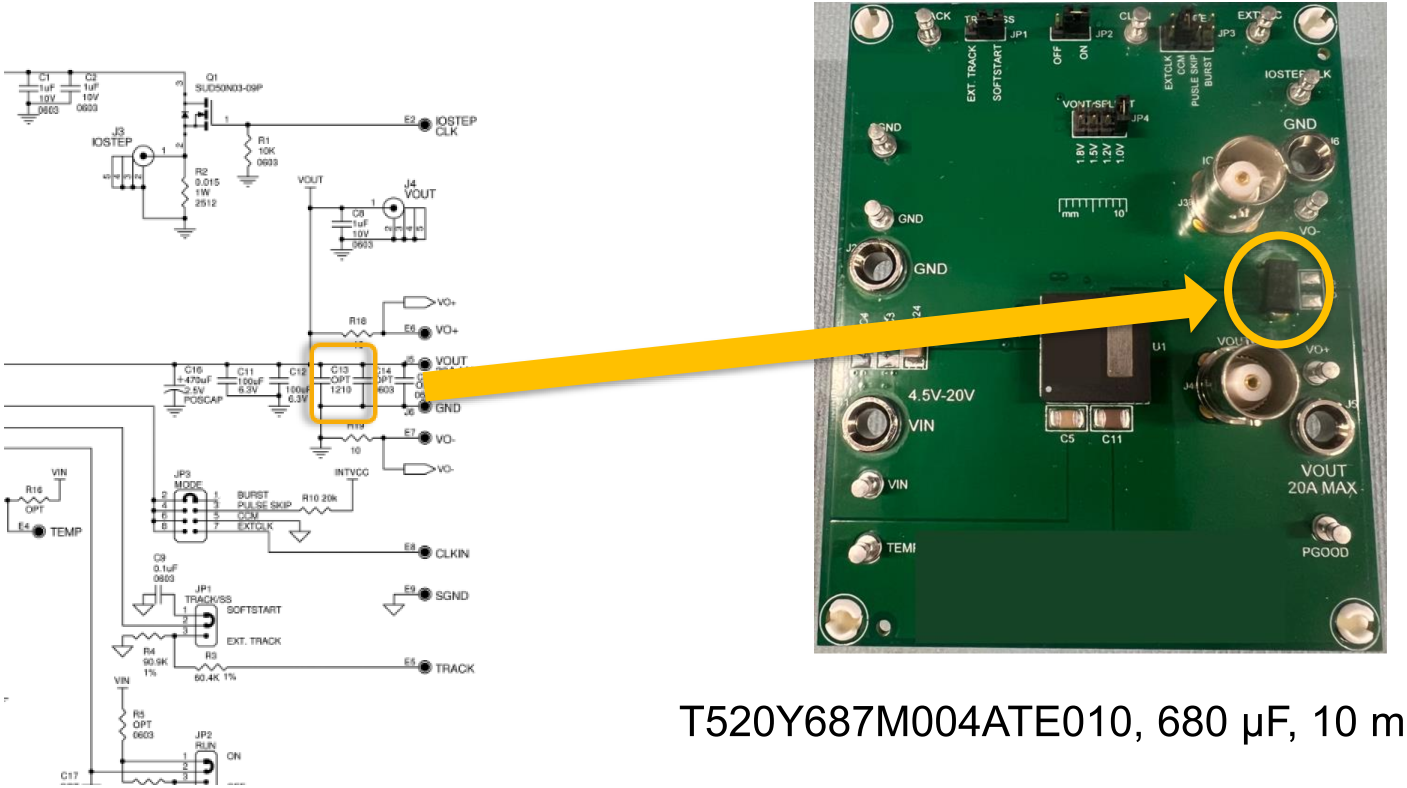
Step 2: Determine $\mathrm{Z_{TGT}}$ and solve for C.

$$\mathrm{C} = \frac{L_{peak}}{R^2} = \frac{151.6\, nH}{(15\ m\Omega)^2} = 674\ \mu F$$

Step 3: Find equivalent capacitor, set capacitor ESR ≤ $\mathrm{Z_{TGT}}$ and update design

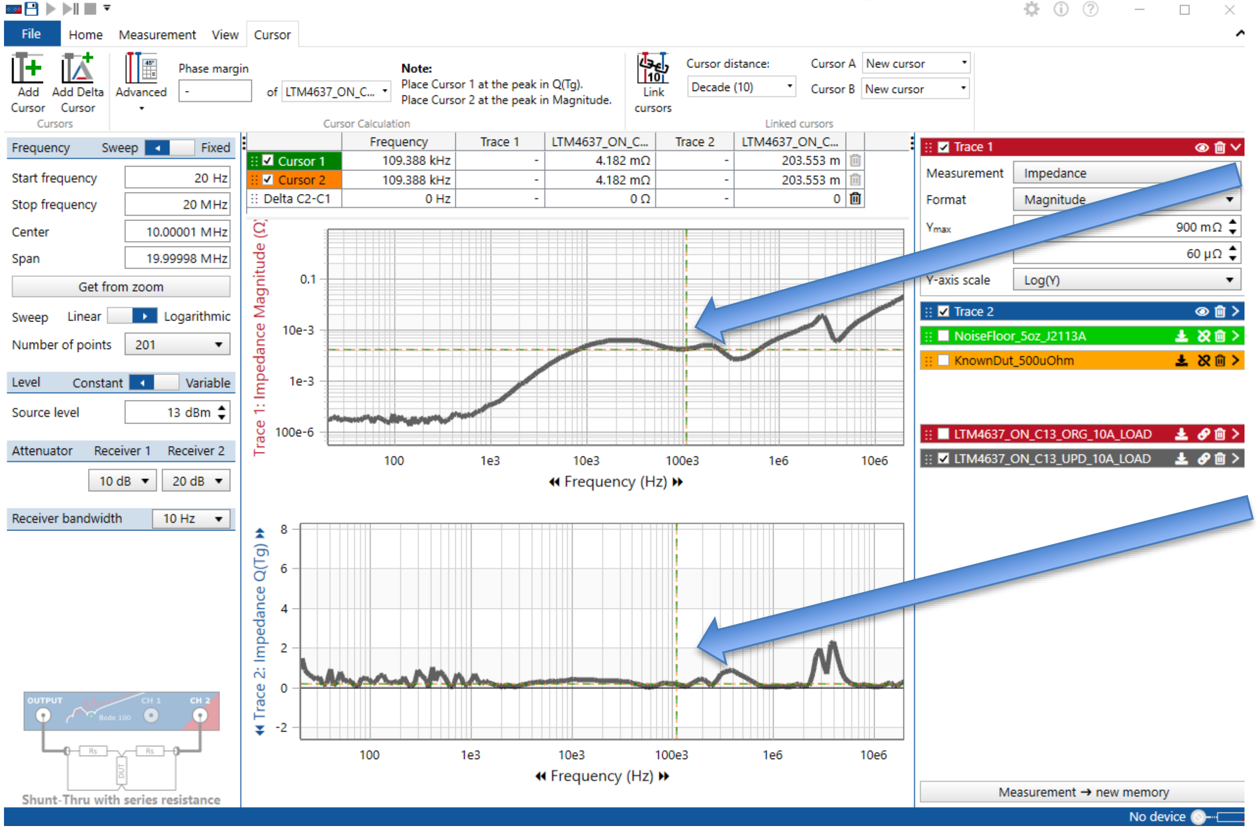
Select -> 680 µF capacitor with ESR ≤ 15 mΩ

Adding a 680 µF Capacitor to the Eval Board



T520Y687M004ATE010, 680 µF, 10 mΩ ESR

Measurement of Zo with Updated Capacitor



Phase margin: -
of LTM4637_ON_C...

Note:
Place Cursor 1 at the peak in Q(Tg).
Place Cursor 2 at the peak in Magnitude.

Cursor distance: Decade (10)
Cursor A: New cursor
Cursor B: New cursor

Frequency: Sweep / Fixed
Start frequency: 20 Hz
Stop frequency: 20 MHz
Center: 10.00001 MHz
Span: 19.99998 MHz
Sweep: Linear / Logarithmic
Number of points: 201
Level: Constant / Variable
Source level: 13 dBm
Attenuator: Receiver 1: 10 dB; Receiver 2: 20 dB
Receiver bandwidth: 10 Hz

	Frequency	Trace 1	LTM4637_ON_C...	Trace 2	LTM4637_ON_C...
☑ Cursor 1	109.388 kHz	-	4.182 mΩ	-	203.553 m
☑ Cursor 2	109.388 kHz	-	4.182 mΩ	-	203.553 m
Delta C2-C1	0 Hz	-	0 Ω	-	0

☑ Trace 1
Measurement: Impedance
Format: Magnitude
Ymax: 900 mΩ
60 µΩ
Y-axis scale: Log(Y)
☑ Trace 2
☐ NoiseFloor_5oz_J2113A
☐ KnownDut_500uOhm
☐ LTM4637_ON_C13_ORG_10A_LOAD
☑ LTM4637_ON_C13_UPD_10A_LOAD

Resonance Point 109kHz,
PM of 71^{o} or greater

Q Factor of 0.2! A 35x Improvement!

Call to Action

- **Do not trust vendor reference designs, they are not always correct**
- **Just because these VRMs are not stable does not mean they are bad. It means they are not integrated with PDN correctly.**
- **The PDN for a VRM design needs to be optimized for each application.**
- **By using NISM, a designer can measure the output impedance see the output impedance, and quickly determine PDN stability**

Conclusion

- **Both demonstrations showed that bill of material (BOM) changes had a dramatic impact on system stability. Additional BOM changes could further improve stability across entire system**
- **Accurate calibration and low inductance measurement paths are a must to properly measure impedance in the system PDN**
- **NISM is simple, accurate and widely available. Designing NISM test points is significantly easier than Bode Plot test points, and NISM can be implemented as part of final design and system sign-off**
- **Power integrity includes everything from the power supply to the load. This entire system needs to be included and measured for the system PDN to meet requirements. *PDN design is specific to each application!***

References

[1] Barnes, H. (2021). Power Integrity Target Impedance Says it All, Power Delivery is AC not DC. *14th Annual Central PA Center for Signal Integrity Symposium*, (pp. 1-54). Harrisburg.

[2] Sandler, S. (2019). Why Full VRM Characterization is Essential. Signal Integrity Journal

[3] Witcher, S., Sandler, S., DesignCon (2023). *A New Power Integrity Requirement to Supplement Target Impedance: Quantifying PDN Impedance Flatness from Sandler NISM* Santa Clara, CA; *DesignCon.*

[4] Sandler, S., Barnes, H., Dannan, B., (2023). *CHIPHEADS, Hands-On PDN Impedance and Calibration Basics;* Santa Clara, CA; DesignCon

[5] What is Non-Invasive Stability Measurement (NISM)- https://www.picotest.com/non-invasive-stability-measurement.html

Thank you!

QUESTIONS?