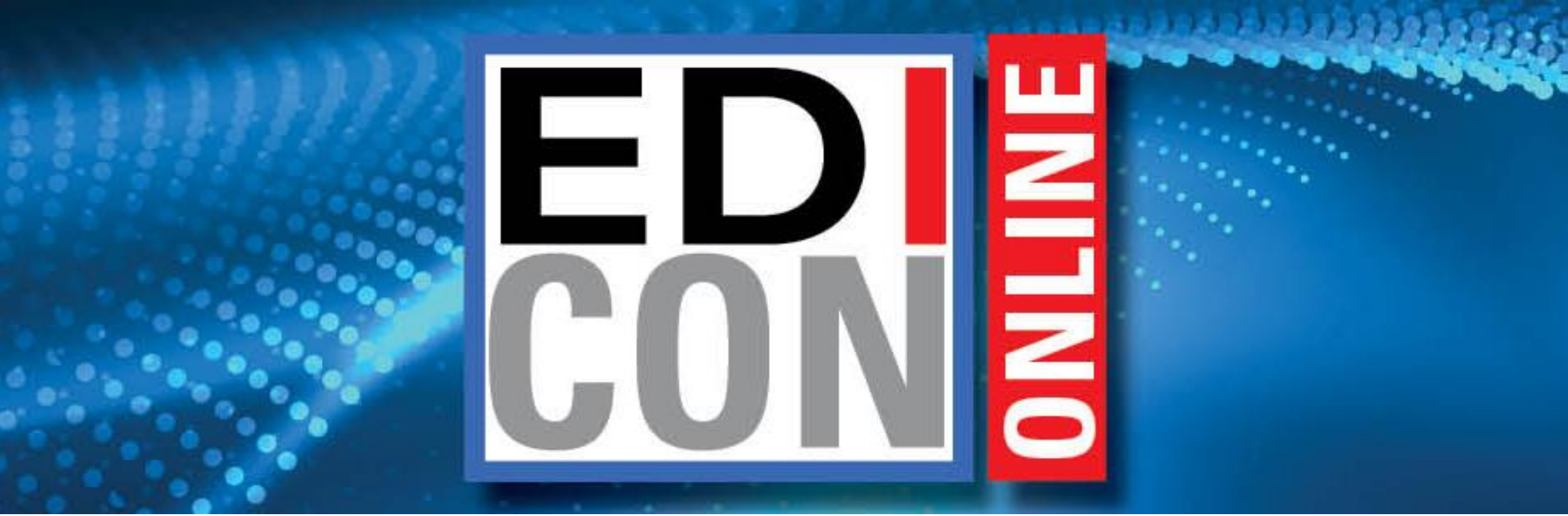


What is enough? VDDQ Package Power Integrity Analysis with a DDR4 PHY

- **Workshop Presented By: Benjamin Dannan**
- **Date: October 4, 2023**
- **Track: Signal Integrity/Power Integrity**

Abstract

As voltage margins for power rails continue to decrease, end-to-end power integrity modeling is already difficult without having to be concerned if all the models, that are part of your simulation, are correct. As system designers, we typically expect and, in most cases, assume that all the models from vendors are correct.

So, what does an engineer do if one of the models needed for a power integrity simulation is not correct? What if this is a die model? How does an engineer verify if the die model is accurate or has enough on-die capacitance to manage the high-frequency currents.

This presentation will demonstrate how to construct an end-to-end power integrity model for a DDR4 PHY and package. It will be determined, as an example, if a DDR PHY integrated into a custom ASIC has sufficient on-die capacitance for the respective DDR4 power domain.

At the end of this presentation engineers will understand how to model and develop an end-to-end power Integrity model for their ASIC while determining if their ASIC has sufficient on-die capacitance for their application.

Author Bios

Benjamin Dannan is a Technical Fellow and an experienced signal and power integrity (SI/PI) design engineer, advancing high-performance ASIC and FPGA designs. He is a Keysight ADS Certified Expert with expertise in high-speed simulation solutions and multiple 3D EM solutions.

He is a senior member of IEEE and has extensive experience with Chip-Package-PCB-VRM power delivery network (PDN) principles, high-speed circuits, and multi-layered PCB design.

Benjamin holds a certification in cybersecurity, has a BSEE from Purdue University, and a Master of Engineering in Electrical Engineering from The Pennsylvania State University. In addition, he has co-authored multiple peer-reviewed journal publications. He has received the prestigious DesignCon 2020 best paper award, given to authors leading as practitioners in semiconductor and electronic design.

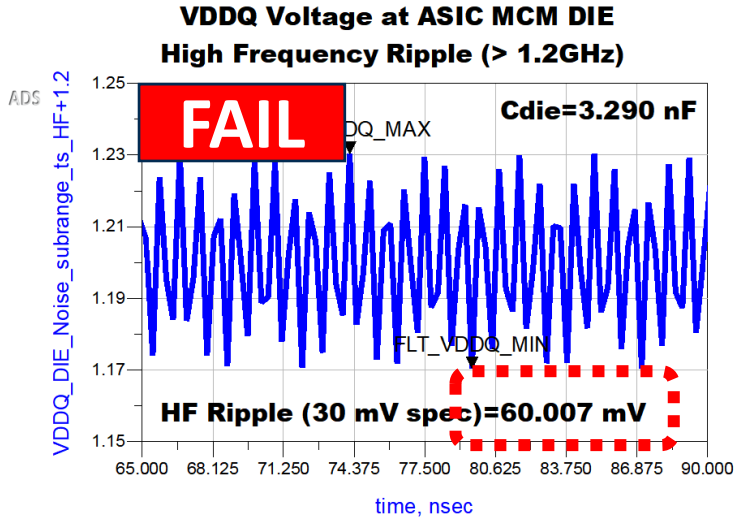
Jim Kuszewski is a Technical Fellow and a Consulting engineer at Northrop Grumman Mission Systems. He holds a BSEE from Michigan State University and a MSCS from the Johns Hopkins University. Jim is the founder of the Northrop Grumman Mission Systems Signal Integrity / Power Integrity Community of Practice. He has also worked on design automation, system security and product integrity initiatives. Currently Jim oversees many programs which use high density, multi gigabit speed SerDes, DDR memory, mixed signal, fine pitch, and high-power dissipation digital components as well as multi-chip module substrate design.

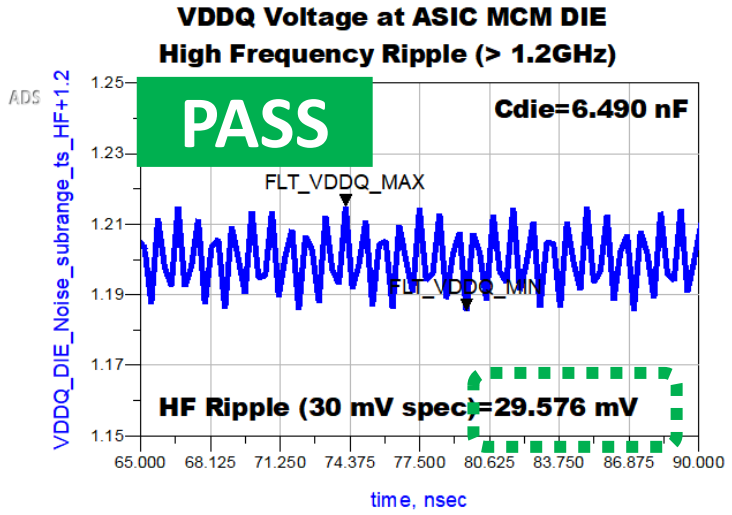
Overview

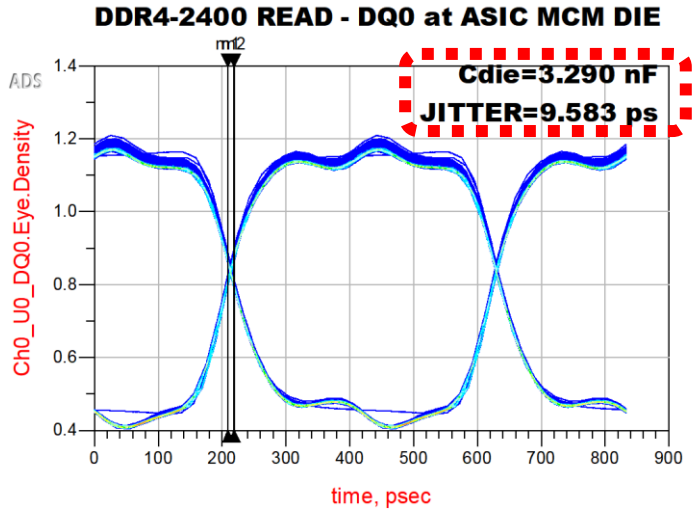
- What happens when the die model is incorrect
- PDN impedance impact from the die model
- PDN effects of the die model and package
- Why should we care about the die model
- Power Integrity case study
- How do you know if a die model from a vendor is correct?
- VDDQ Full PDN Impedance
- Determining the worst-case test pattern in simulation
- DDR4-2400 Simulation Results with worst-case test pattern
- Determining the minimum Cdie value
- DDR4-2400 Simulation model results with the updated Cdie value
- Call to action
- Summary and conclusions

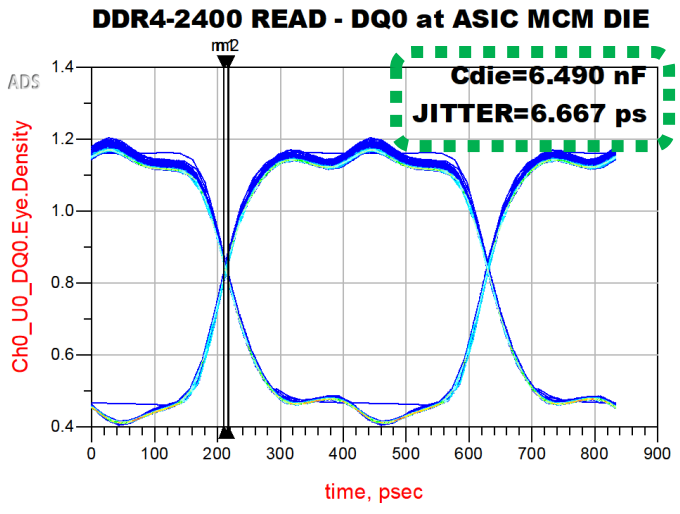
What happens when the die model is incorrect?

When the die model is not correct, both timing jitter and voltage ripple are affected



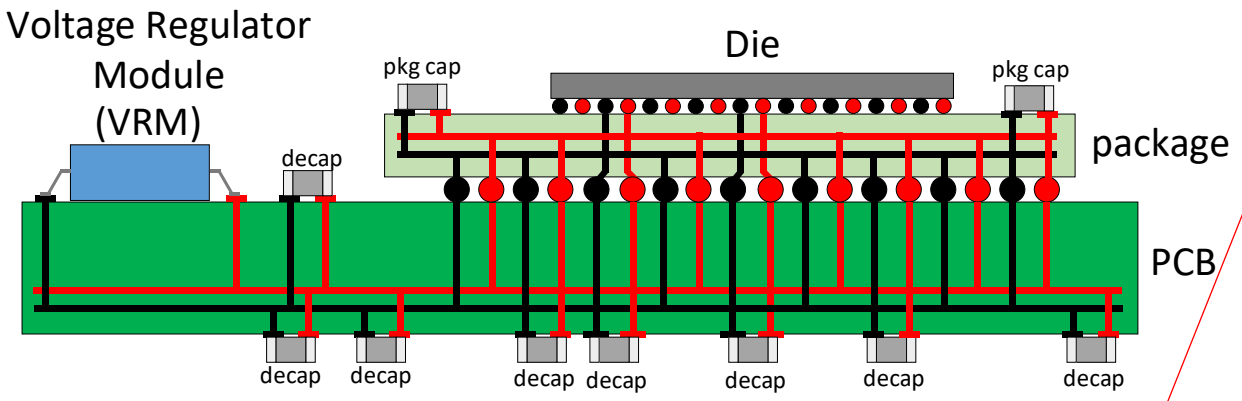


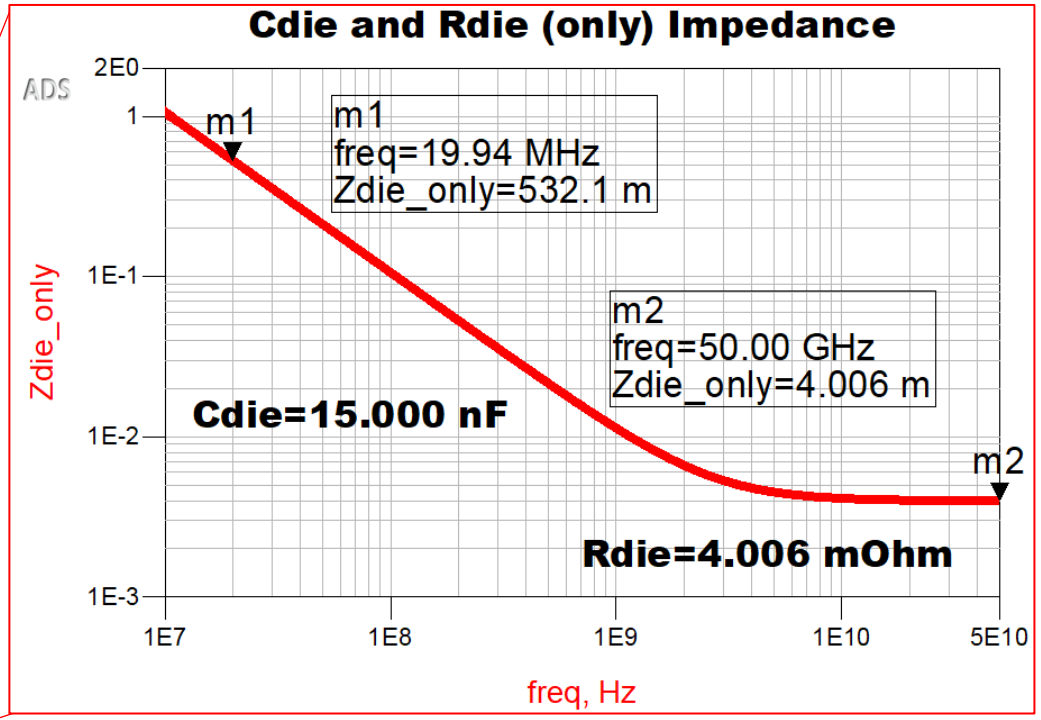


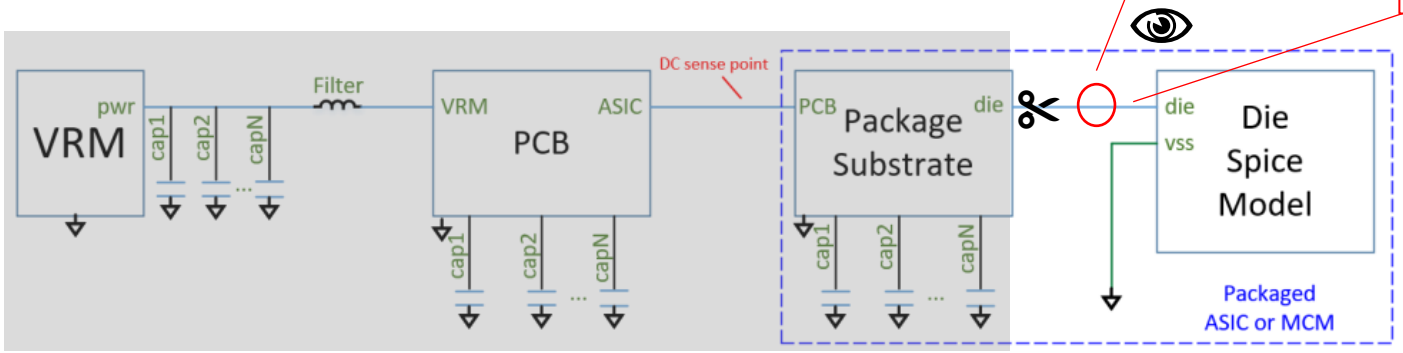


51% improvement in voltage ripple just by adjusting the Cdie of the die model

The die model only affects high frequency impedance of the PDN

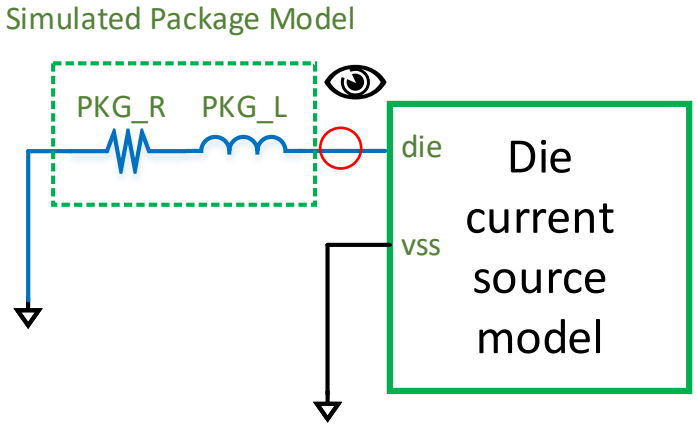


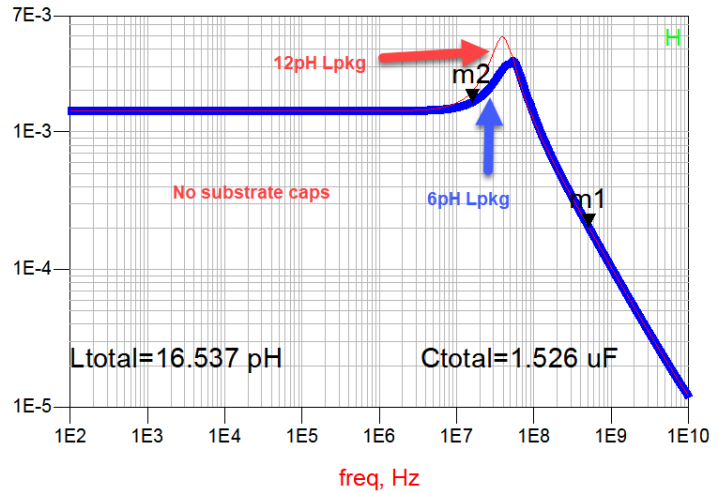




PDN Effects of the die model including the package

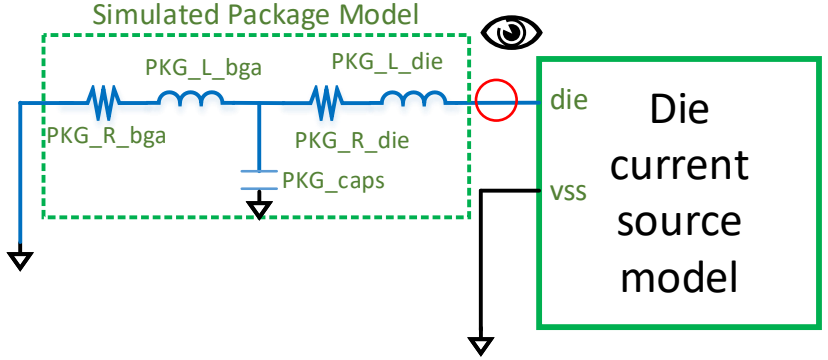
Package-die impedance curve without package substrate caps

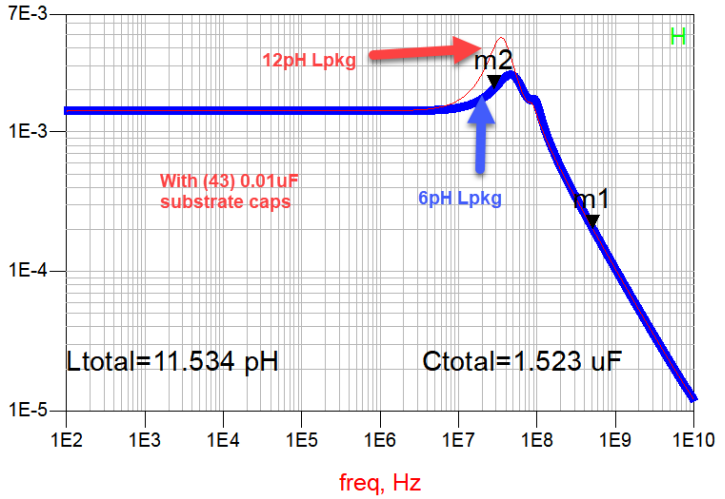




Inductance between the PKG & die limits the effectiveness of on-pkg capacitance

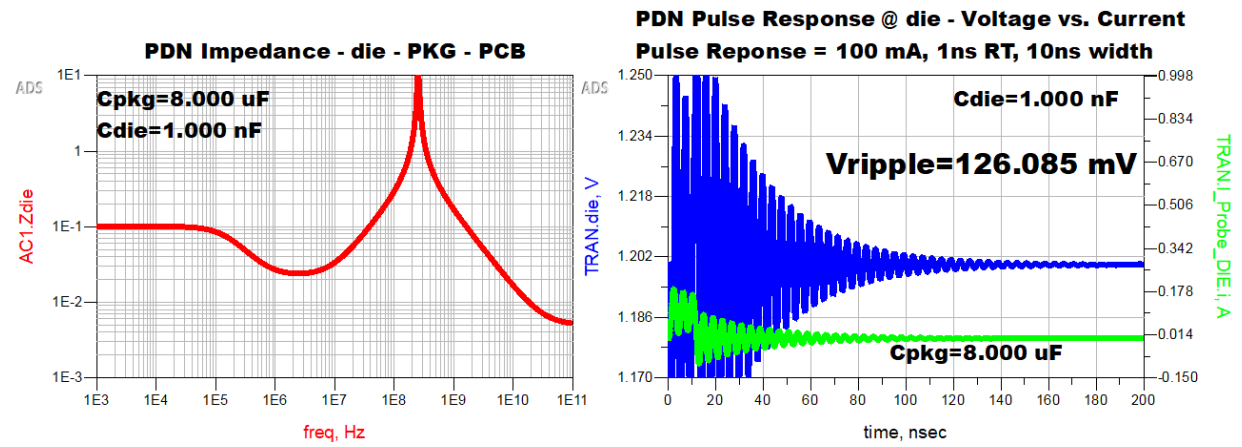
Package-die impedance curve including package substrate caps



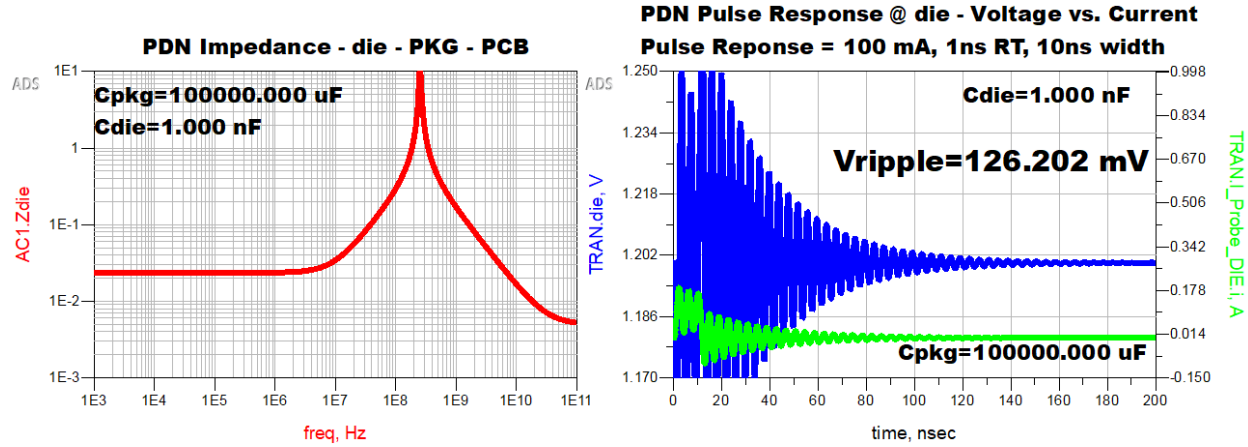


Why should we care about the Cdie?

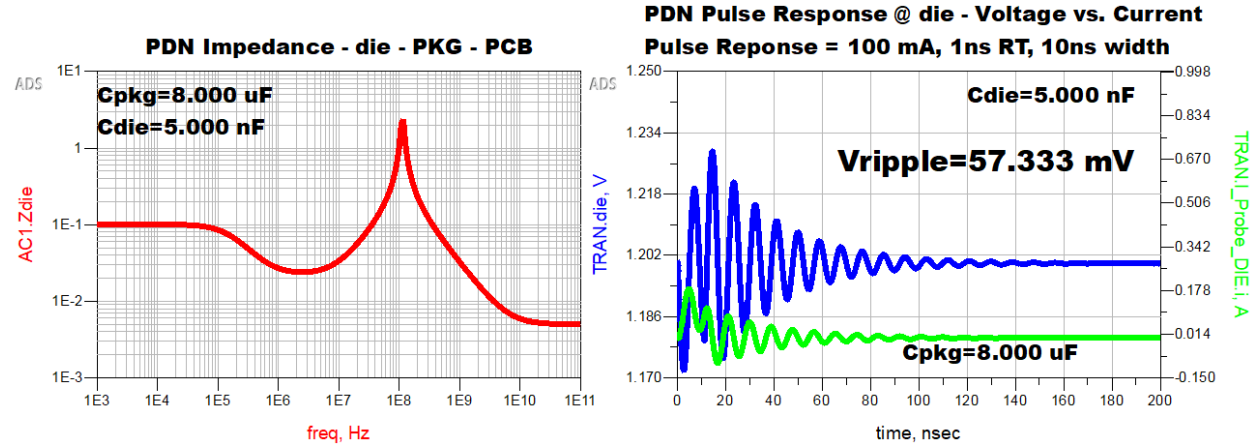
Cdie=1nF, Cpkg=8uF



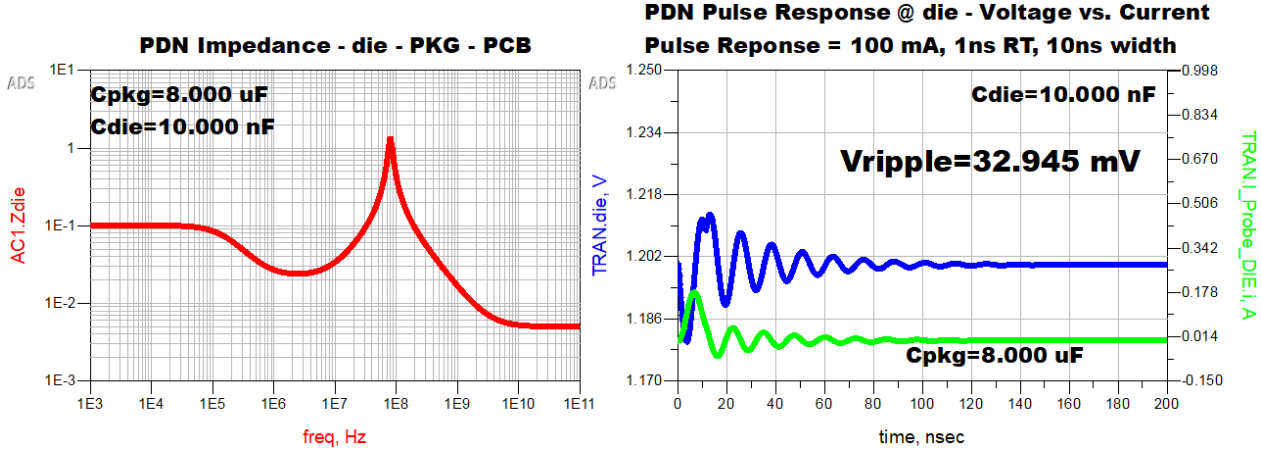
Cdie=1nF, Cpkg=100mF



Cdie=5nF, Cpkg=8uF



Cdie=10nF, Cpkg=8uF



Due to the inductance between the package and die, if Cdie is not enough to mitigate high frequency ripple, then no amount of on package capacitance can fix voltage ripple issues!

Power integrity case study

The DDR4 IP PHY vendor stated that their PHY had to meet the following AC voltage specs:

- 30mV Ripple (> F_{clk})
- 150mV Ripple (< F_{clk})

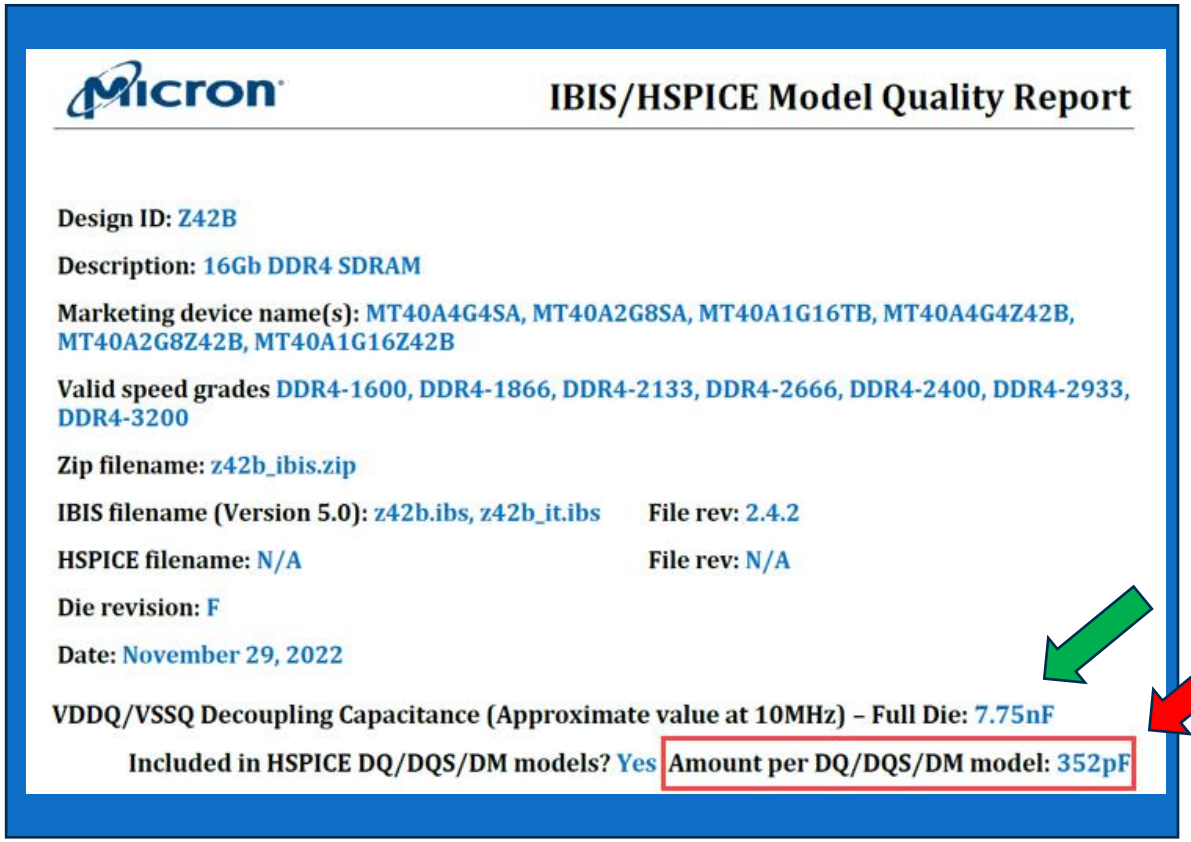
The DDR4 PHY die model provided from the vendor initially had the following specs:

- Cdie = 3.29 nF
- Rdie = 4.23 mΩ

Note: F_{clk}=1.2 GHz for DDR4-2400

How do you know if a die model from a vendor is correct?

Most ASIC IP vendors provide a quality report



Micron — IBIS/HSPICE Model Quality Report

Design ID: Z42B

Description: 16Gb DDR4 SDRAM

Marketing device name(s): MT40A4G4SA, MT40A2G8SA, MT40A1G16TB, MT40A4G4Z42B, MT40A2G8Z42B, MT40A1G16Z42B

Valid speed grades DDR4-1600, DDR4-1866, DDR4-2133, DDR4-2666, DDR4-2400, DDR4-2933, DDR4-3200

Zip filename: z42b_ibis.zip

IBIS filename (Version 5.0): z42b.ibs, z42b_it.ibs File rev: 2.4.2

HSPICE filename: N/A File rev: N/A

Die revision: F

Date: November 29, 2022

VDDQ/VSSQ Decoupling Capacitance (Approximate value at 10MHz) – Full Die: 7.75nF

Included in HSPICE DQ/DQS/DM models? Yes Amount per DQ/DQS/DM model: 352pF

Source: micron.com

Comparing our DDR4 PHY die vs. a Micron SDRAM

Initial vendor Cdie model

ASIC PHY VDDQ/VSSQ Decoupling Capacitance – Full Die: **3.29 nF**

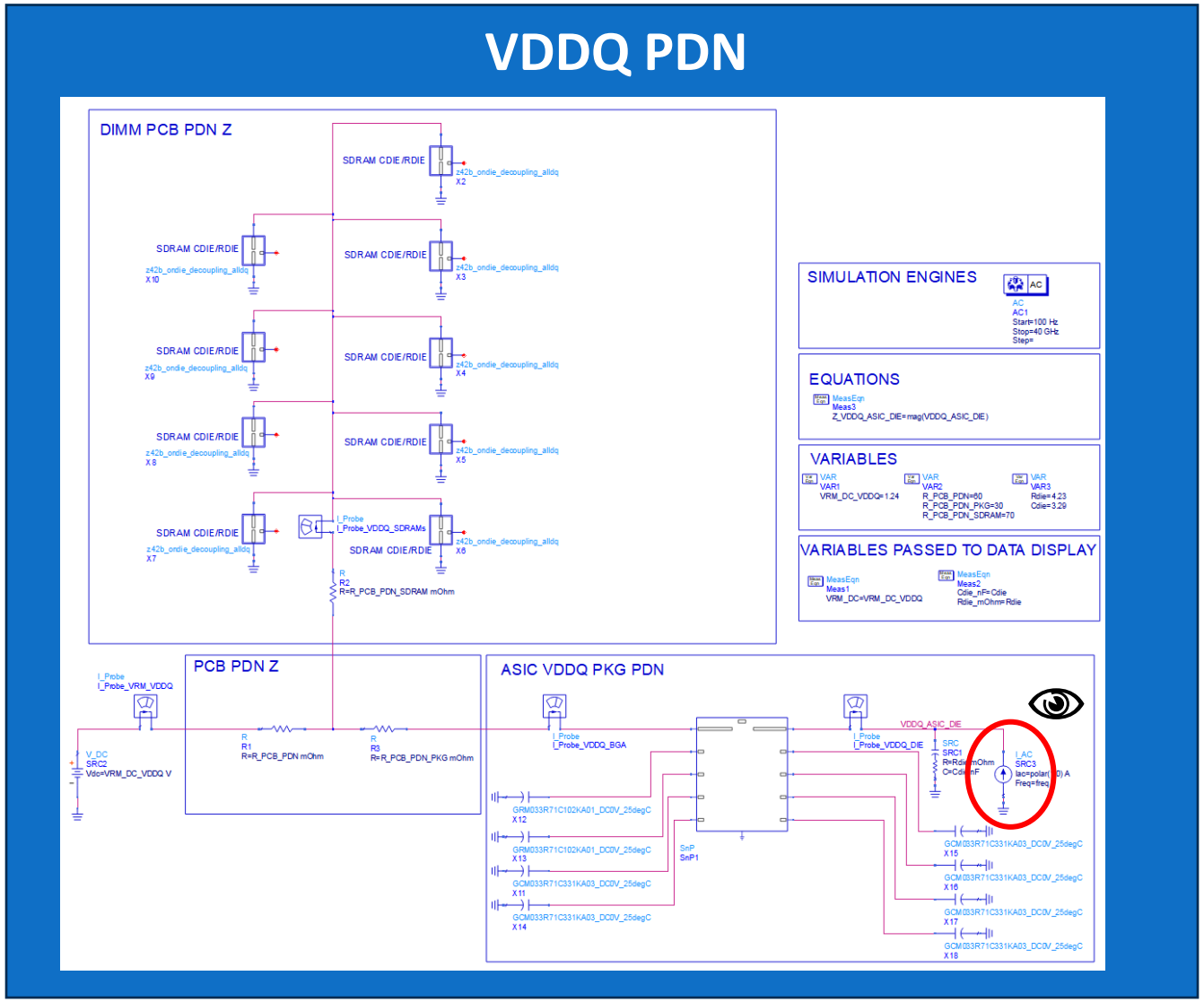
Amount per DQ/DQS/DM model = **33.23 pF**

The Micron x16 SDRAM has 2X the amount of Cdie in the comparison to a memory controller (DDR4) for all x72 DDR4 nets.

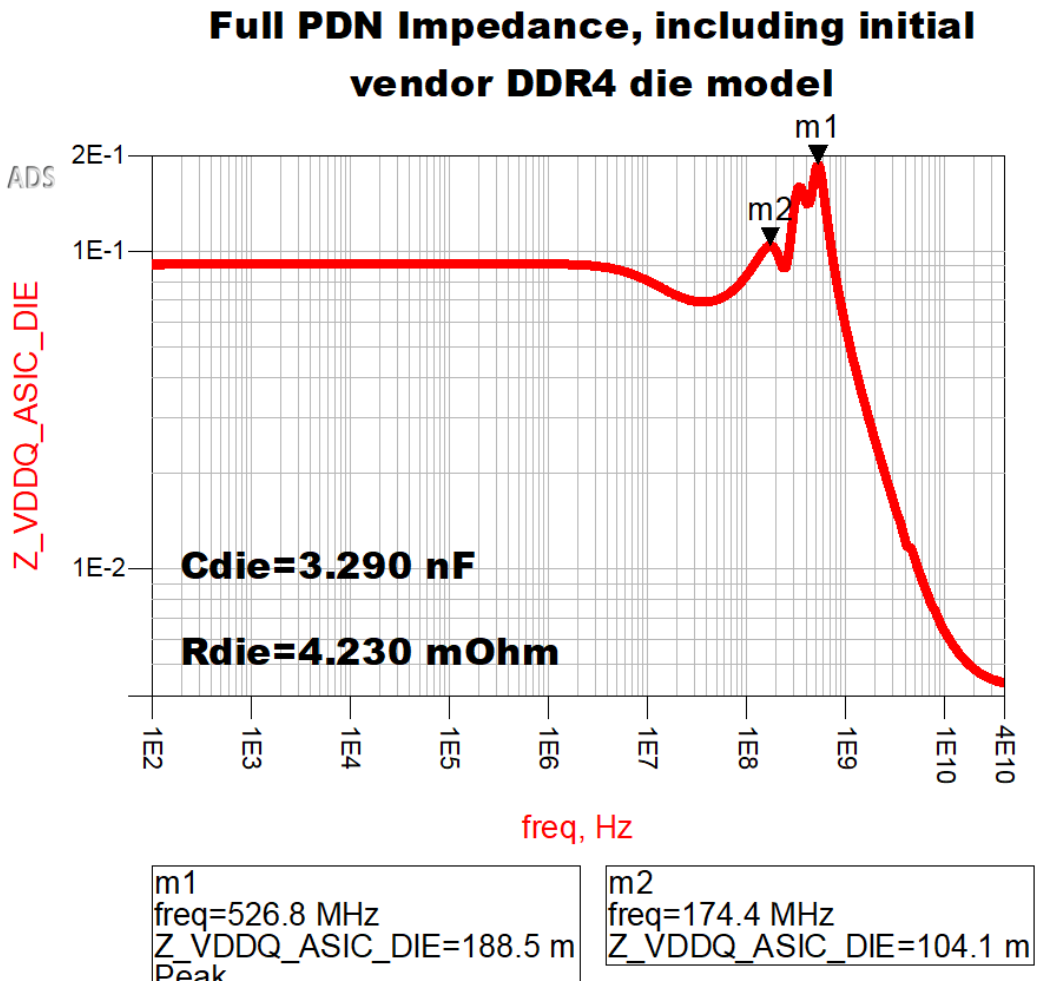
The amount of capacitance per DQ/DQS/DM is 10x less for the memory controller (DDR4 PHY) vs. the Micron SDRAM

Full VDDQ PDN Impedance with DDR4 PHY and SDRAM

With Cdie = 3.29nF



Matched PCB and VRM output impedance set to 90 mΩ



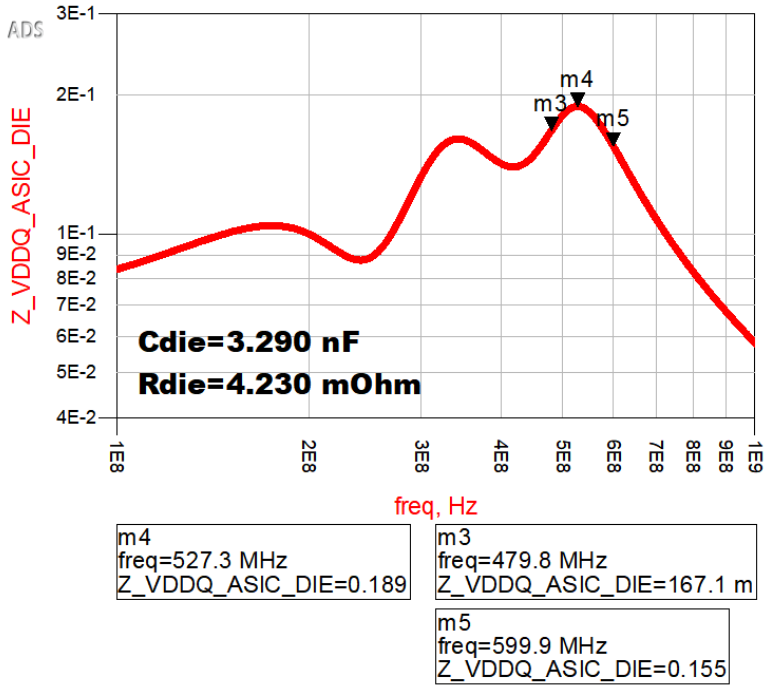
Worst-case impedance peak at marker m1

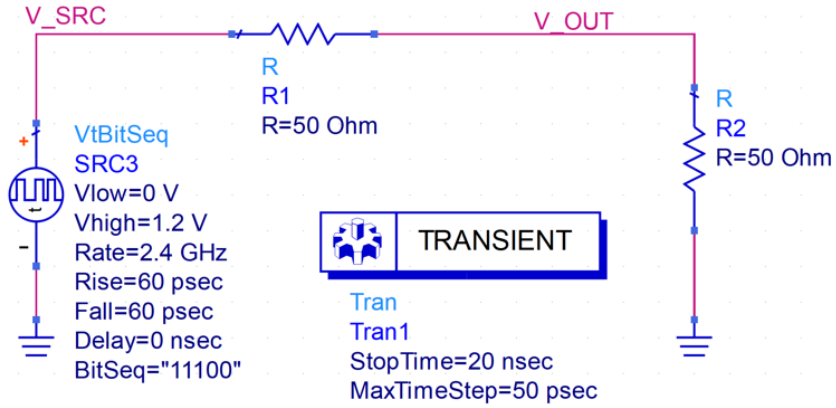
Determining worst-case excitation test pattern

With Cdie = 3.29nF

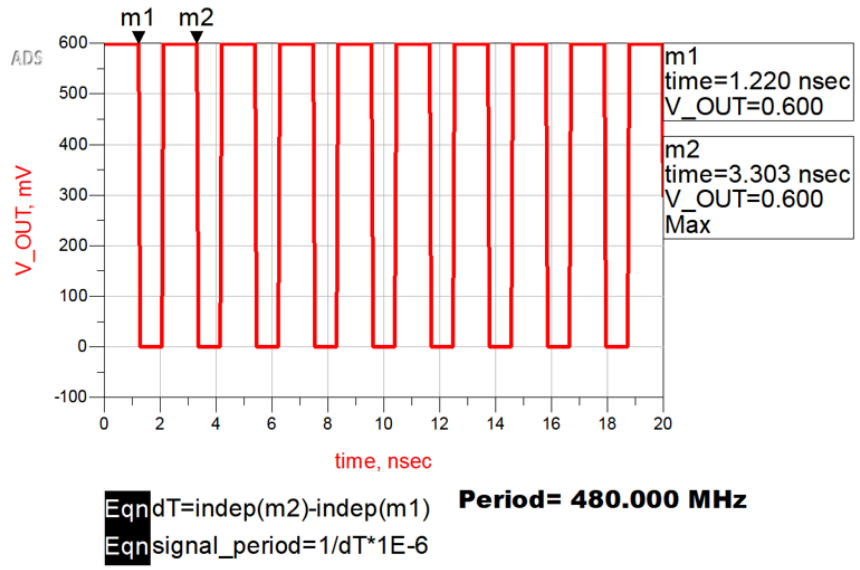
A worst-case PDN stimulus is used to test the robustness of the system PDN.

Full PDN Impedance (ZOOMED IN)
VDDQ Impedance at ASIC die





480 MHz Excitation Bit Pattern
BIT SEQUENCE = "11100"



- "1100" bit pattern would yield a 600MHz (marker m5) excitation period
- 480MHz (marker m3) is closer to the worst-case impedance point
- A 480MHz excitation period with a "11100" repeating bit sequence is used since this is the worst-case excitation pattern

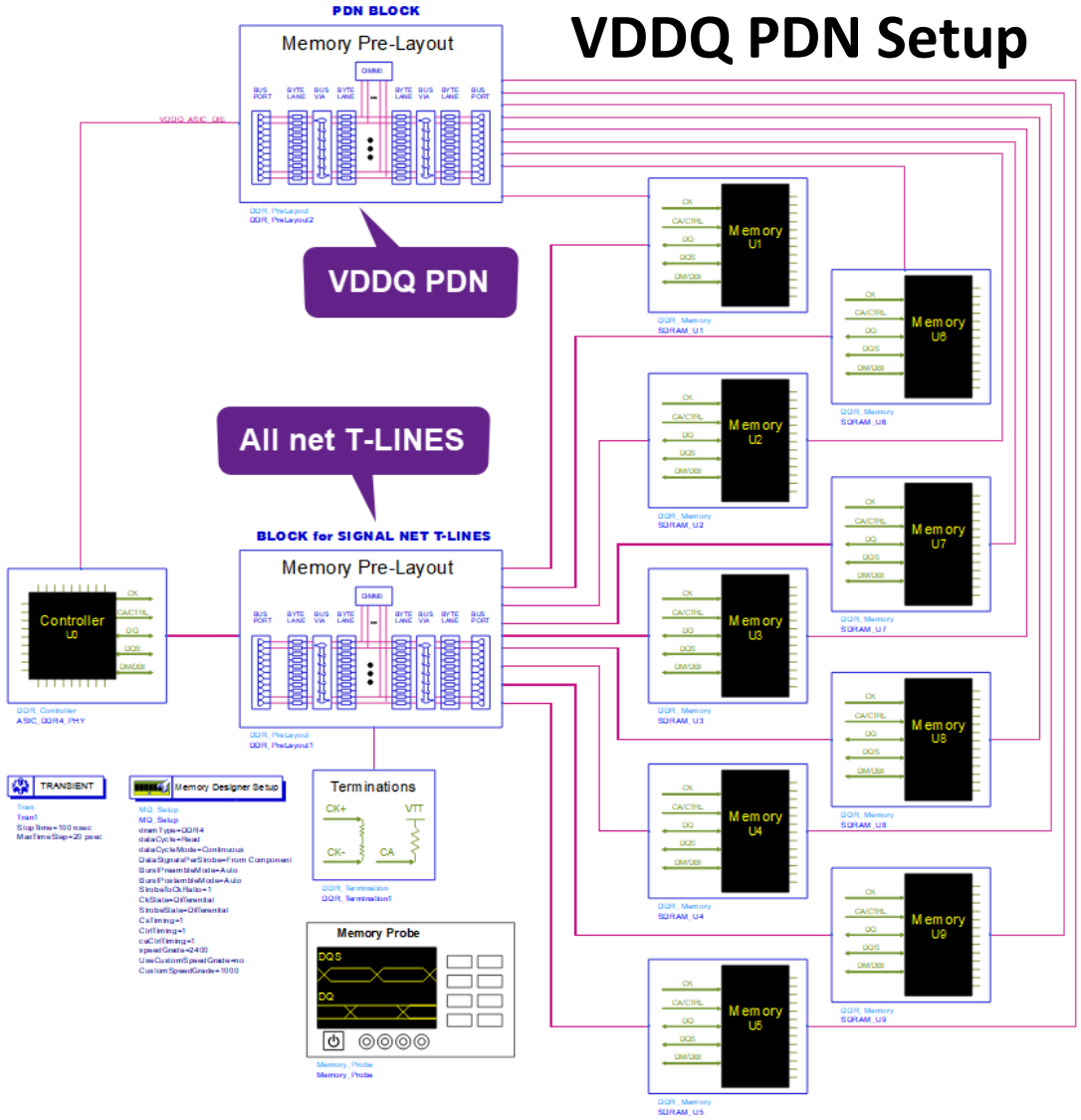
DDR4-2400 Read Simulation Setup with DDR4 PHY and 9 SDRAM

480MHz Excitation Pattern

- The setup shown includes 9 Micron SDRAM IBIS models
- All ODT settings are set to 48Ω at the ASIC
- All DQ/DM/DQS and CAC net drive strengths are set to 48Ω
- The VTT voltage is set to 0.6V
- All CAC nets are running a repeating "1010" pattern

Excitation pattern for DQ bits is set to “11100”

VDDQ PDN Setup

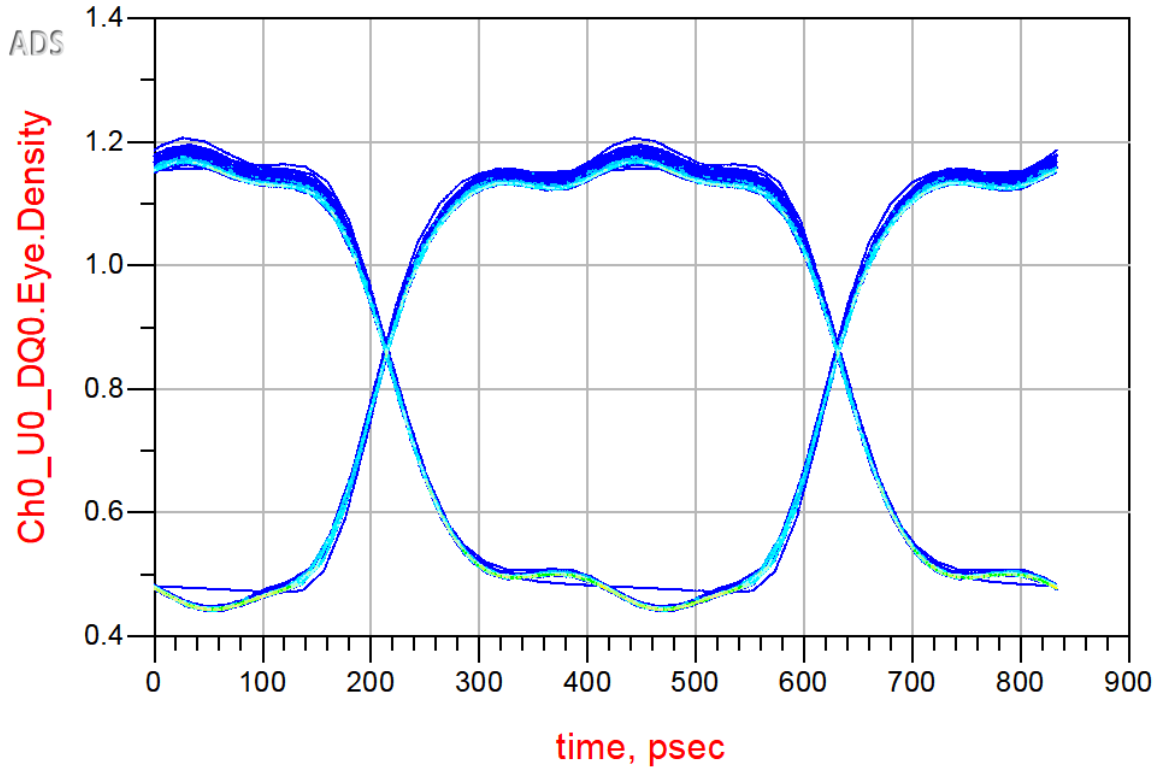


Simulation setup for DDR4-2400 data rate. All DQ/DM/DQS are loaded with 48 Ω T-lines.
All CAC nets are loaded with a fly-by T-line.

DDR4-2400 Read Simulation Results with DDR4 PHY and 9 SDRAM

480MHz Excitation Pattern and Cdie = 3.29nF

DQ[0] at Memory CTLR



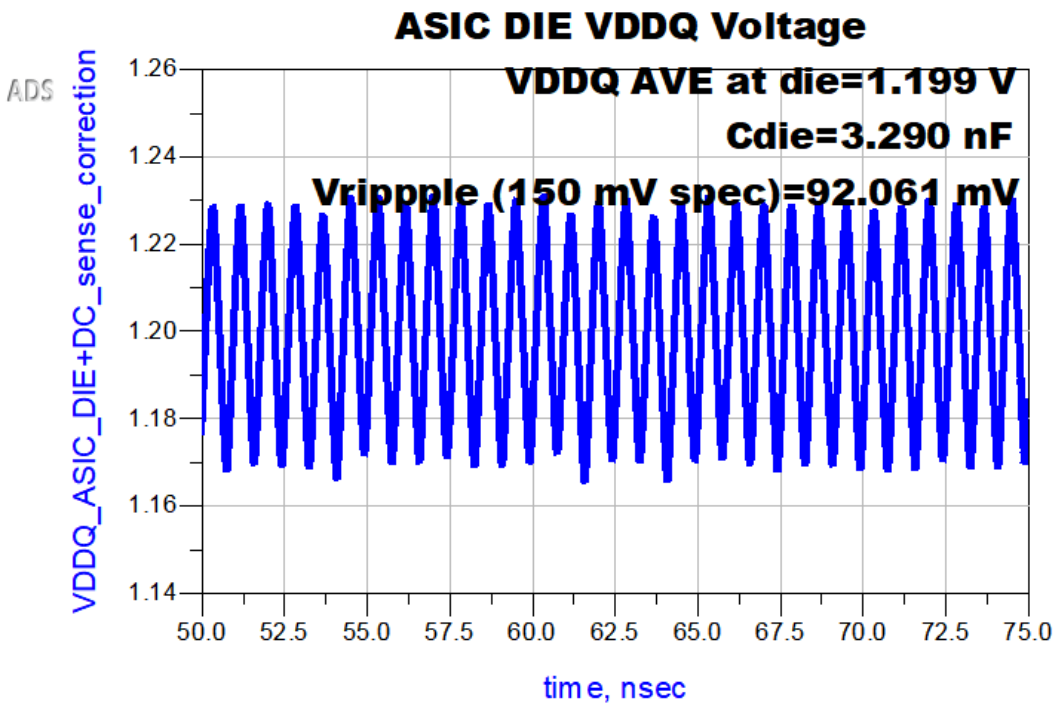
All DQ/DM/DQS and CAC nets had open eyes similar to what is shown here

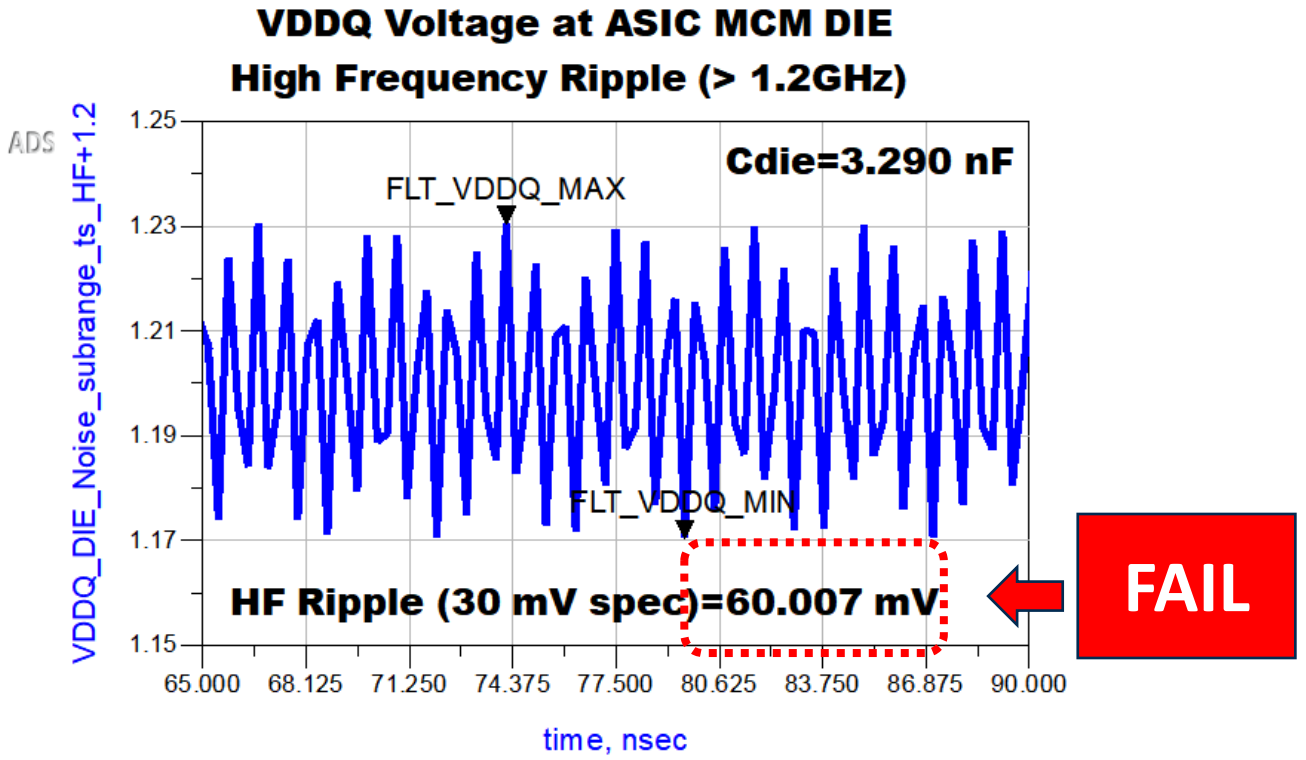
Eye looks open and passing. However, this assumes power rail ripple spec is met

Time Domain Results – DDR4-2400 READ

With 480MHz Excitation Pattern and Cdie = 3.29nF

ALL IBIS CORNERS = MAX





FAIL

According to the vendor, this should pass. So why doesn't it?
Answer: The die model does not seem correct

What do you do if you think the die model from a vendor is inaccurate?

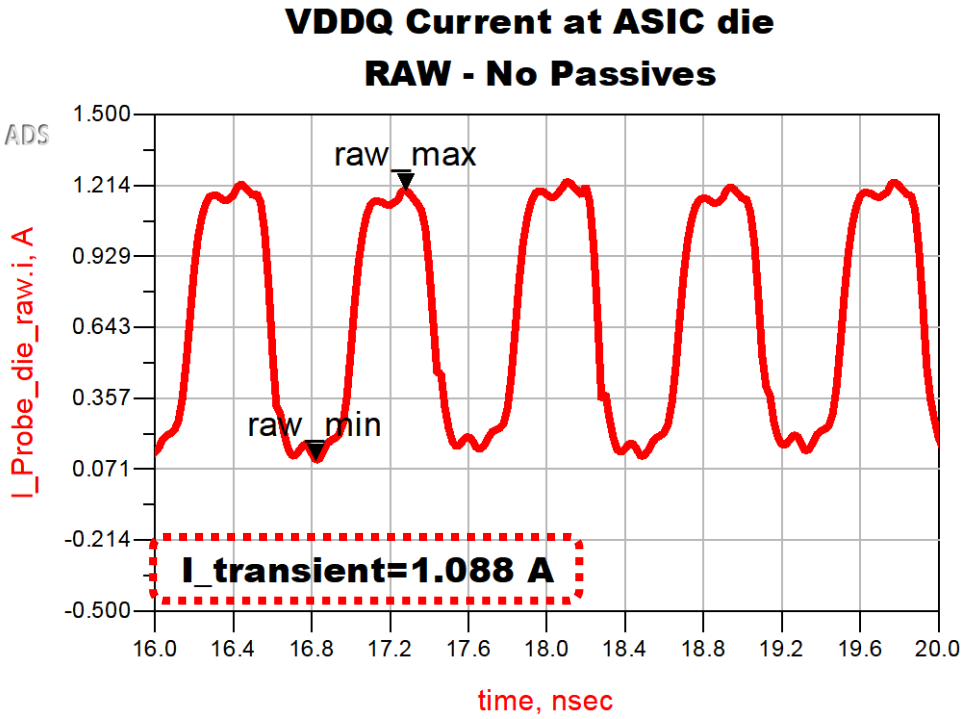
- Check the die model fidelity
- Keep in mind, most ASIC IP vendors specify their compliance point to the die bumps. On-die capacitance is critical to managing and reducing PDN for the circuits at the die.

How to determine minimum Cdie

For DDR4-2400:

- f_{clk} = 1.2 GHz
- ΔV=30 mV
- $\Delta I = 4/\pi \cdot I_{transient} \approx 1.4$ A

Determining $I_{transient}$ →



ALL IBIS CORNERS = MAX

4/π comes from Fourier transform of a square wave [5]

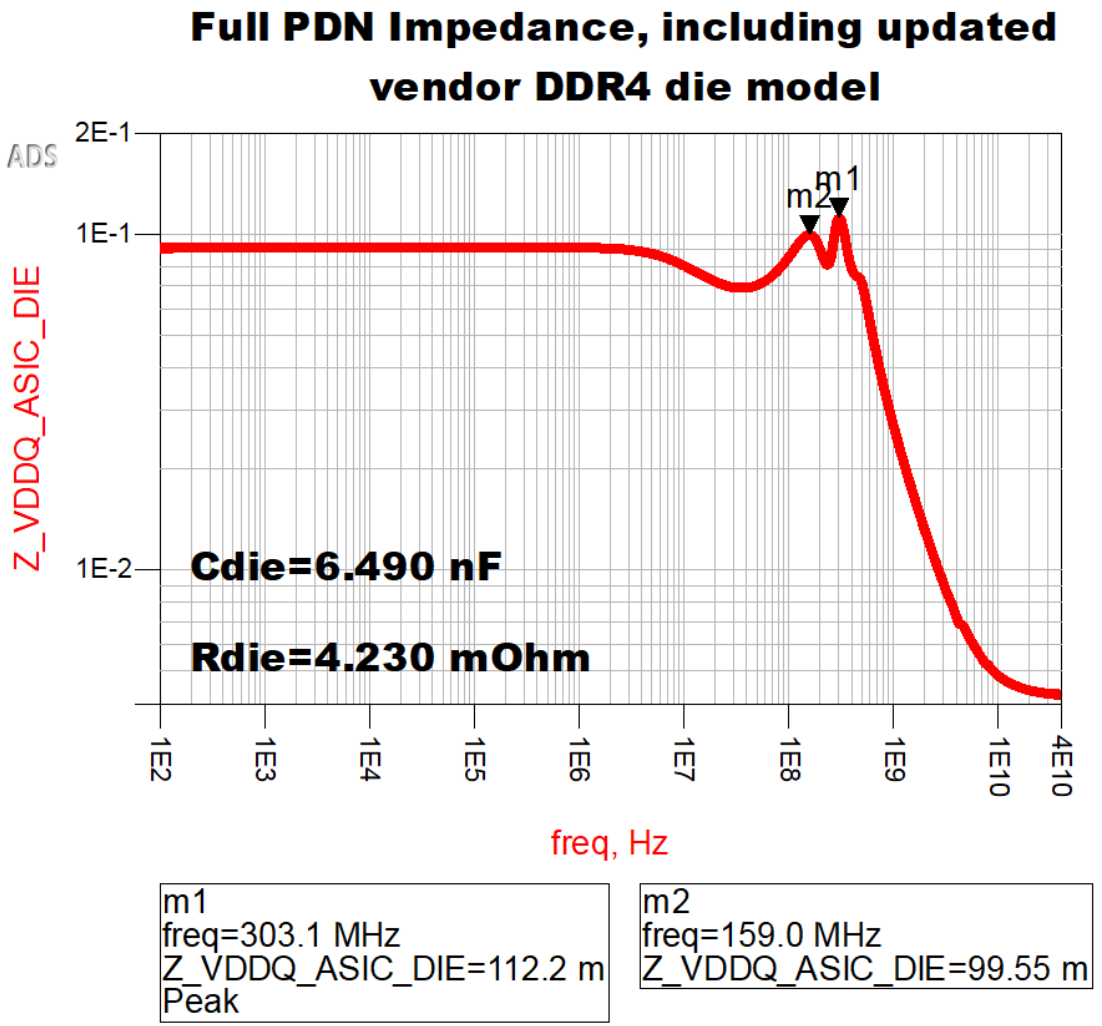
$$Z_{TGT\ (min)} = \frac{\Delta V}{\Delta I} = \frac{30\ mV}{1.4\ A} = 21.4\ m\Omega$$

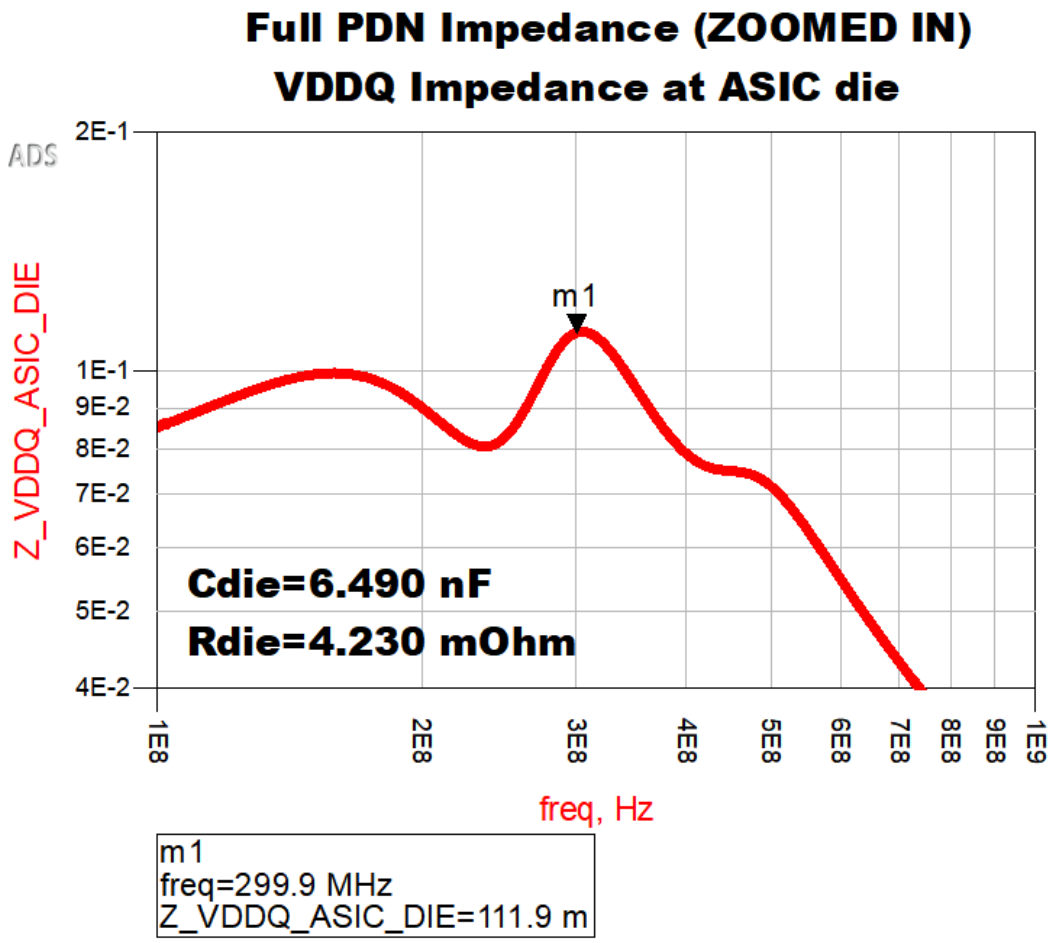
$$C_{die}(min) = \frac{1}{2 \cdot \pi \cdot f_{clk} \cdot Z_{TGT(min)}} = \frac{1}{2 \cdot \pi \cdot 1.2\ GHz \cdot 21.4\ m\Omega} > 6.19\ nF$$

This indicates Cdie must be greater than 3.29nF

Updated VDDQ PDN Impedance with DDR4 PHY and SDRAM

With Cdie = 6.49nF

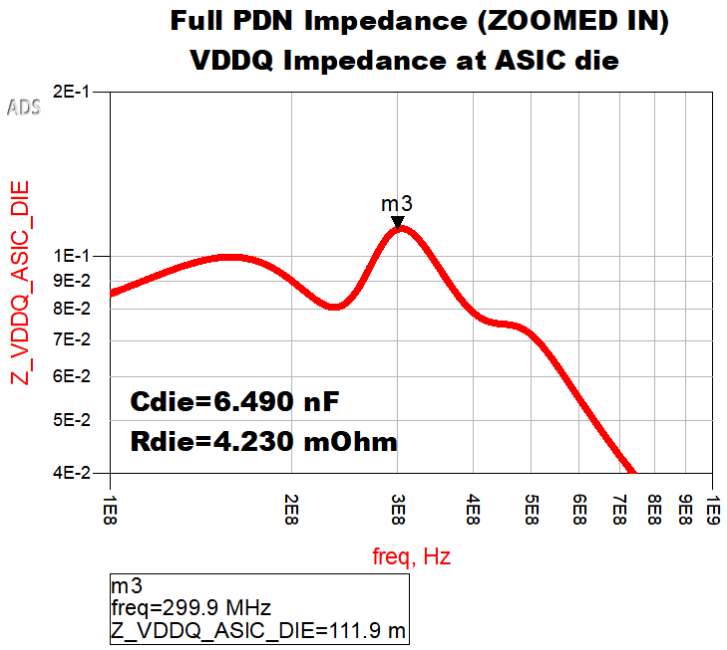


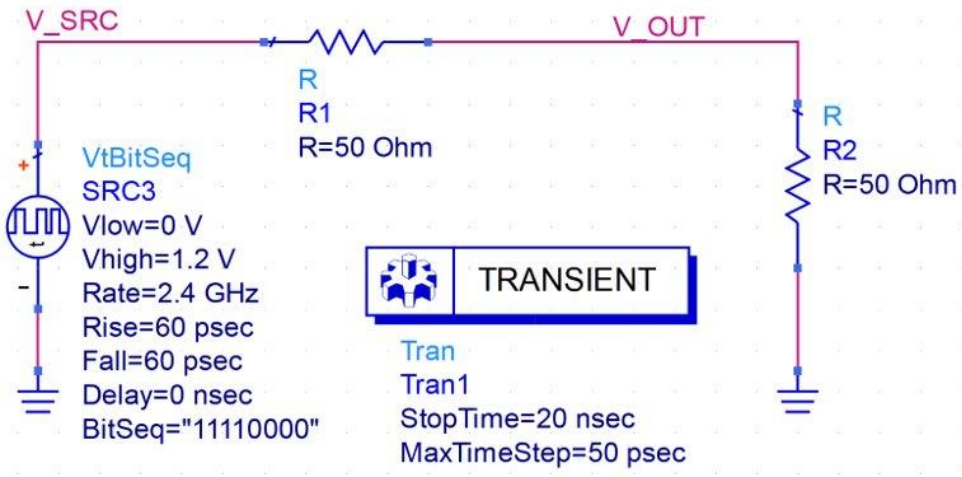


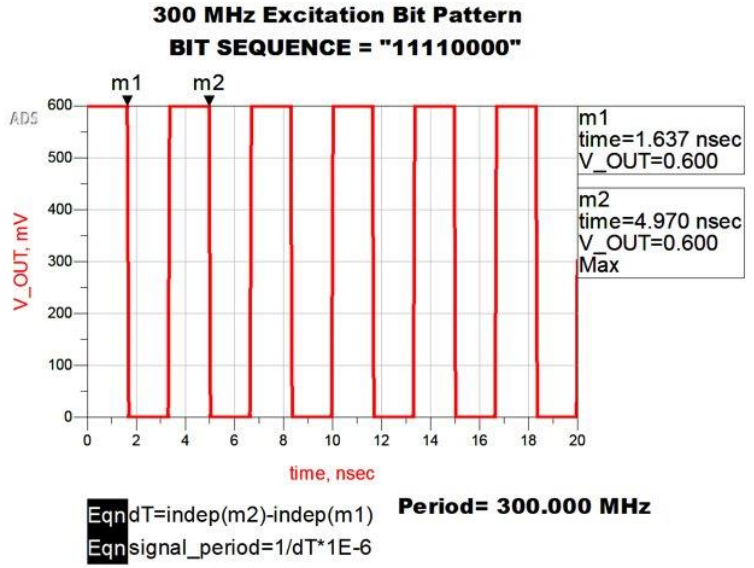
Worst-case impedance peak at marker m1

Determining worst-case excitation test pattern

With Cdie = 6.49nF







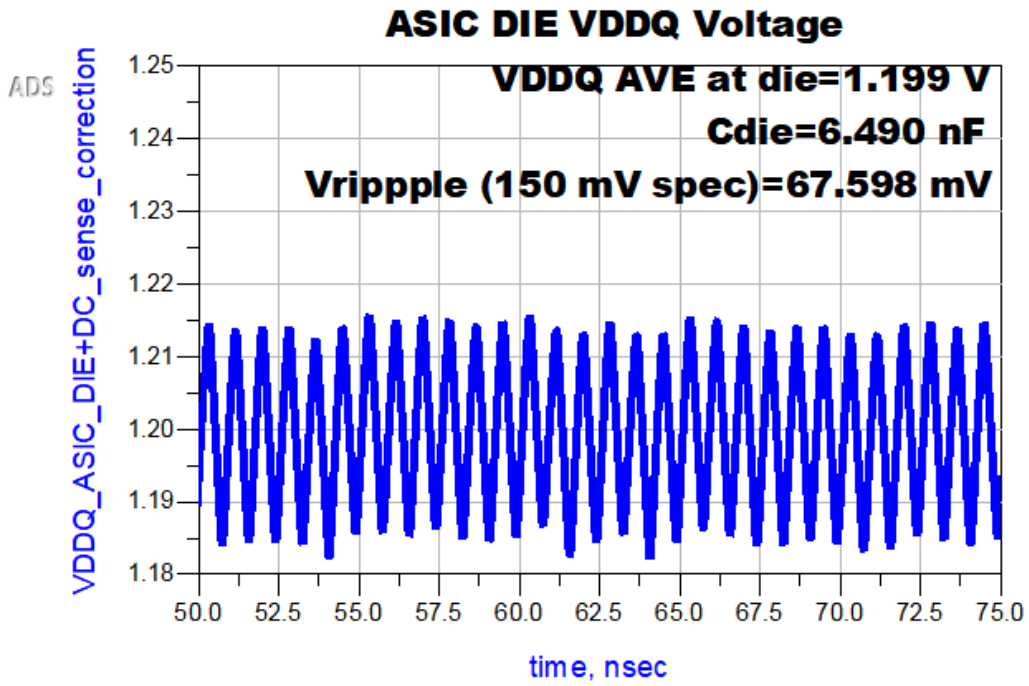
A “11110000” repeating bit pattern yields a 300MHz excitation period, which matches the peak at marker m3, and excites our PDN with the worst-case bit pattern.

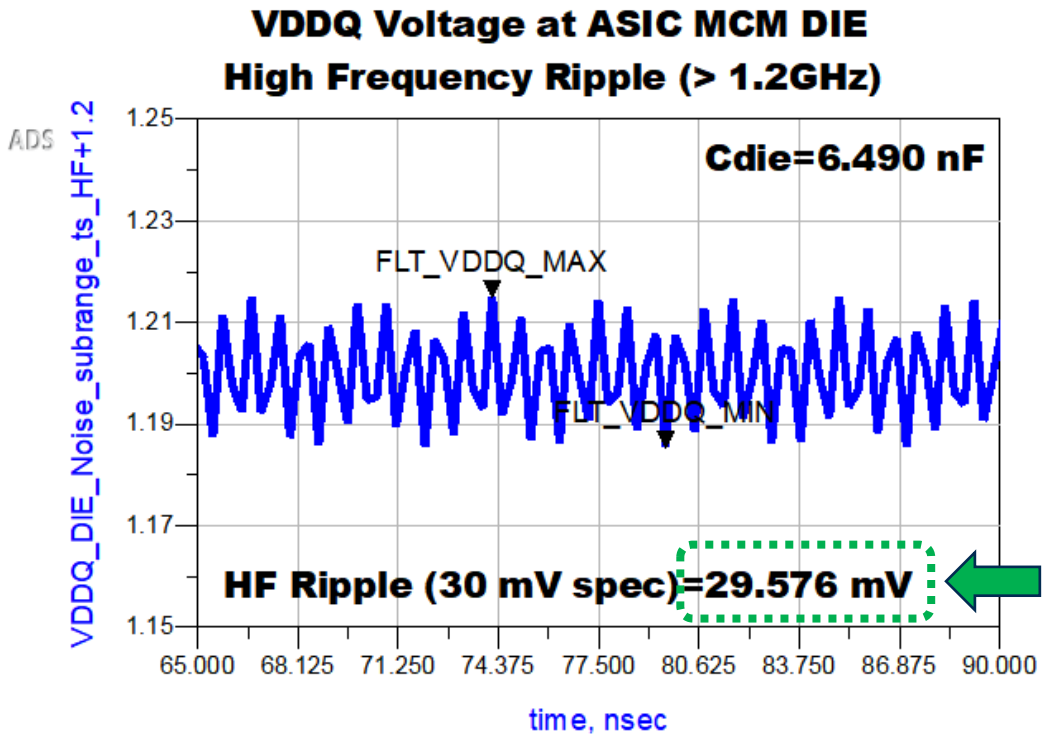
Updated Time Domain Results – DDR4-2400 READ

With 300MHz Excitation Pattern – Cdie = 6.49nF

Now let's check the results at with updated vendor Cdie

ALL IBIS CORNERS = MAX





PASS

With Cdie = 6.49 nF, a 51% reduction of HF ripple is observed. And the HF ripple spec (30mV) is now met

Call to Action

- IP vendor later confirmed they gave us an incorrect Cdie value
  - The correct Cdie value for this DDR4 PHY is 6.49nF at the worst-case corner, very close to the calculated 6.19nF
  - A new model was provided by the vendor.
- ***Hold IP vendors accountable! Ask for quality reports***

"**Power integrity is the science of getting power to the devices that it likes**. Our job in power integrity is to ensure we have optimized the power for the devices that we are powering so that they can work at their peak performance." – Steve Sandler, Picotest.com

Summary and Conclusions

- Don’t always trust the models you get from vendors! Vendor models are not always correct.
- When integrating IP from another vendor on your ASIC, ask the IP vendor to confirm what the Cdie value is for each IP power domain
  - Ask for quality report
  - Ask for manual calculation for total capacitance on each power domain ($C=Dk \cdot \varepsilon 0 \cdot A/D$)
    - The foundry tech file provides the dielectric constant (Dk)
    - The mimcap area (A) or capacitors per layer area is known
    - Distance between layers (D) is known
    - Total capacitors per power domain is known -> manually calculate expected Cdie
  - The model impacts both the PDN noise and timing jitter. An accurate model allows verification of both

“**Power integrity is all about the quality of power (& noise) seen by the circuits on the ASIC die**.”
– Larry Smith and Dr. Eric Bogatin - Principals of Power Integrity for PDN Design

Thank You for Attending

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