How Power Integrity is Changing the World of Power Electronics

Heidi Barnes, Keysight Technologies
Steve Sandler, Picotest
Benjamin Dannan, Signal Edge Solutions

Tutorial Session S12 – Sunday March 19th
2:30pm to 6pm

Speakers

Steve Sandler

Managing Director, Picotest

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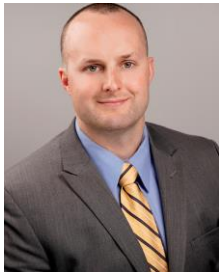
Steve Sandler has been involved with power system engineering for more than 40 years. The founder and CEO of Picotest.com, a company specializing in instruments and accessories for high-performance power system and distributed system testing



Benjamin Dannan

Chief Technologist, Signal Edge Solutions

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Benjamin Dannan is a Chief Technologist and an experienced signal and power integrity (SI/PI) design engineer, advancing high-performance ASICs and high-speed digital designs. He is a Keysight ADS Certified Expert with numerous publications on SI/PI-related topics and received the prestigious DesignCon best paper award in 2020.

Heidi Barnes

Power Integrity Applications, Keysight Technologies

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Senior Application Engineer in the PSS EDA Group of Keysight Technologies. Her recent activities include the application of electromagnetic, transient, and channel simulators to solve signal and power integrity challenges. Author of over 20 papers on SI and PI and recipient of the DesignCon 2017 Engineer of the Year.

AGENDA

Introductions

Power Integrity Basics – VRM + PDN + Digital Load

presented by Heidi Barnes

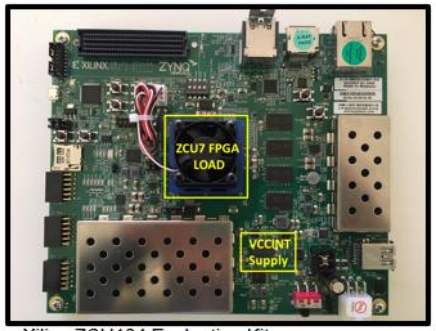
Measurement Based VRM Modeling

presented by Steve Sandler

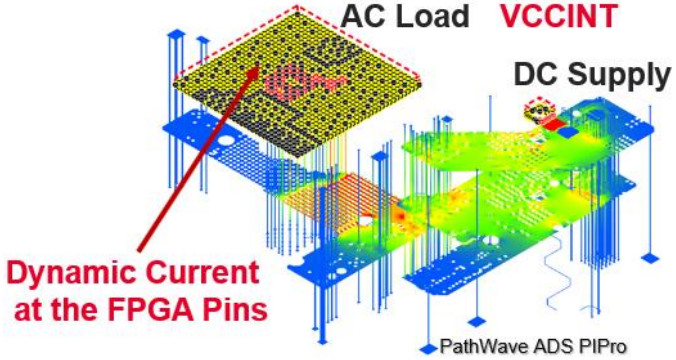
Building a Power Delivery Digital Twin - TI TPS7H4003 SSAM Case Study

presented by Benjamin Dannan

Power Rail Noise Ripple is Not Intuitive



Xilinx ZCU104 Evaluation Kit



DesignCon 2020

A Method for Dynamic Load Current Testing with a Benchtop Power Supply

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Steve Sandler, PICOTEST.com
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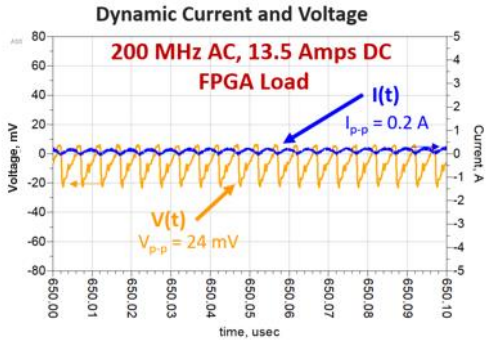
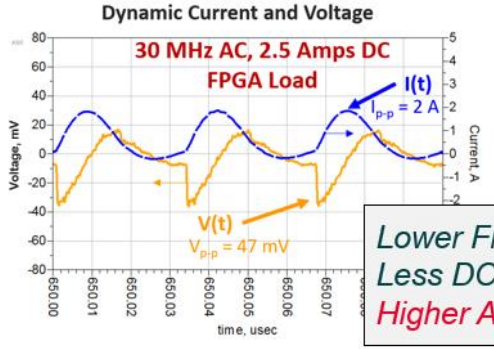
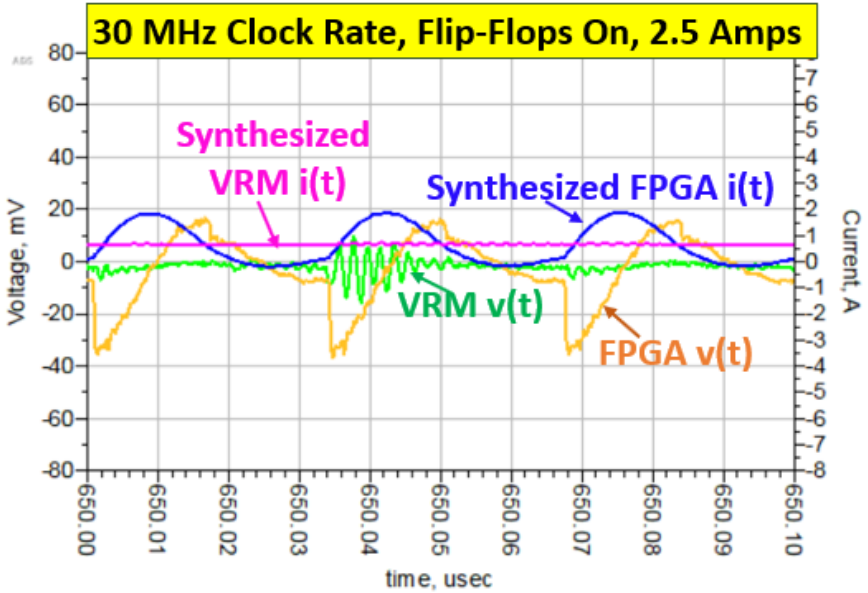


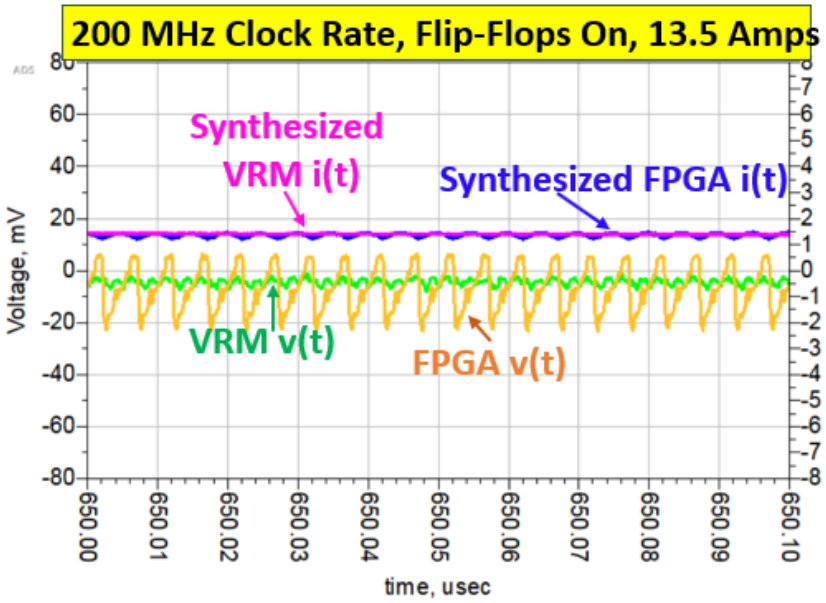


Lower Frequency
Less DC Current
Higher AC Noise!

Power Rail Dynamic Voltage and Current Ripple

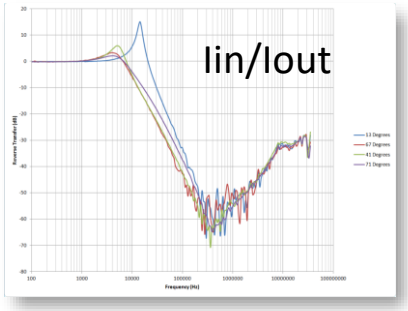
The Ultimate Digital Twin: Measurement Enabled Simulations



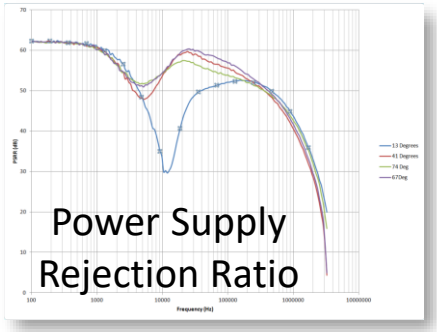


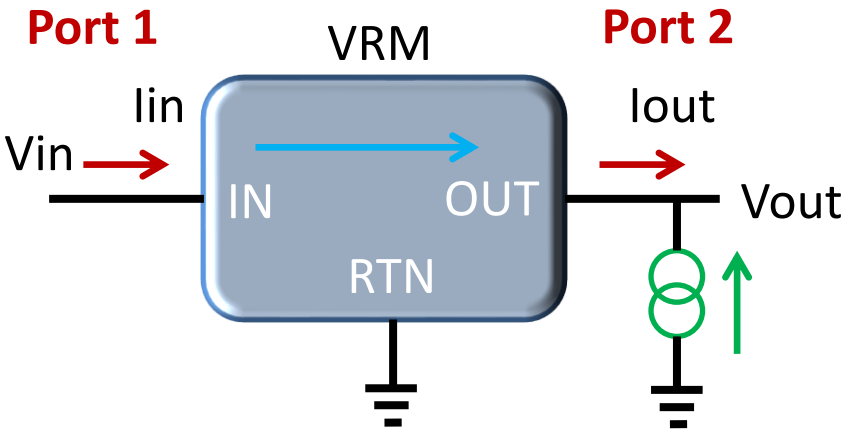
The Voltage Regulator Module (VRM) needs to consider ALL noise sources (large and small signal EMI)

Reverse Transfer - (S12)



PSRR - (S21)



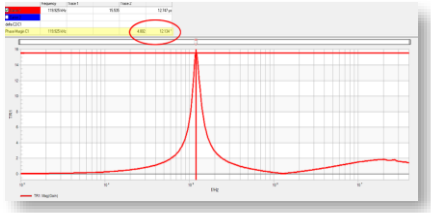


Input Impedance - (S11)

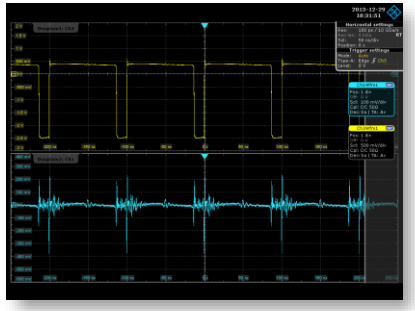
Input impedance can be NEGATIVE!

An R-L model only considers the output impedance

Output Impedance - (S22)



Output Noise/Spikes

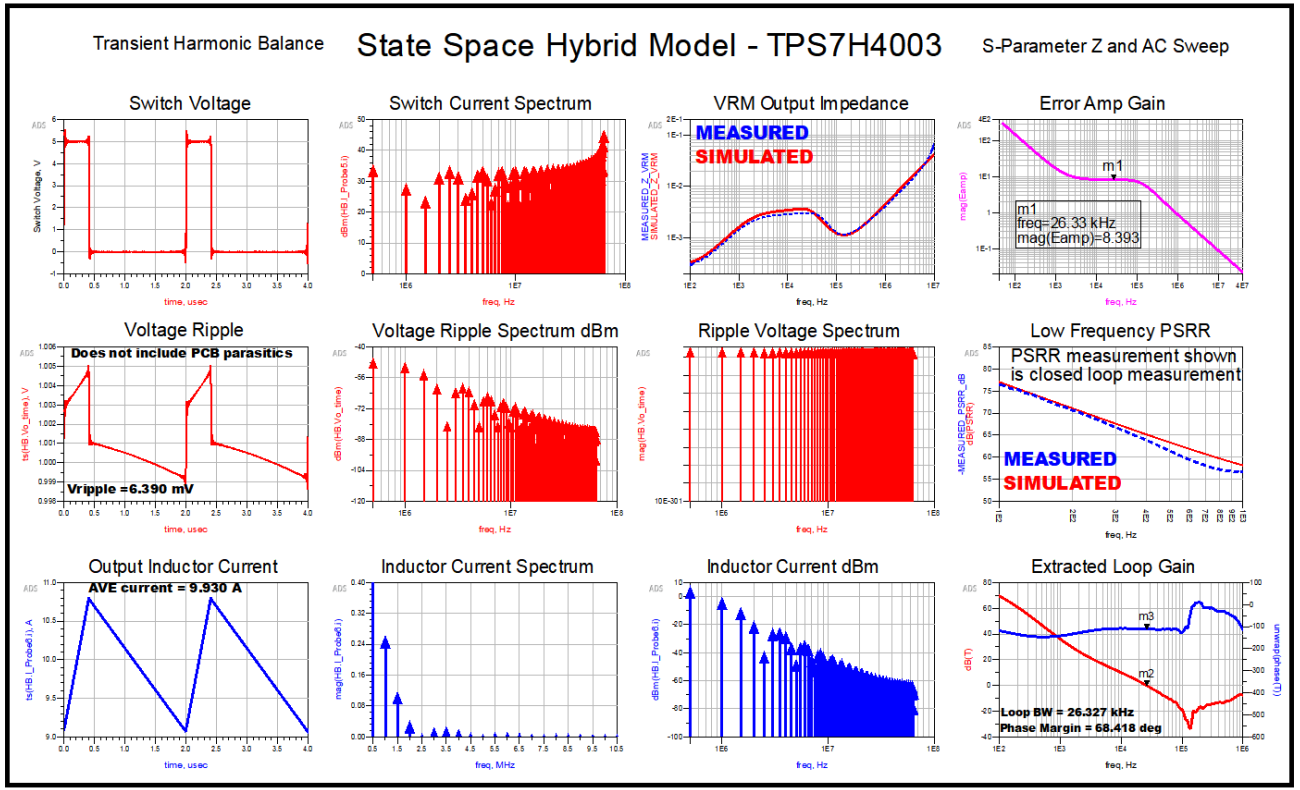


TPS7H4003 State-Space Average VRM Model Example

Does not include PCB effects

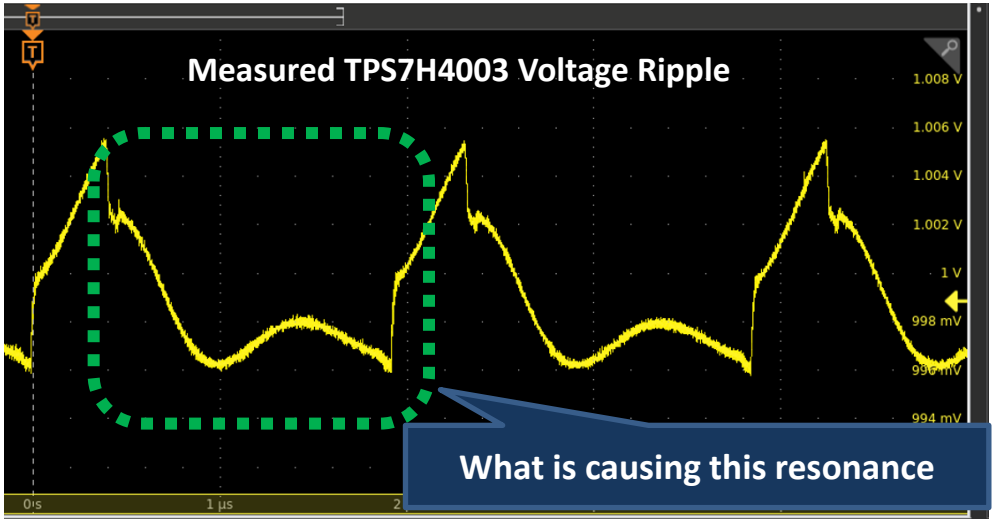
Simulation matches measurement…
Model is good!

We're finished!
Or are we?

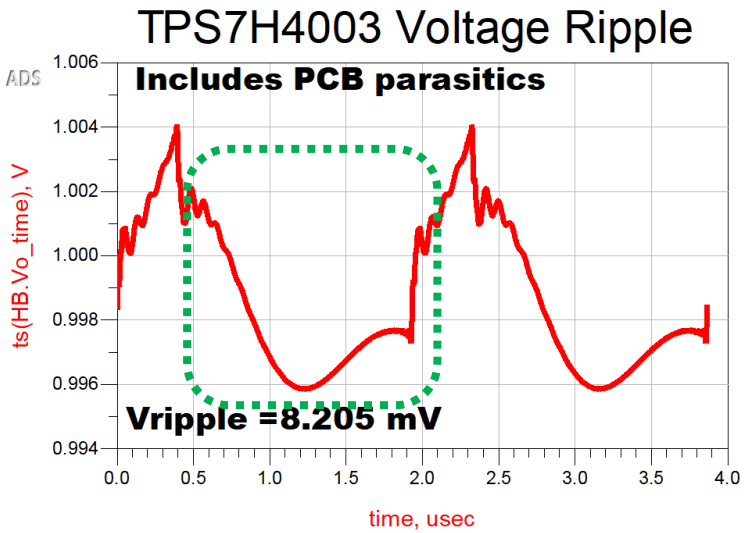


TPS7H4003 VRM Output Voltage Ripple

Measurement vs. Simulation with included PCB effects

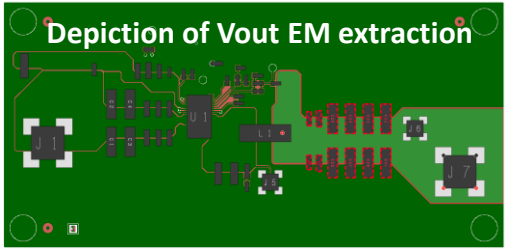


Simulated TPS7H4003 Voltage Ripple using State-Space Average VRM Model



All extracted PCB artwork was from Keysight PathWave PIPro

Extracted PCB Artwork, the extracted Switch node is not depicted



APEC

S12: How Power Integrity is Changing the World of Power Electronics

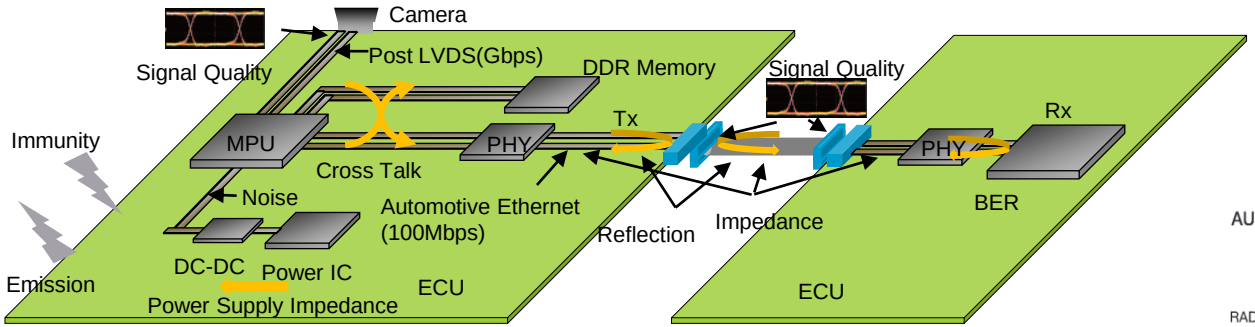
Power Integrity Basics: VRM + PDN + Digital Load

Speaker:

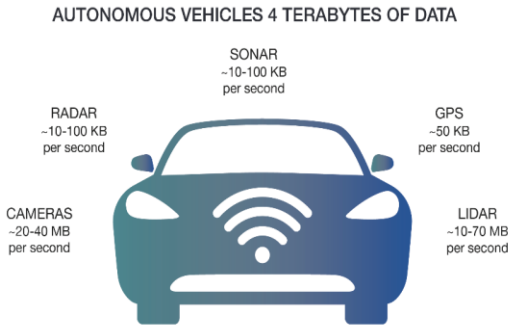
Heidi Barnes, Keysight Technologies

SI is the Goal, PI is the Foundation

PI is not DC - Fast delivery of power at microwave frequencies



Key Take Away:
Power Integrity Engineers need RF/uW design and measurement tools!



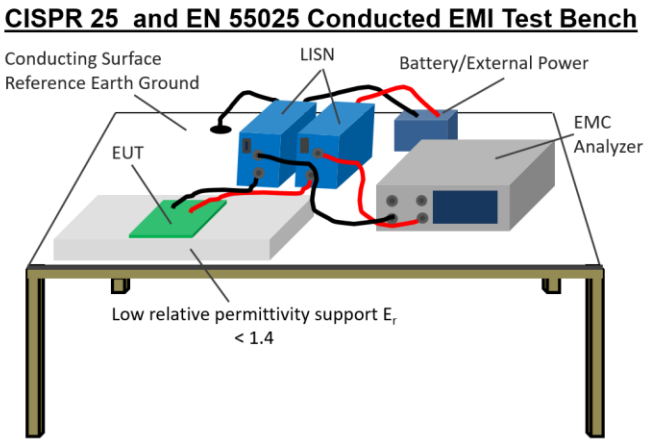
Power Delivery Eco-System

- Many Point-of-Load power supplies
- Low Voltage, High $\frac{dI}{dt}$ Switching Loads
- Target Z to reduce broadband $L\frac{dI}{dt}$ Voltage Noise
- Power Supply Rejection Ration (PSRR)
- DC-DC Converter Switching Noise and Stability

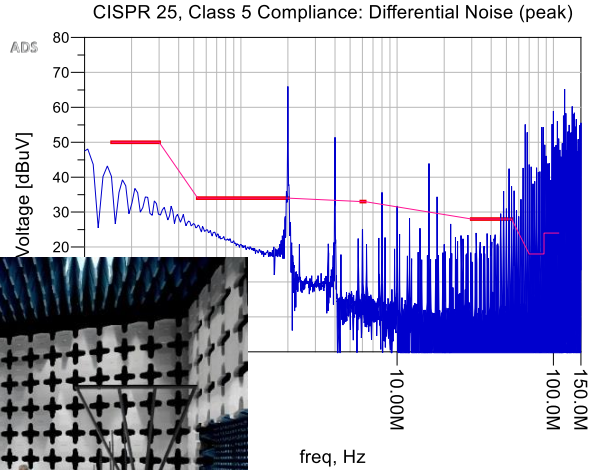
Note: A Point-of-Load (POL) Power Supply is typically a Switched Mode Power Supply (SMPS) with a Buck Regulator DC-DC Converter design that the Microprocessor PCB world often calls as a Voltage Regulator Module (VRM)

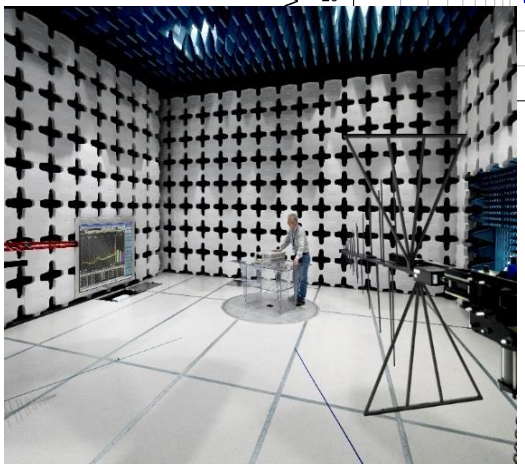
Failing EMI is Expensive

Conducted Emission Testing



CISPR Compliance





Key Take Away:
Late in the design EMI/EMC failures are expensive. Take the time to simulate!

Agenda

- **The 3 Sources of Power – VRM, PDN Capacitors, Package/Die**
- Case Study – Finding Worst Case Noise with Impedance
- How to Build a PI Ecosystem Simulation

Power Delivery for Digital Loads is AC not DC!

$$V = L\frac{dI}{dt}$$

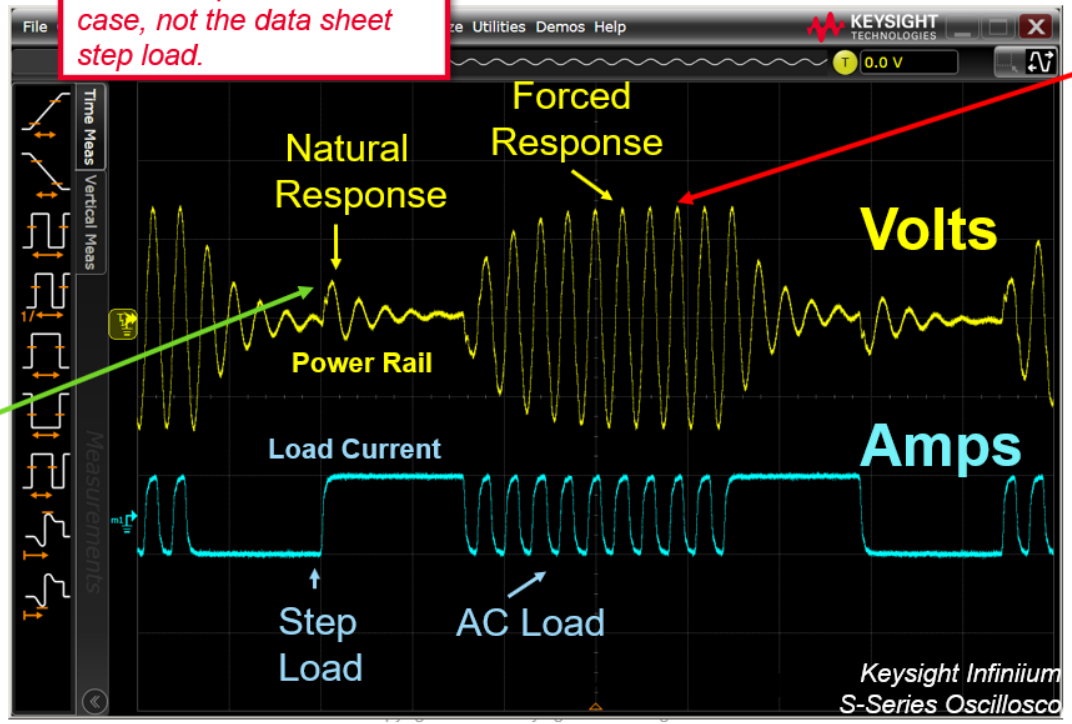
KEY TAKE AWAY
Forced response is worst case, not the data sheet step load.

New Method: Finding the worst case Load

FAIL
Over Voltage
Tx/Rx Bit Error
EMI
Crosstalk

Old Method: Step Load Transient Test (False Positive)

PASS
Datasheet Design



Power Integrity Starts with Target Impedance

Key Take Away:
Impedance is the new way to deliver quiet power to a digital load.

Target Impedance Calculation

$$Z_{\text{Target}} = \frac{\Delta V_{\text{Max Ripple}}}{\Delta I_{\text{Max Transient Load}}}$$

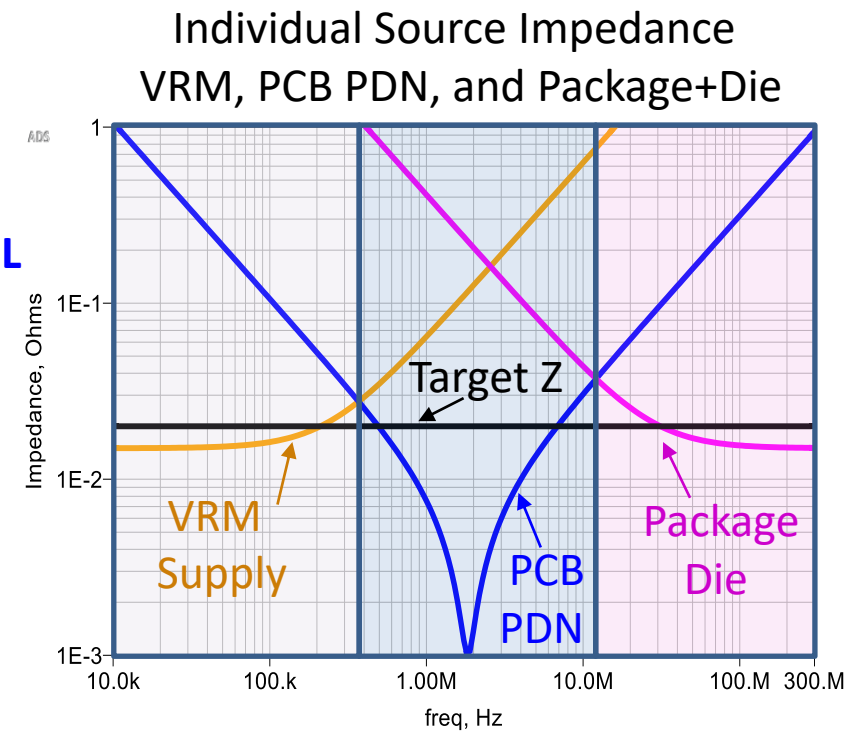
The Source of Power Depends on Frequency!

VRM = Low Pass Series R-L

PDN Capacitors = Band Pass Series C-R-L

Package/Die = High Pass R-C

Key Take Away:
There are 3 bands of power delivery, the VRM, the PCB PDN, and the Package+Die



Where does the ringing come from?

Key Take Away:
Most PDN resonances are from energy flowing between an L and a C

Energy stored in the Magnetic Field

$$V(t) = L\frac{di}{dt}$$

$$Z = j\omega L$$

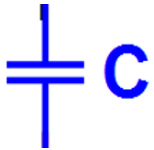
$\vec{B}$ 

Phase V Leads I

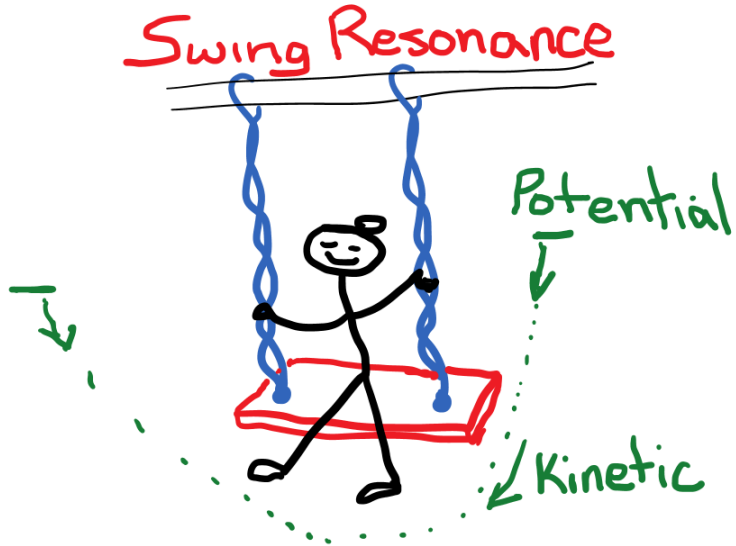
Energy stored in the Electric Field

$$I = \int C\frac{dV}{dt}$$

$$Z = \frac{-1}{j\omega C}$$

$\vec{E}$ 

Phase V Lags I

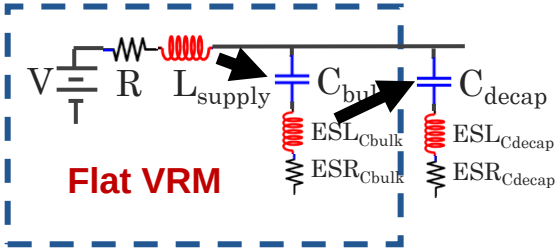


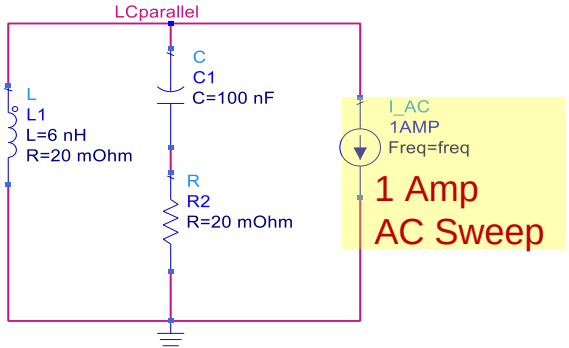
Root Cause of Ringing on the Power Rail

Key Take Away:
A resonant Zpeak is dampened with real resistance.

Parallel inductance can resonate with the decoupling capacitance

Parallel L-C in the PDN





$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

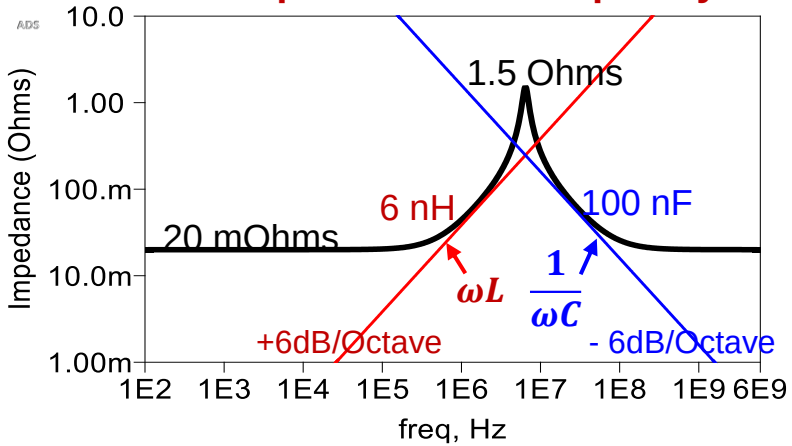
$$\Delta V = \Delta I \cdot Z_{peak}$$

$$\boldsymbol{Z_{peak} = Z_0 \cdot Q}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$

$$Q = \frac{Z_0}{R_{total}}$$

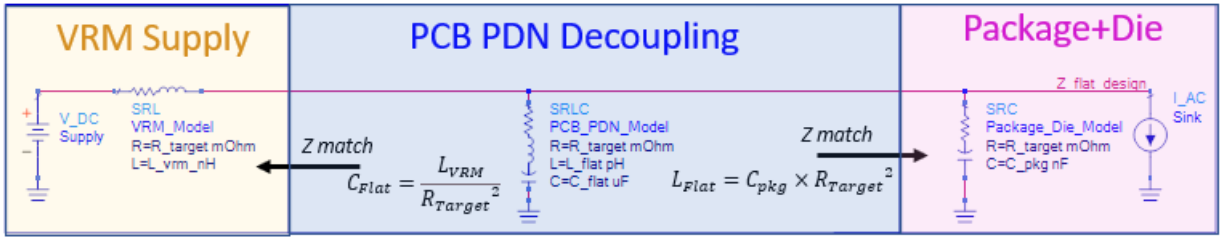
Impedance vs. Frequency



Zpeak=1.5 Ohms

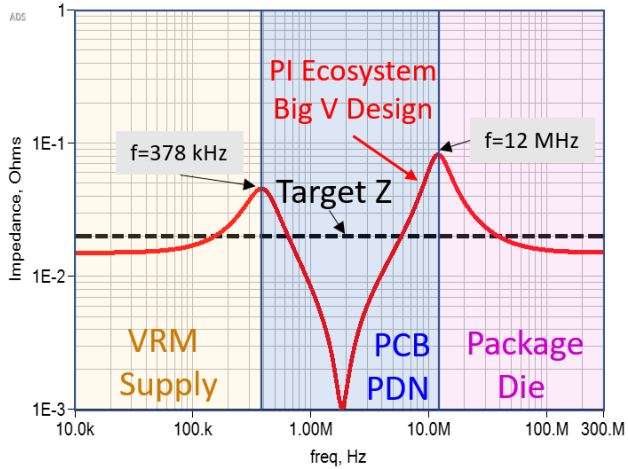
Zo=250 mOhms

PI Ecosystem Simulation: VRM + PCB PDN + Load

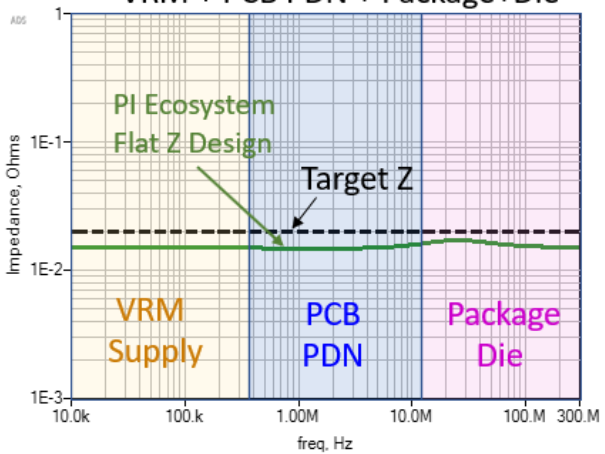


Key Take Away:
Power sources must match impedance to avoid resonances.

PI Ecosystem Impedance
VRM + PCB PDN + Package+Die



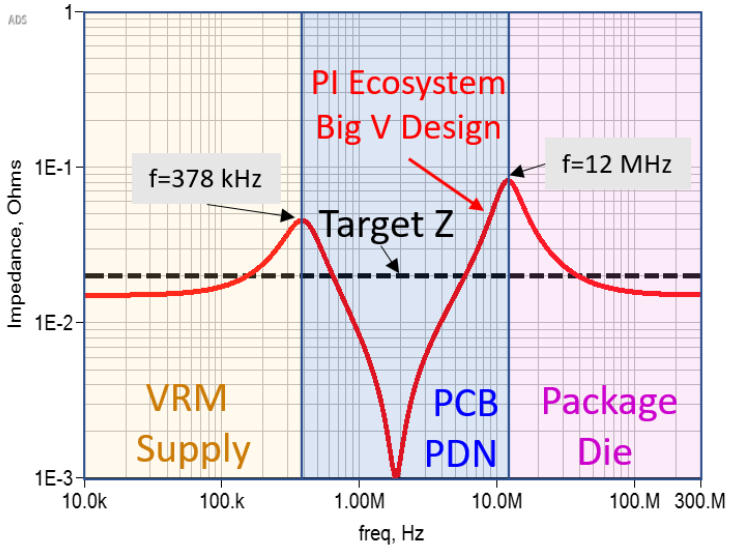
Flat Impedance Design
VRM + PCB PDN + Package+Die



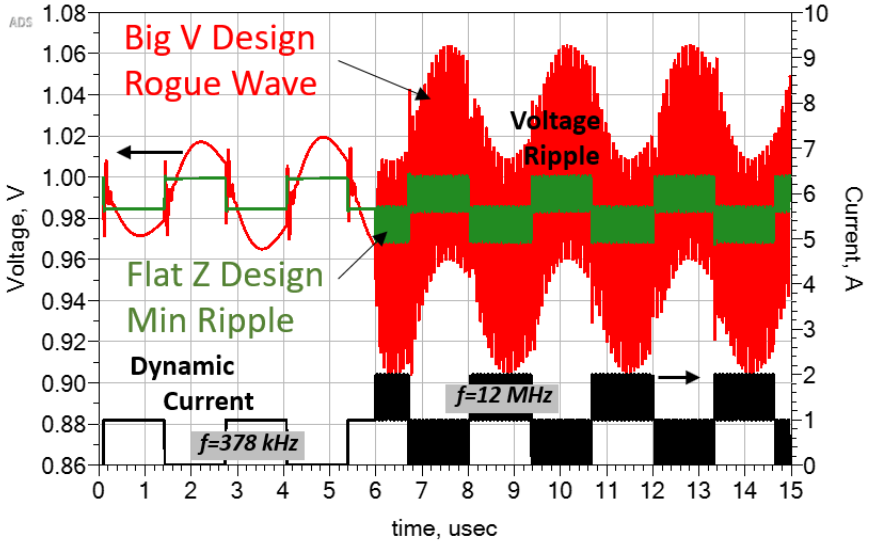
Worst Case Power Rail Noise Ripple

Key Take Away:
Frequency Domain plus Time Domain finds Worst Case Noise Ripple

PI Ecosystem Impedance
VRM + PCB PDN + Package+Die



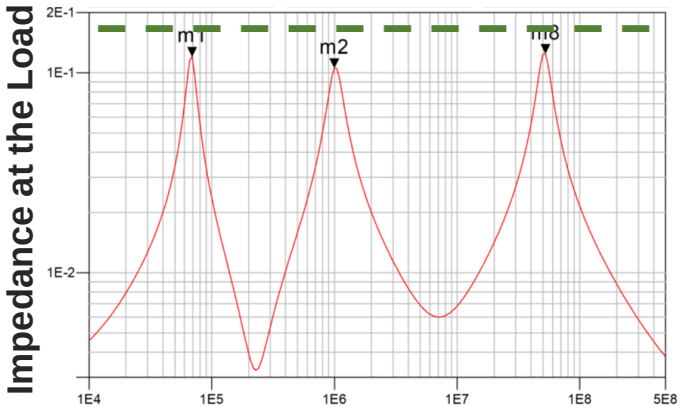
Dynamic Load at 378 kHz and 12 MHz
Big V PDN vs. Flat PDN



Power Rail Impedance is the New Way!

$$Vripple = Itransient * Zpdn$$

Impedance Peaks Help Predict Worst Case Load Transients

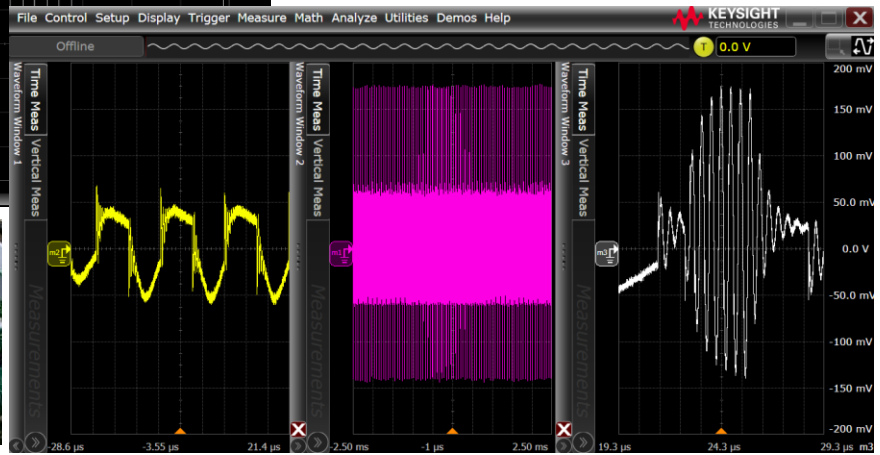


Log Scale 10kHz to 5MHz

Forced Excitation at Peak Z Frequencies

Key Take Away:
Voltage Rogue Waves are Real

Rogue Wave Captured



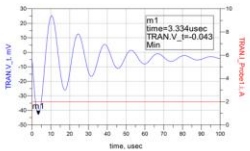
Time Domain – A One to Many Relationship

Target Z = delta V / delta I
What V? What I?

A 2 Amp change yields 3 different responses

Step

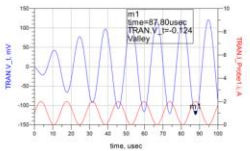
$$\Delta V = \Delta I \cdot \sqrt{\frac{L}{C}} \cdot e^{\frac{-\pi}{4Q}} = 39mVpk$$



$\Delta I = 2Amps$
$\Delta V = 43mVpk$

Sine forced

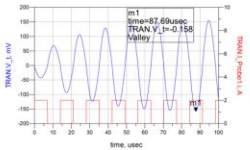
$$\Delta V = \Delta I \cdot \sqrt{\frac{L}{C}} \cdot \frac{Q}{2} = 123mVpk$$



$\Delta I = 2Amps$
$\Delta V = 123mVpk$

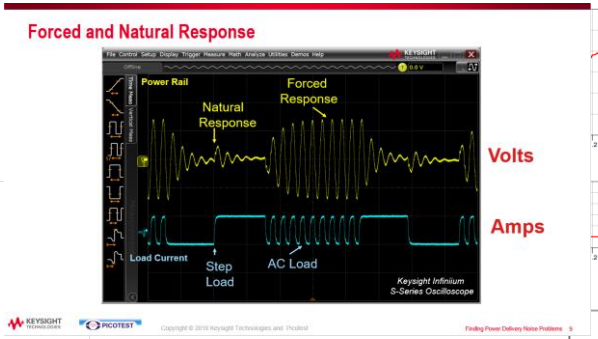
Square forced

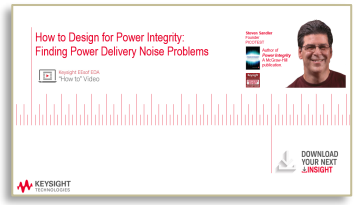
$$\Delta V = \Delta I \cdot \sqrt{\frac{L}{C}} \cdot \frac{2Q}{\pi} = 157mVpk$$

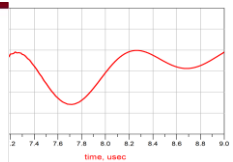


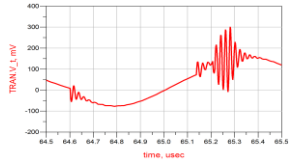
$\Delta I = 2Amps$
$\Delta V = 157mVpk$

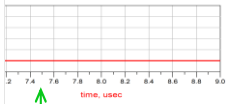
Clearly $\Delta V \neq \Delta I \cdot Z_{Target}$

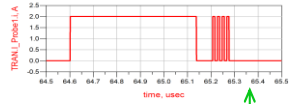


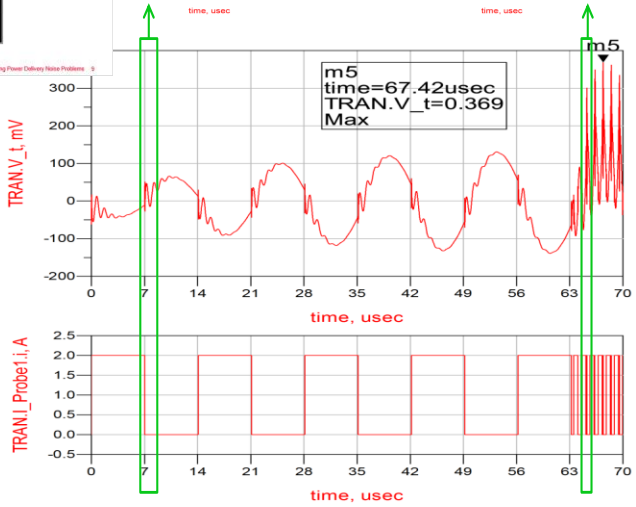




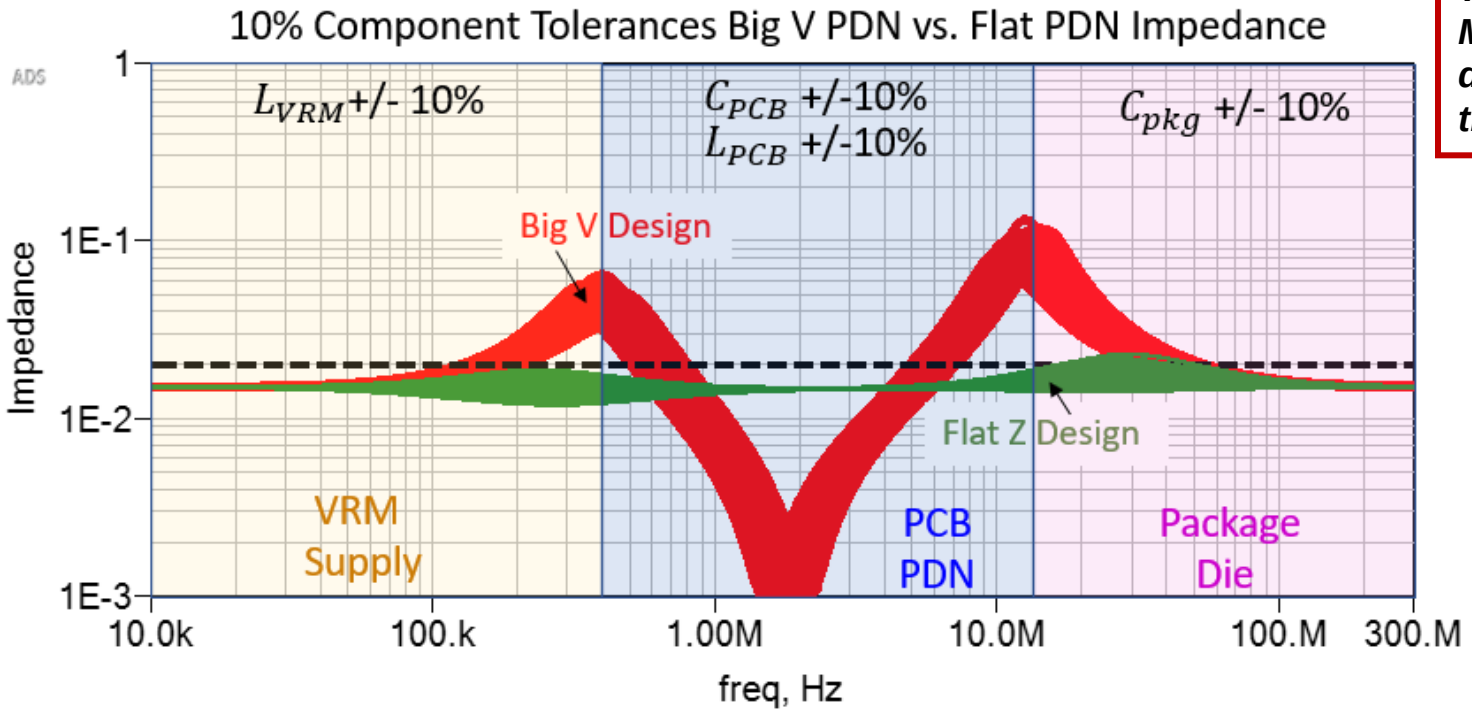








Flat Impedance Design Provides Bigger Margins

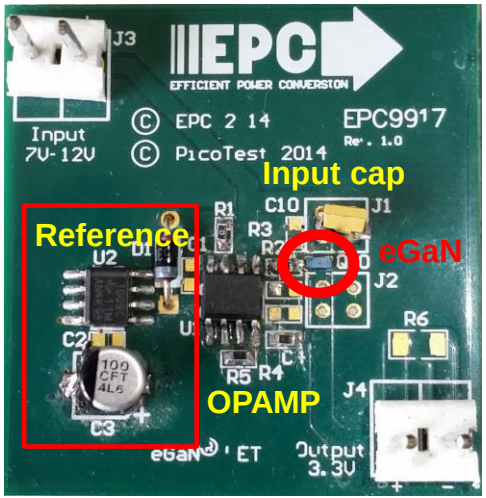


Key Take Away:
Tolerances matter! Make sure your design is not on the edge of a cliff.

Why Wide Bandgap is So Exciting for Power Delivery

….not just the size

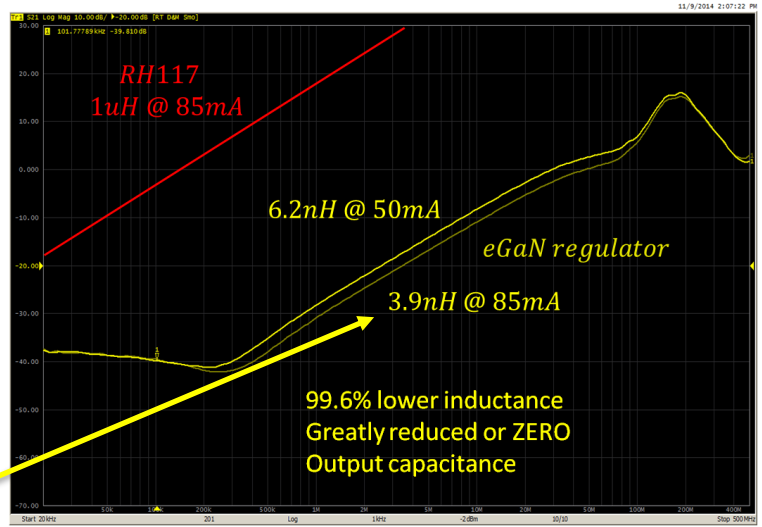
GaN



$$C_{Flat} = \frac{L_{VRM}}{Z_{Target}^{\ 2}}$$

Key Take Away:
The lower output inductance of Wide Bandgap reduces the total C required. Saves $$ and space.

Maintaining a 0.1Ω maximum PDN impedance up to 2MHz requires 80uF for a RH117 and NO output cap for the eGaN regulator.

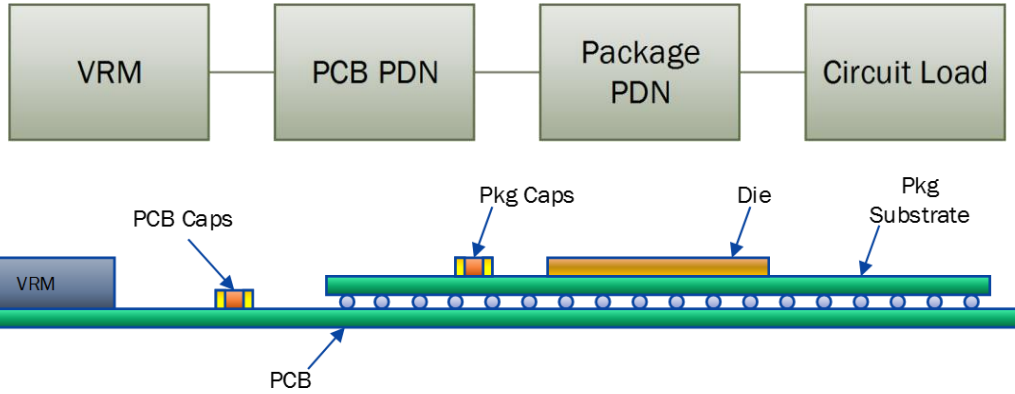


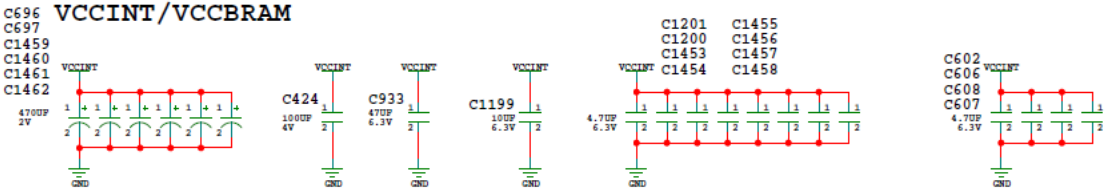
3.9nH is nearly equivalent to the ESL of a tantalum capacitor

Agenda

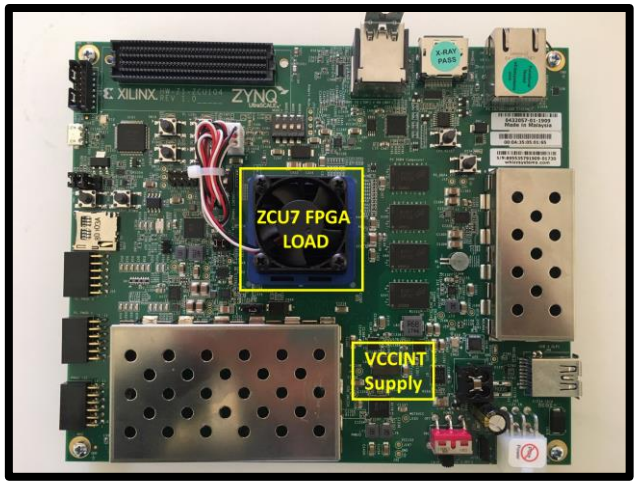
- The 3 Sources of Power – VRM, PDN Capacitors, Package/Die
- **Case Study – Finding Worst Case Noise with Impedance**
- How to Build a PI Ecosystem Simulation

Why Lowest ESR is Not Good, It Must be Matched



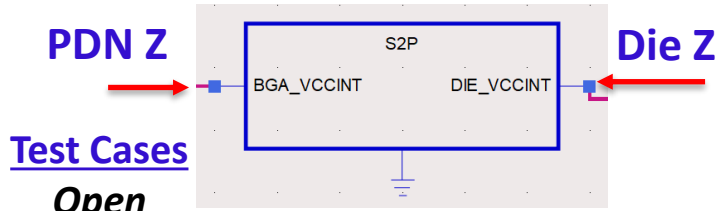


AMD* Zynq UltraScale+
XCZU7EV-2FFVC1156 MPSoC



* Formerly Xilinx

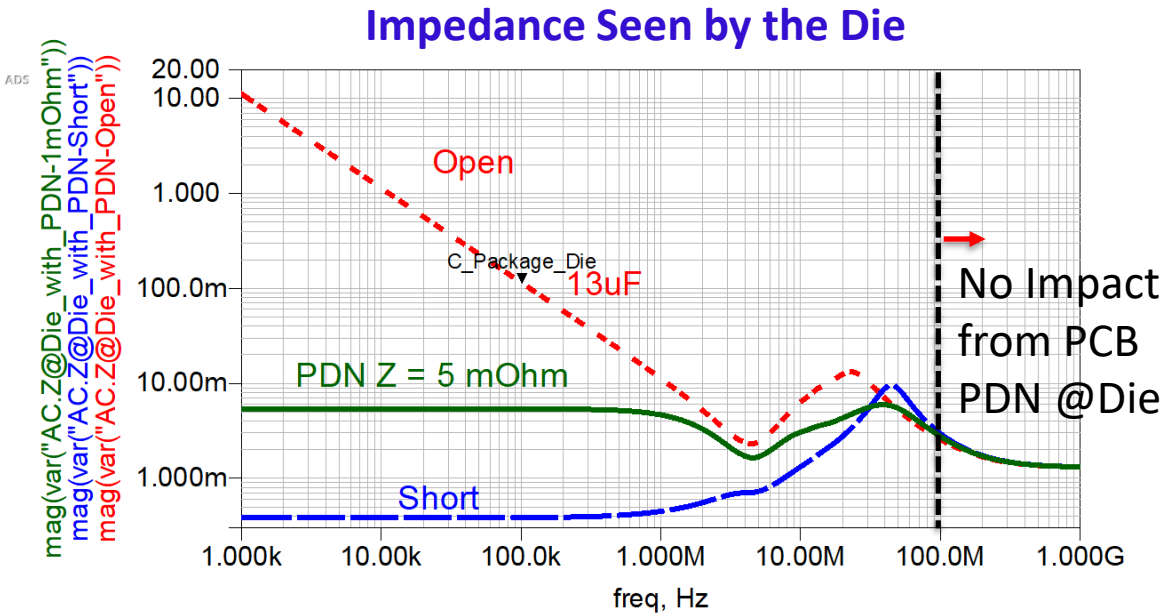
FPGA Package/Die Model Connected to the PCB PDN



Test Cases

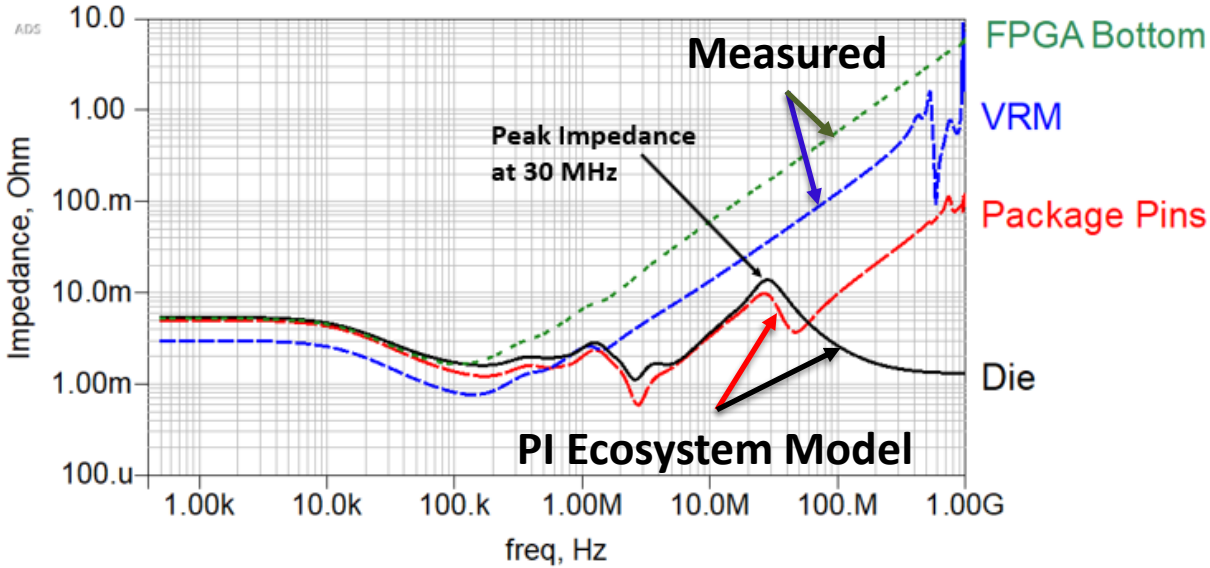
Open
5 milliohm
Short

Key Take Away:
Matched Z avoids high Q resonances.



FPGA Package/Die, PCB PDN EM, and Capacitor Models are Critical

Impedance measurements did not see the resonance at 30 MHz!

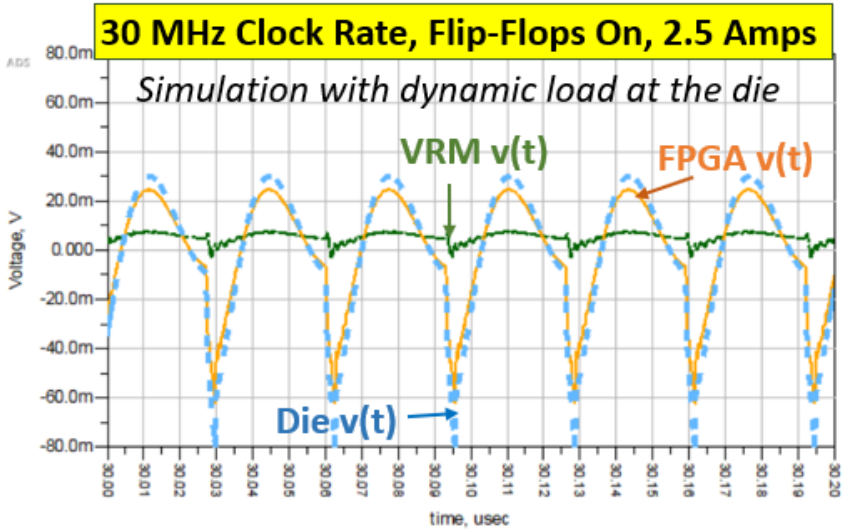


Key Take Away:
Simulation with accurate models show what is missed in measurement.

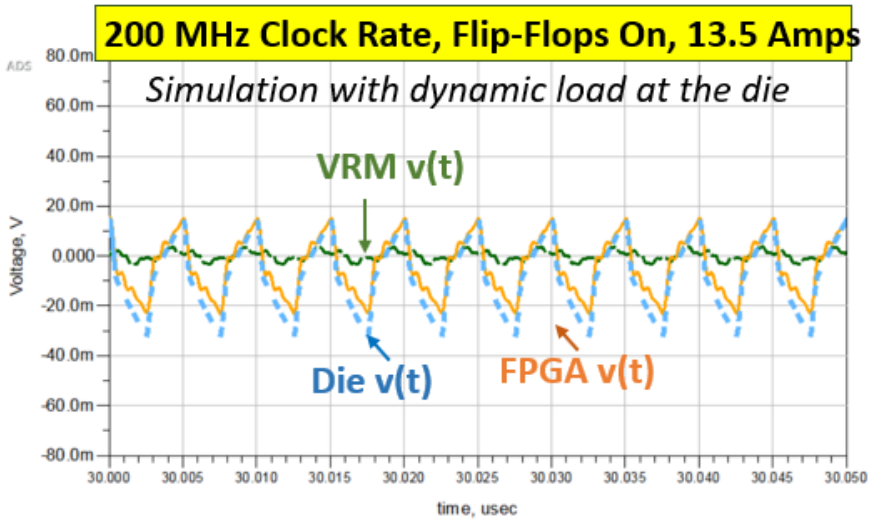
- *Measurements with VCCINT are only accessible on the bottom side of the FPGA and include the via inductance.*
- *PIPro PDN EM model with package/die (CPM) in ADS schematic accurately predicts impedance peak that measurement could not see.*

Simulation Shows 30 MHz Toggling has More Noise

Lower frequency and lower current has higher noise



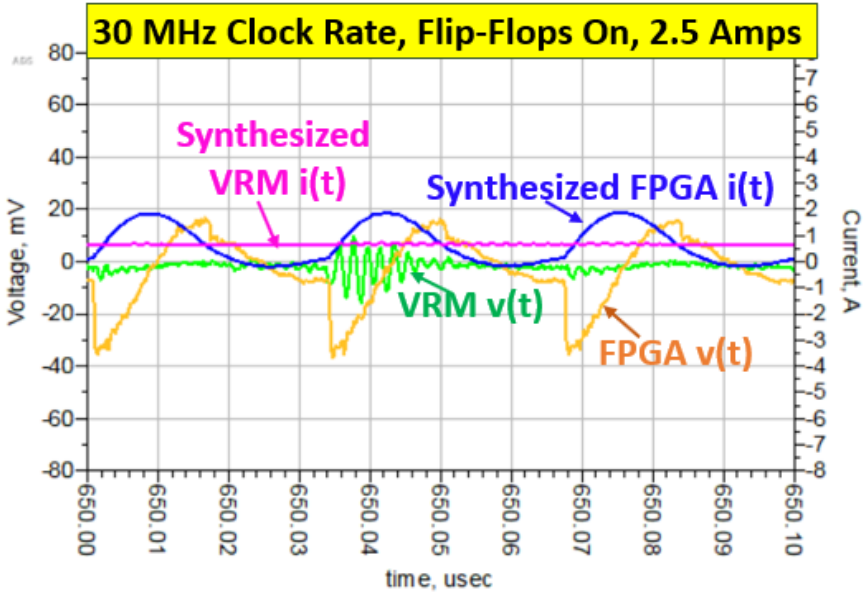
Higher frequency and higher current has less noise

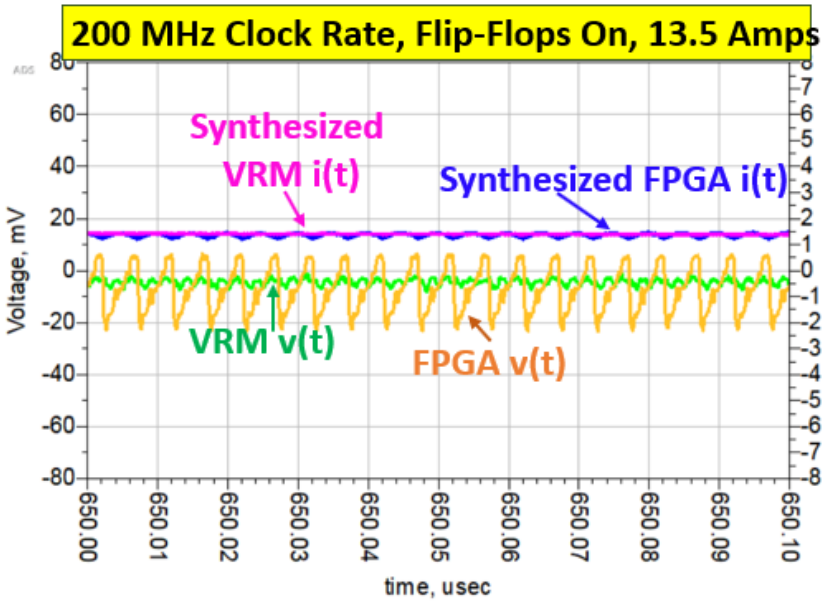


Key Take Away:
Power delivery is not intuitive!

Synthesized Currents from Measured Voltages

The Ultimate Digital Twin: Measurement Enabled Simulations



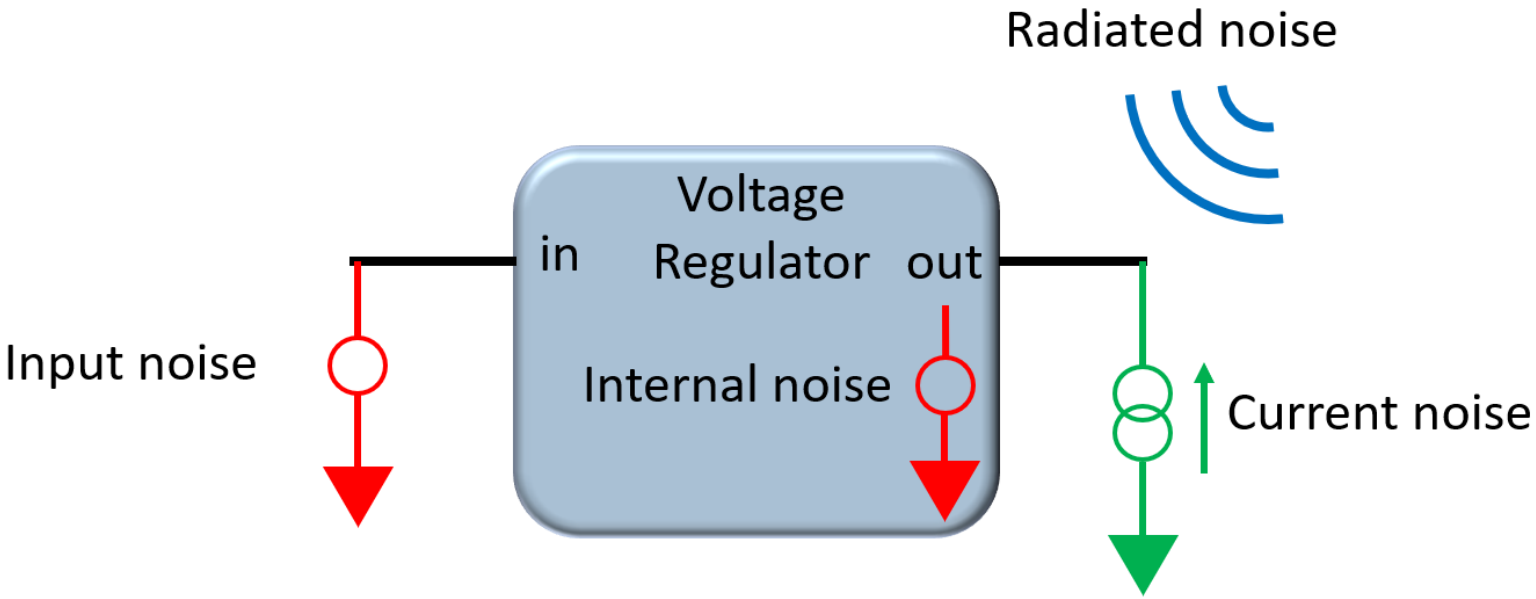


H. Barnes, S. Sandler, and J. Carrel, "A Method for Dynamic Load Current Testing with a Benchtop Power Supply" DesignCon 2020.

Agenda

- The 3 Sources of Power – VRM, PDN Capacitors, Package/Die
- Case Study – Finding Worst Case Noise with Impedance
- **How to Build a PI Ecosystem Simulation**

The VRM is a Noise Source AND a Noise Hub

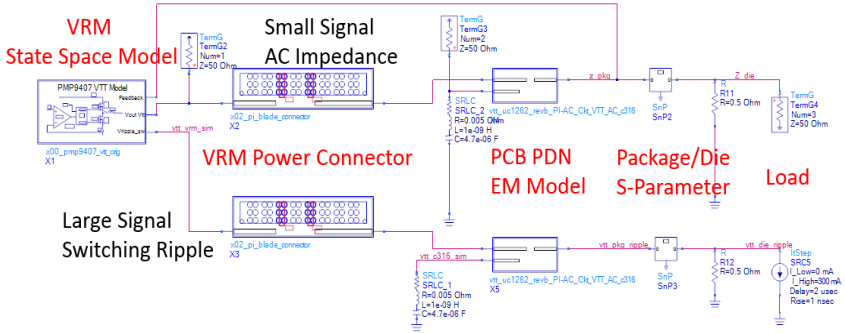


State Space VRM Models Enable PI Ecosystem Simulations

Three Separate Simulations in one Schematic

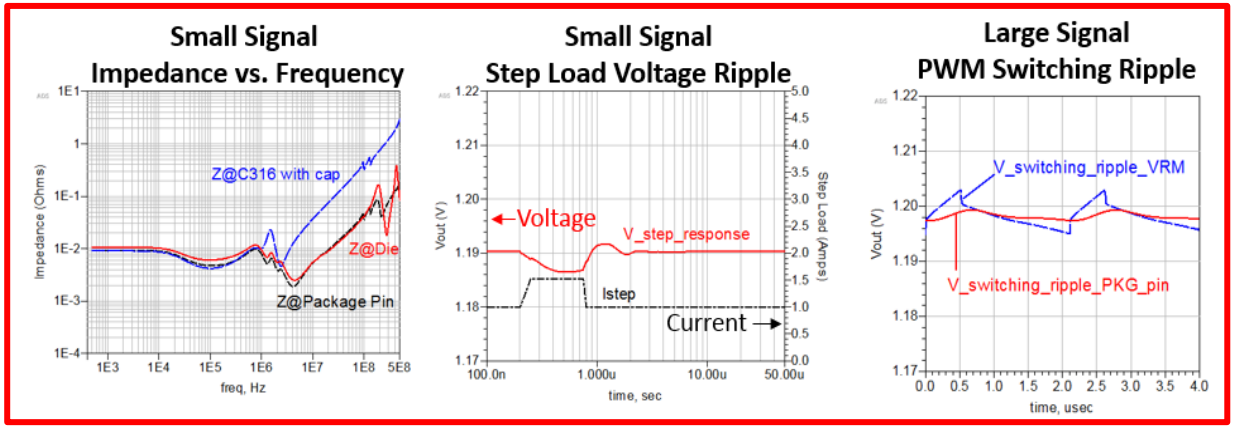
Simulation Controllers

AC	S-PARAMETERS	HARMONIC BALANCE
AC AC1 Start=100 Hz Stop=40 MHz Step=	S_Param SP1 Start=100 Hz Stop=40 MHz Step=	HarmonicBalance HB1 Freq[1]=Fs Order[1]=256



Key Take Away:

VRM models provide small signal load ripple and large signal VRM switching ripple



How Good is Your Capacitor Model?

3 Different 0805 1uF/25V capacitors

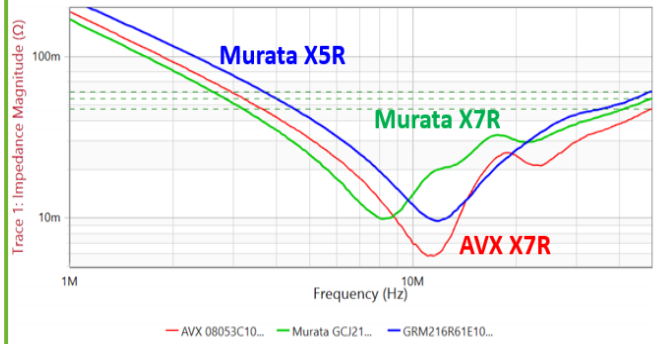
Vendor Data for Inductance:

- 709 pH **08053C105JAT2A**
- 400 pH for the **GCJ21BR71W105KA12L**
- 340 pH for the **GRM216R61E105KA12D**

Vendor data has wildly different inductance values, while the measured data shows that the 0805 package is consistent with ~155 pH.

Measured Data with Mounting Inductance Removed:

AVX 08053C10...	Murata GCJ21...	GRM216R61E10...
140.119 pH	148.087 pH	174.123 pH

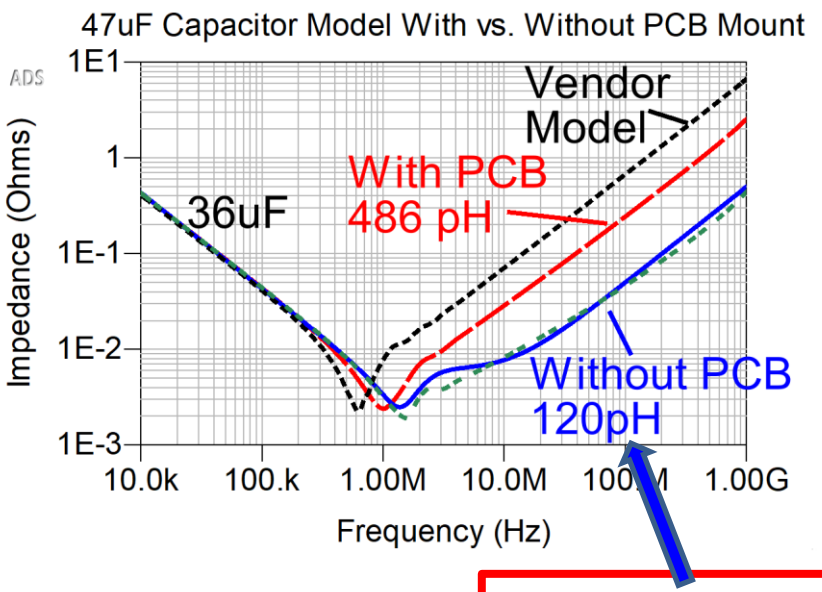


EDICON 2021

Key Take Away:
Capacitor placement optimization with incorrect models can lead to wasted engineering efforts.

Measuring Capacitors and Mounting Parasitics

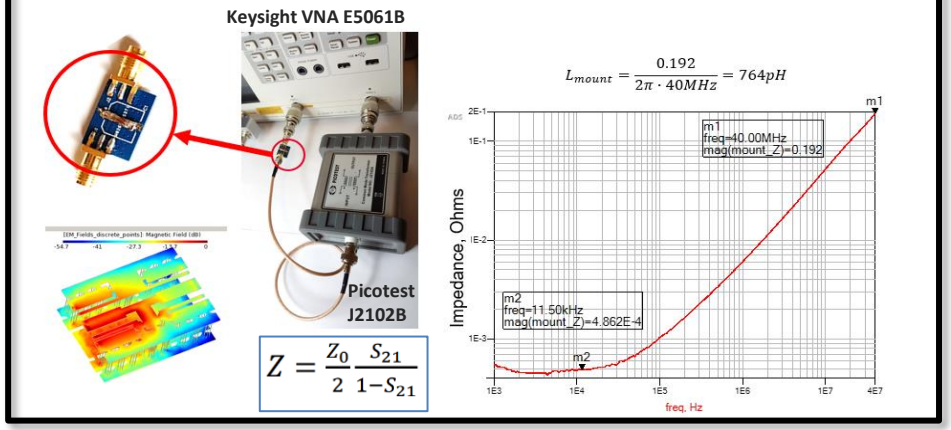
VNA 2-Port Shunt Measurement Method



Use this one with the PCB EM Model. Mounting Inductance is De-Embedded

Measuring Micro-Ohm Mounting Impedance

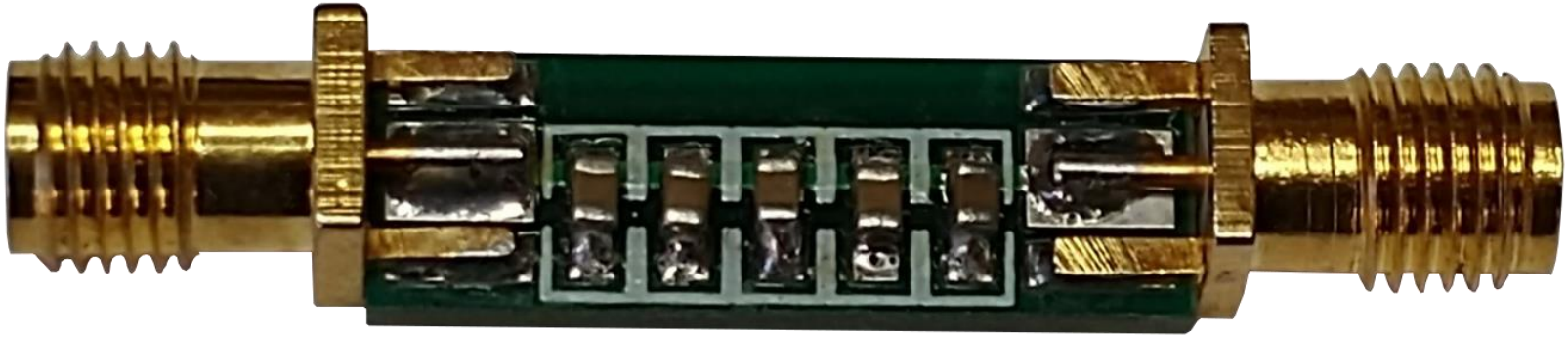
Determining the fixture and mounting parasitics with a short across the capacitor pads.



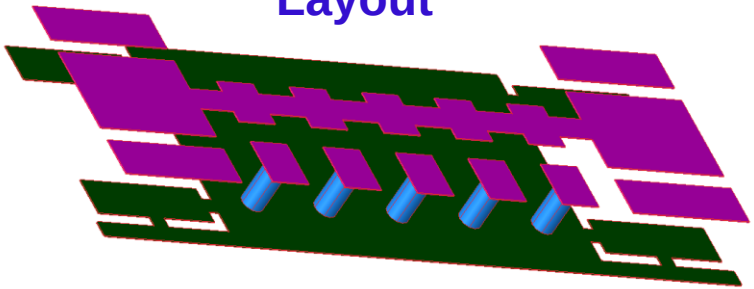
Key Take Away:

The PCB EM model already includes the mounting inductance. So, make sure to use a Capacitor model with all the mounting inductance removed or it will be counted twice!

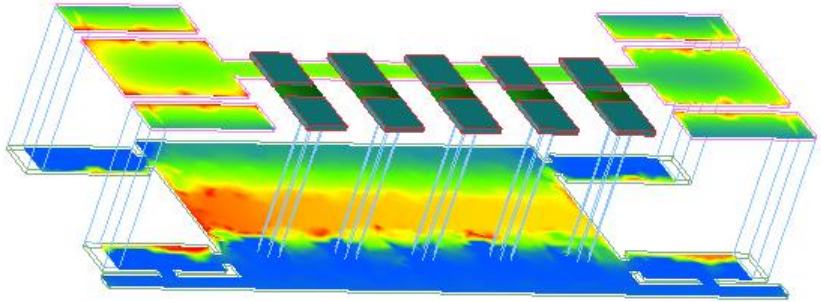
Why the PI Workflow Needs EM Modeling



Layout



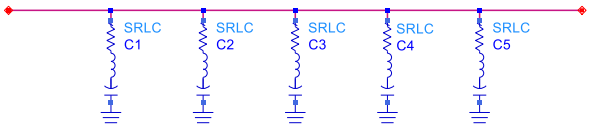
EM Simulation with PIPro



Lumped SPICE Gets It Wrong, EM Includes PCB Parasitics

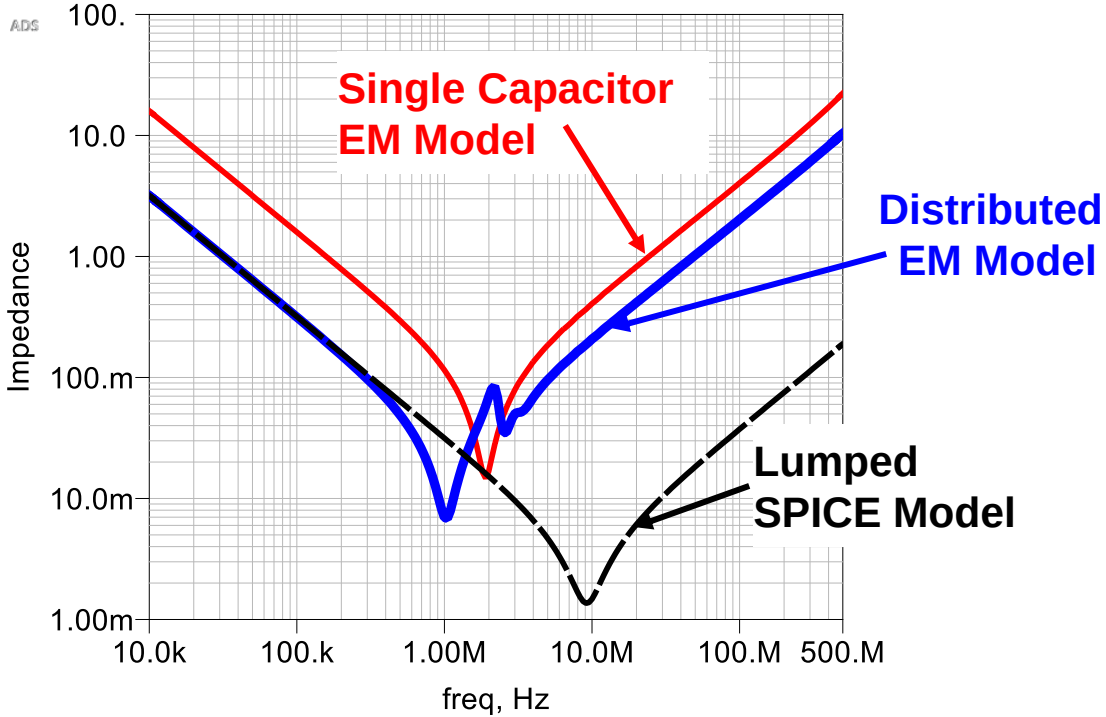
Paralleling same value caps

	C	ESR	ESL
C1	1 uF	7 mΩ	300 pH

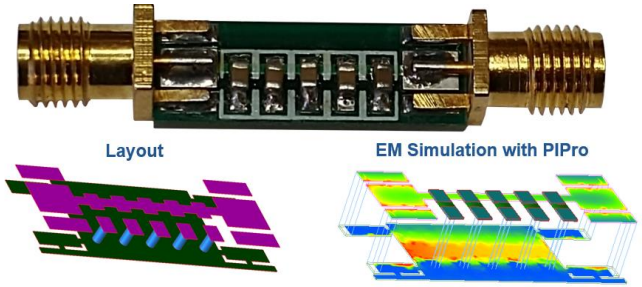


Key Take Away:
Paralleling N of the same capacitor values does not result in the ideal SPICE result when PCB parasitics are included.

Parallel Capacitors SPICE vs PCB EM Model

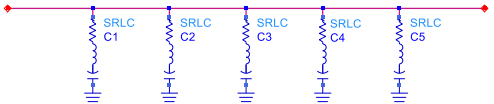


PDN Noise Depends on Measurement Location

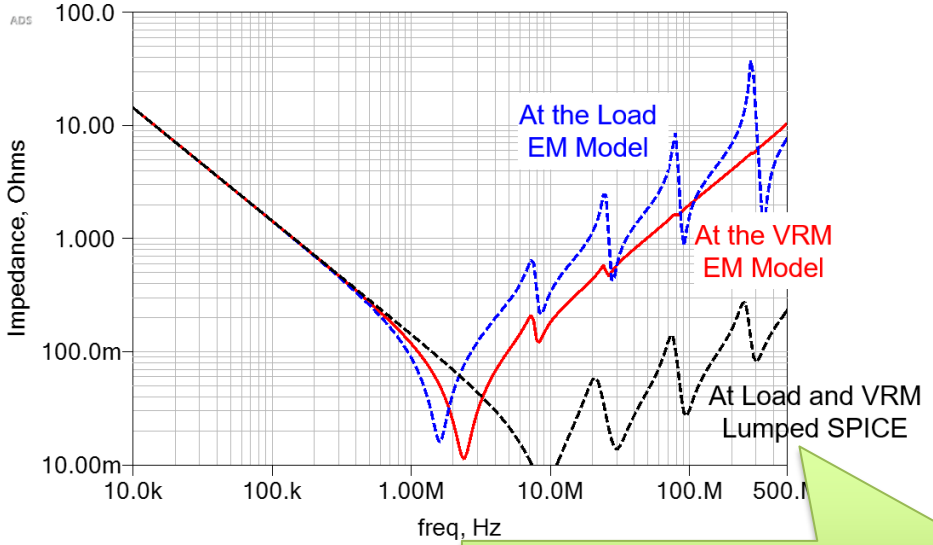


Capacitor Loading by the Decade

	C	ESR	ESL
C1	1 uF	7 mΩ	300 pH
C2	0.10uF	15 mΩ	300 pH
C3	0.01uF	30 mΩ	300 pH
C4	0.001uF	100 mΩ	300 pH
C5	100pF	200 mΩ	300 pH

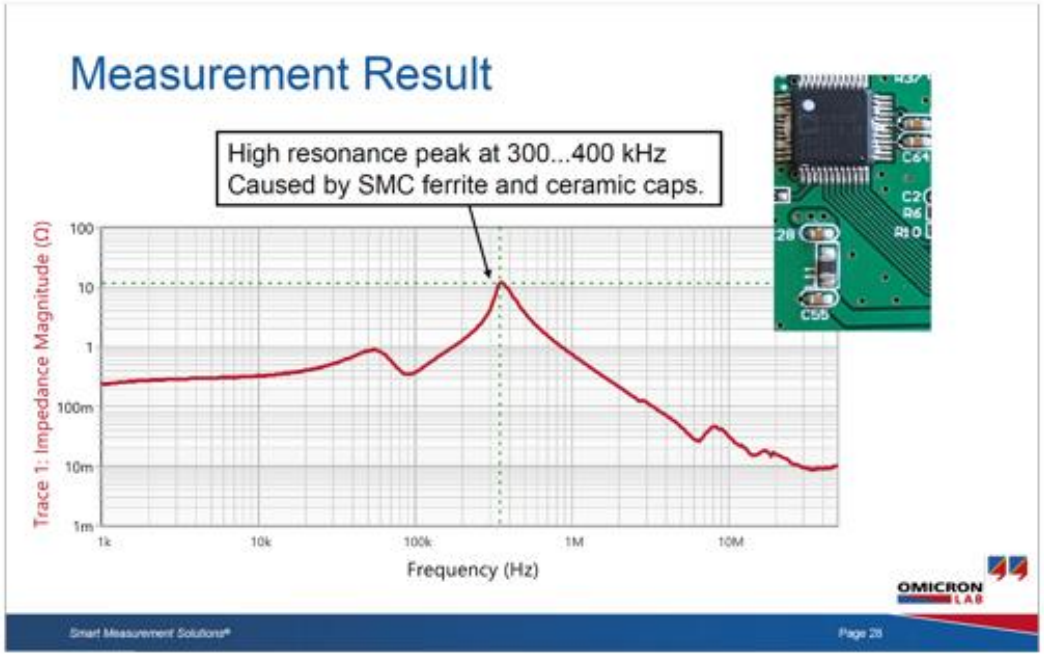


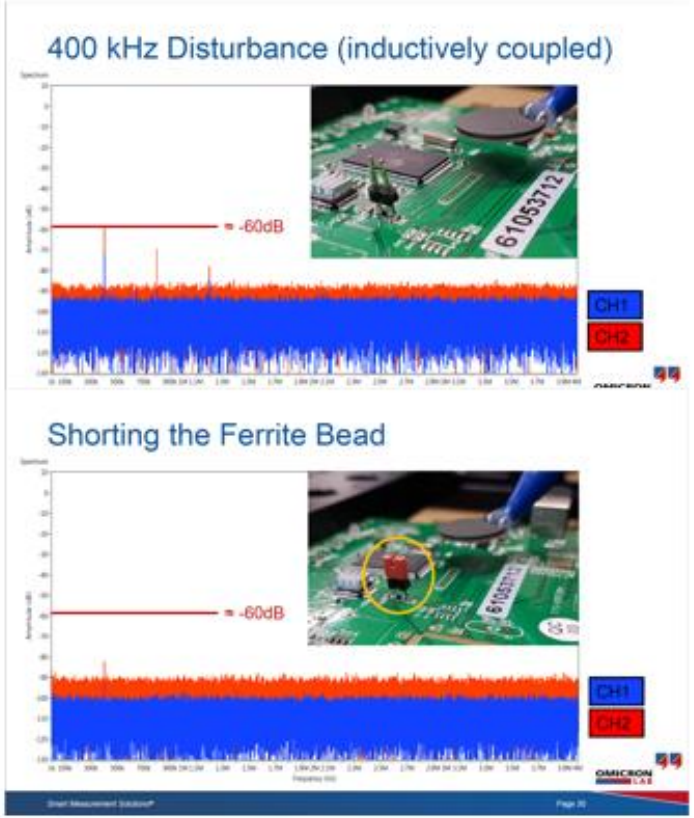
Z at Load vs. Z at VRM



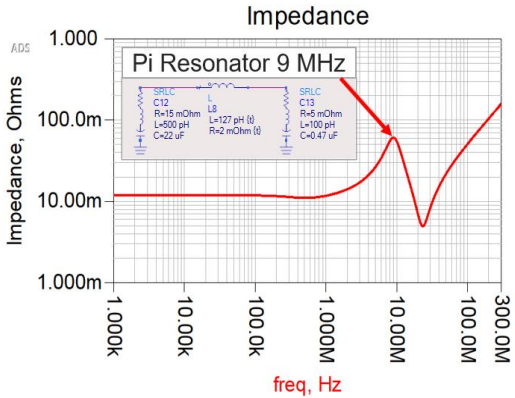
SPICE fails to predict the difference in power rail noise at the VRM vs. the Load.

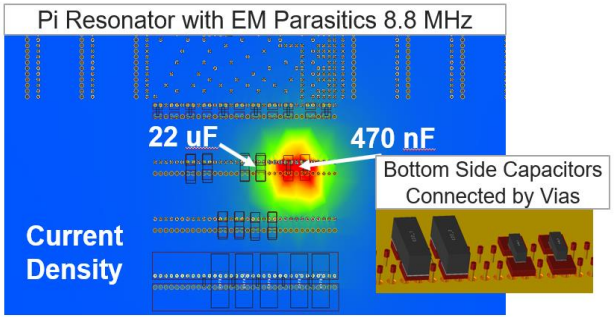
Pesky Ferrite Beads (and LARGE Signal)



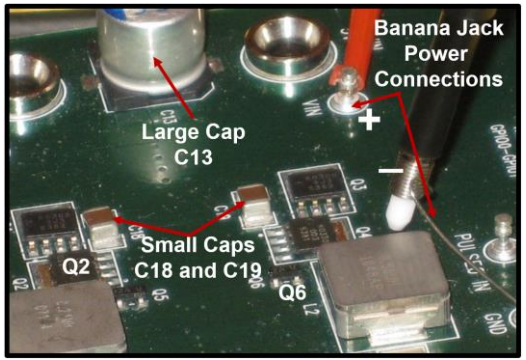


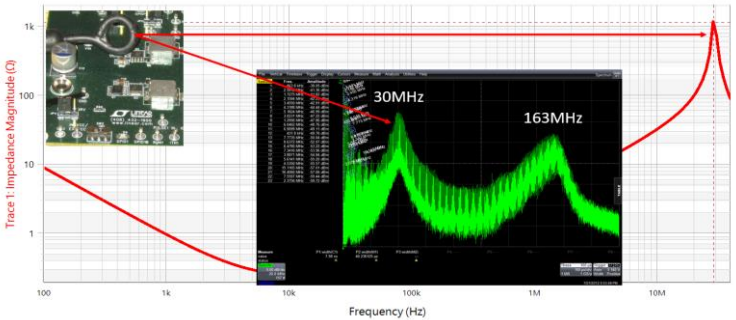
Noise From Capacitor Resonances

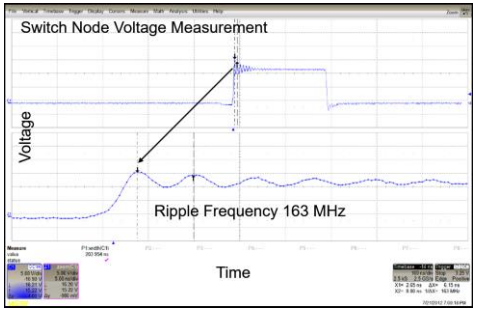




Key Take Away:
Capacitors resonating with other capacitors can cause excessive noise ripple and be a source of EMI

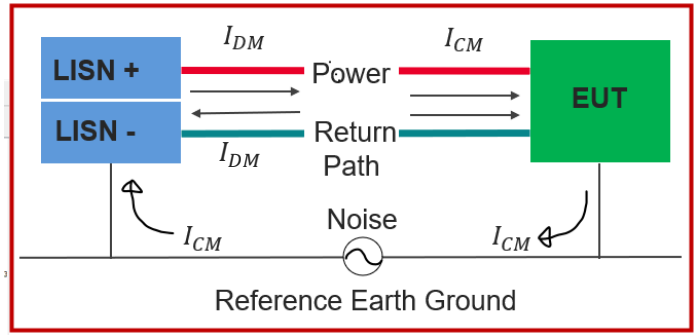




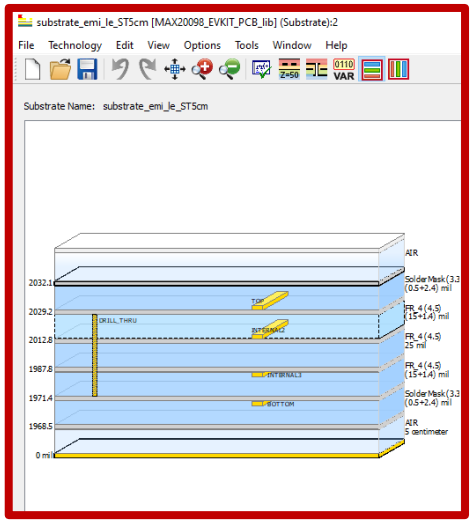


EMI Simulations Need EM Models

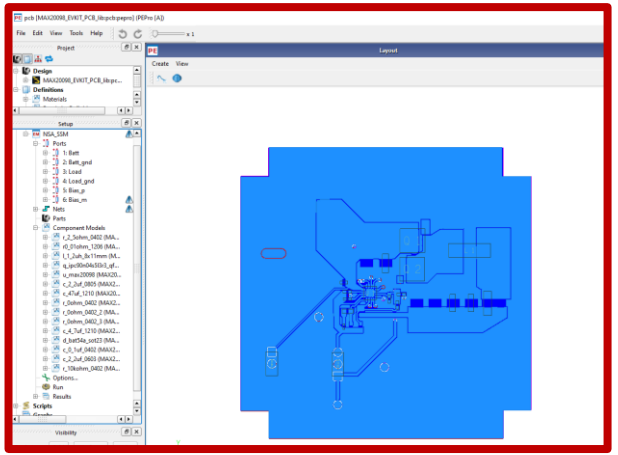
Differential and Common Excitation Requires a Reference Earth Ground



Reference Earth Ground Setup Requires Stack-up Modification



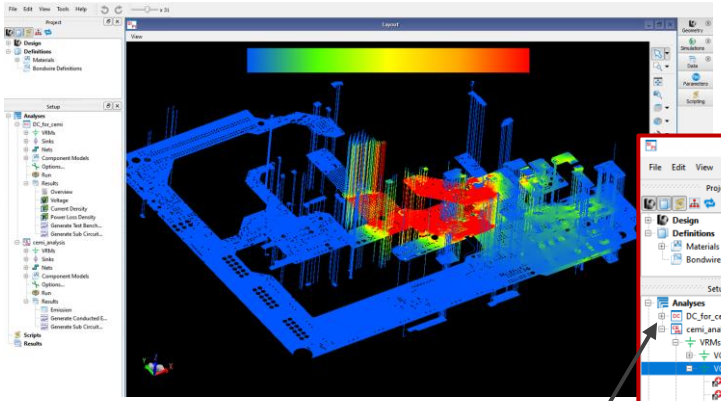
Referencing ports to Earth Ground doubles the number of EM ports to keep track of ☹



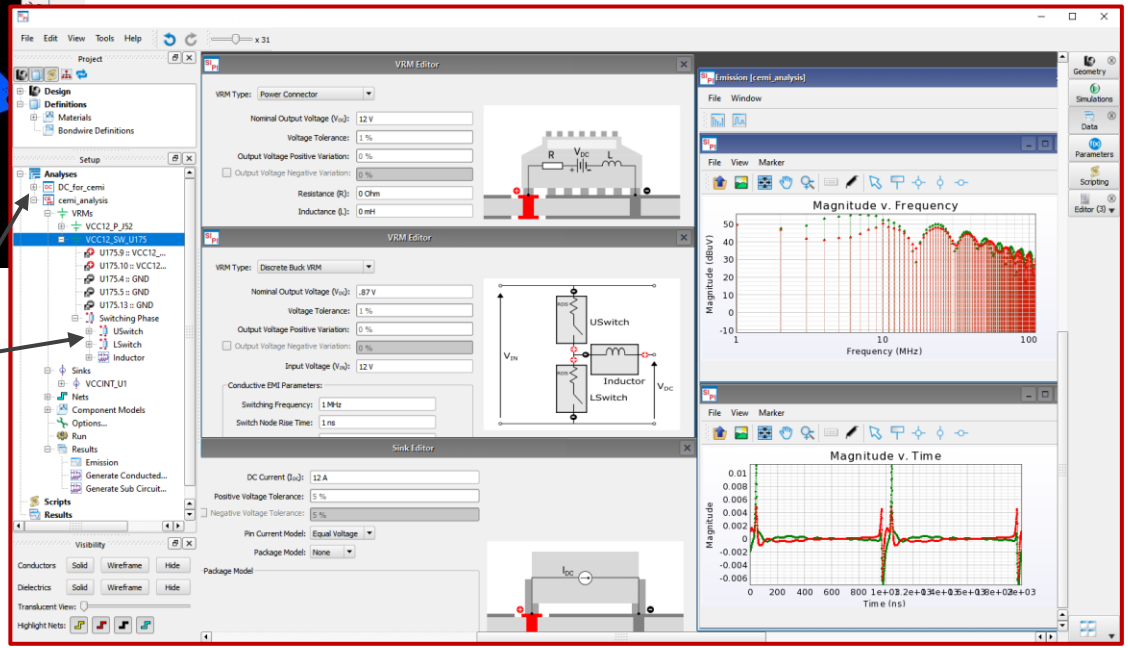
Key Take Away:
Traditional EM simulators require a modified stack-up and complex port setup for conducted EMI.

PI EMI Simulations Need a Switch Model

PIPro DC IR Drop Current Density



***PIPro CEMI** EM Analysis automates ground plate reference ports and populates a generic switching model that runs with **Harmonic Balance for fast** steady state results.*

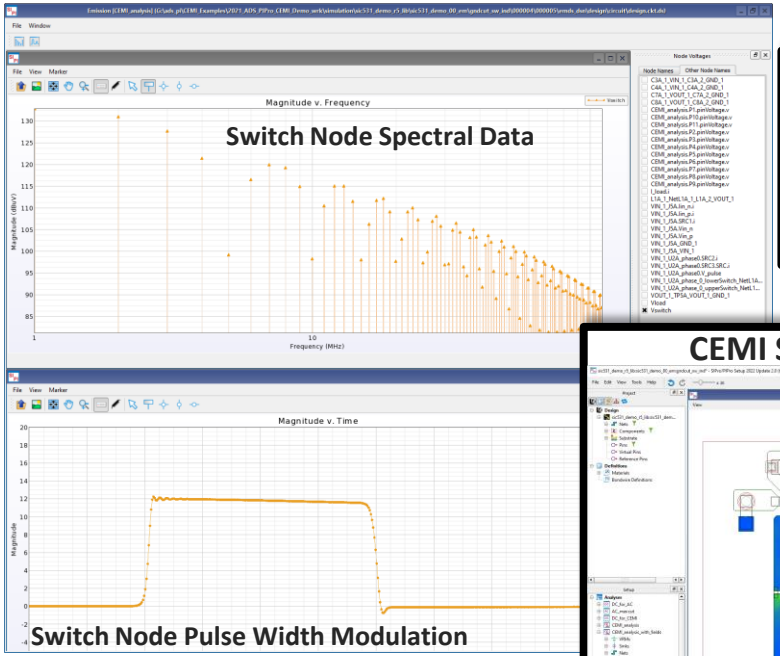


Switching Regulator DC setup for Buck, Boost, and Inverting, and multi-phase can be copied to CEMI setup.

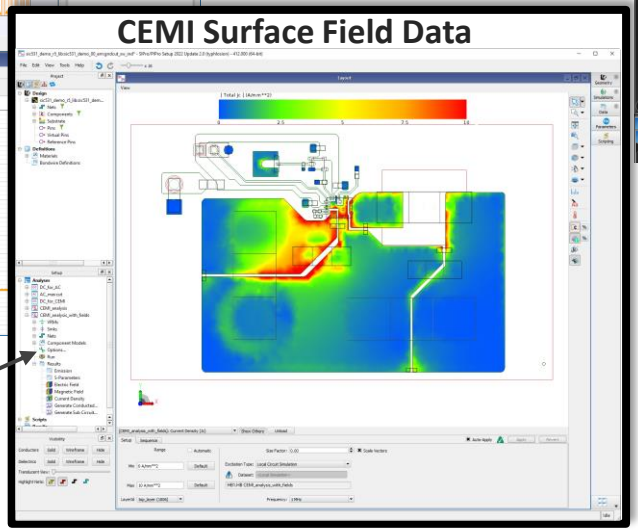
Key Take Away:
PIPro CEMI Analysis automates the differential setup and generic large signal switching model.

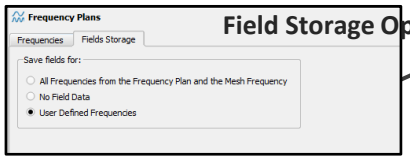
Measurement Tricks for Switching Models

PIPro CEMI EM with Harmonic Balance Excitation



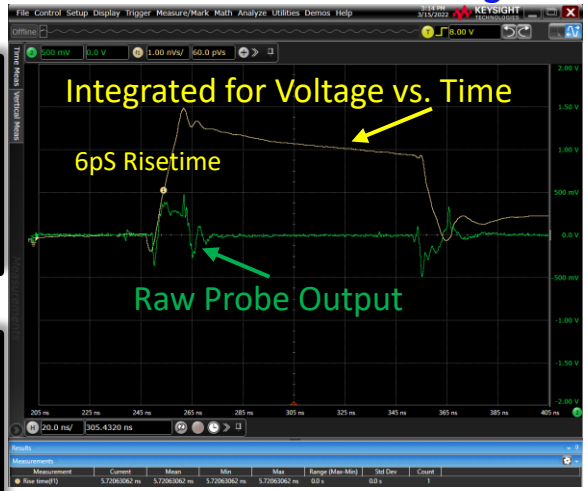
Field Excitation from CEMI Test Bench Harmonic Balance Emission Results to determine phase and magnitude at each frequency. Phase animation available at discrete frequencies.





Field Storage Option

H-Field Probe Raw Data vs. Integrated

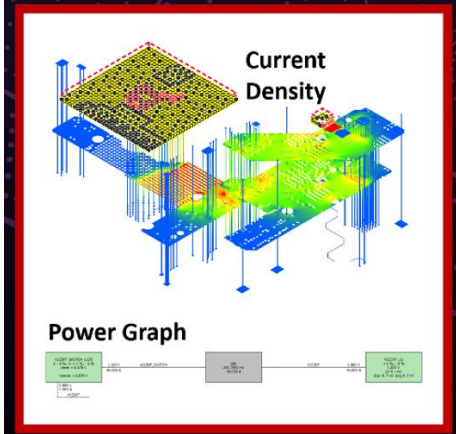


H-Field Probe Beehive H100A

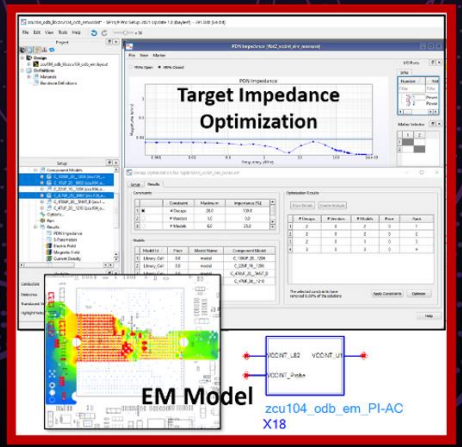
Picotest SIC351 PCB

Power Integrity Needs a Simulation Workflow

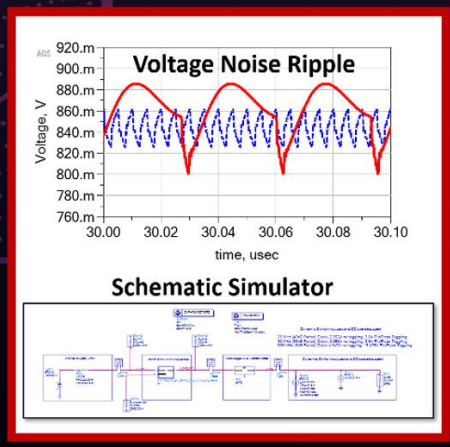
1 PIPro DC IR Drop



2 PIPro AC Impedance



3 PI Ecosystem Transient

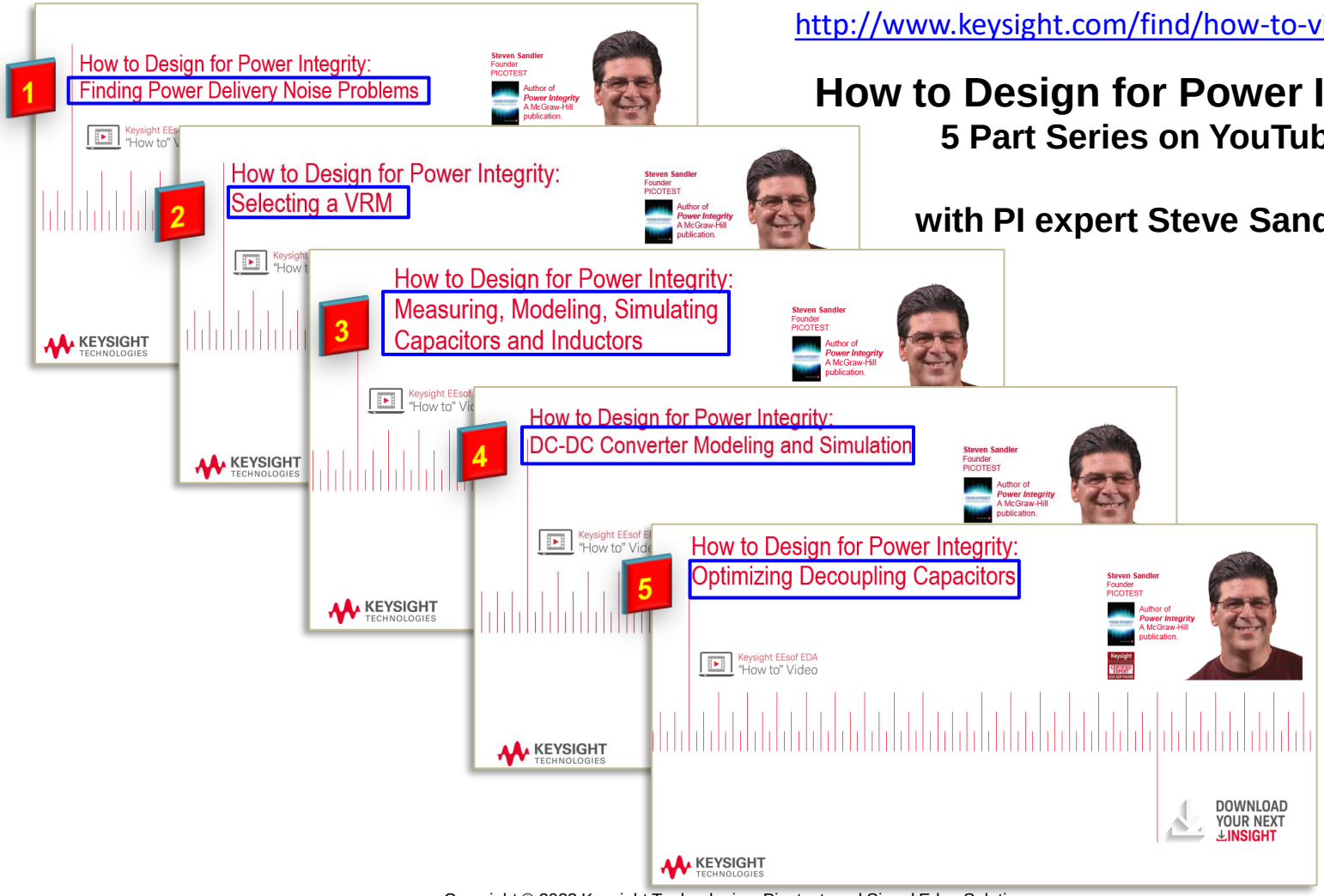


http://www.keysight.com/find/how-to-videos-for-pi

How to Design for Power Integrity

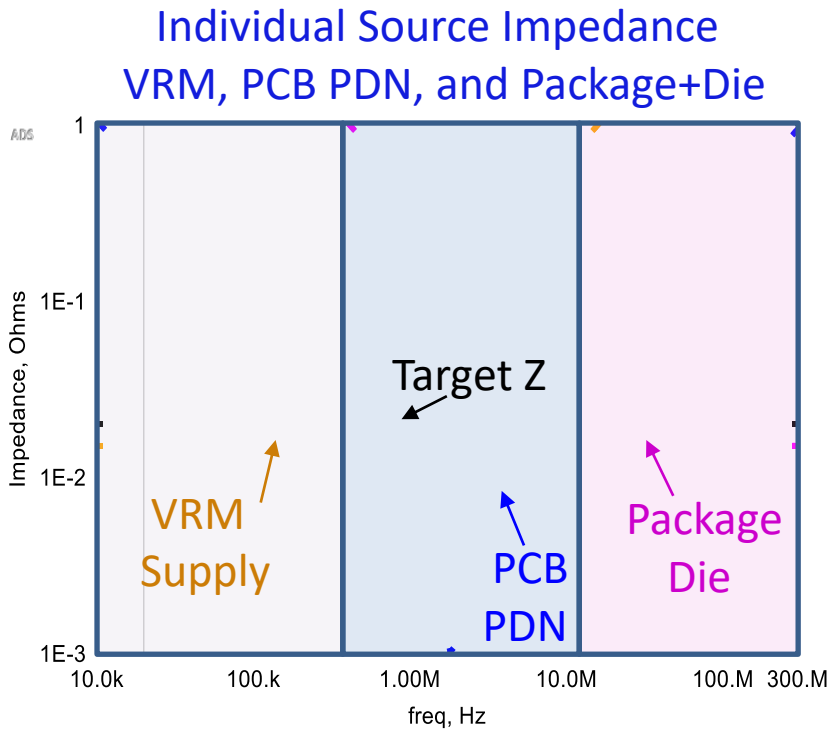
5 Part Series on YouTube

with PI expert Steve Sandler



Remember

- Parallel L and C resonate in the time domain but are easier to find as impedance peaks in the frequency domain.
- Flat impedance minimizes the noise ripple by reducing the dynamic currents.
- Flat impedance is matched impedance with the simple rules of thumb based on $Z_0 = \sqrt{\frac{L}{C}}$



$$C_{Flat} = \frac{L_{VRM}}{R_{Target}{}^2} \qquad L_{PCB} = C_{Pkg} * R_{Target}{}^2$$

Thank you!

—

QUESTIONS?

AGENDA

Power Integrity Basics – VRM + PDN + Digital Load
presented by Heidi Barnes

Measurement Based VRM Modeling
presented by Steve Sandler

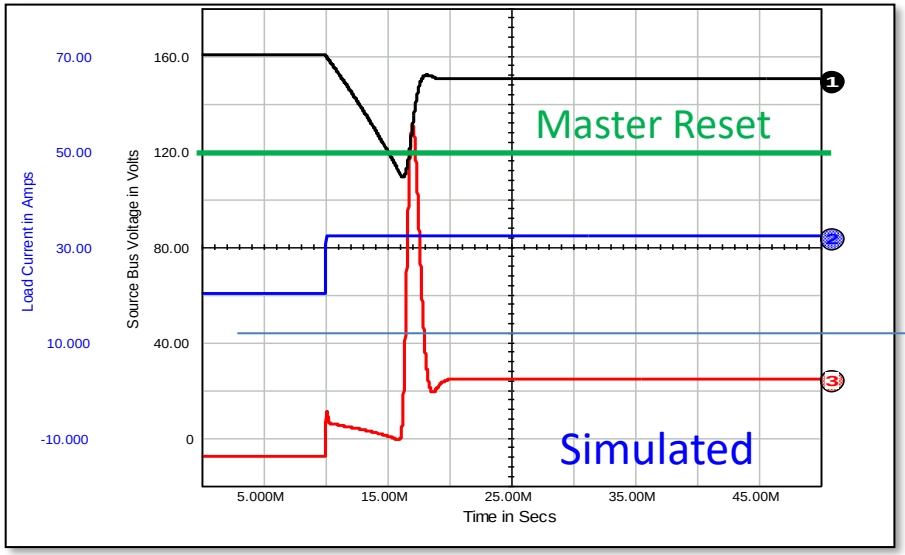
Building a Power Delivery Digital Twin - TI TPS7H4003 SSAM Case Study
presented by Benjamin Dannan

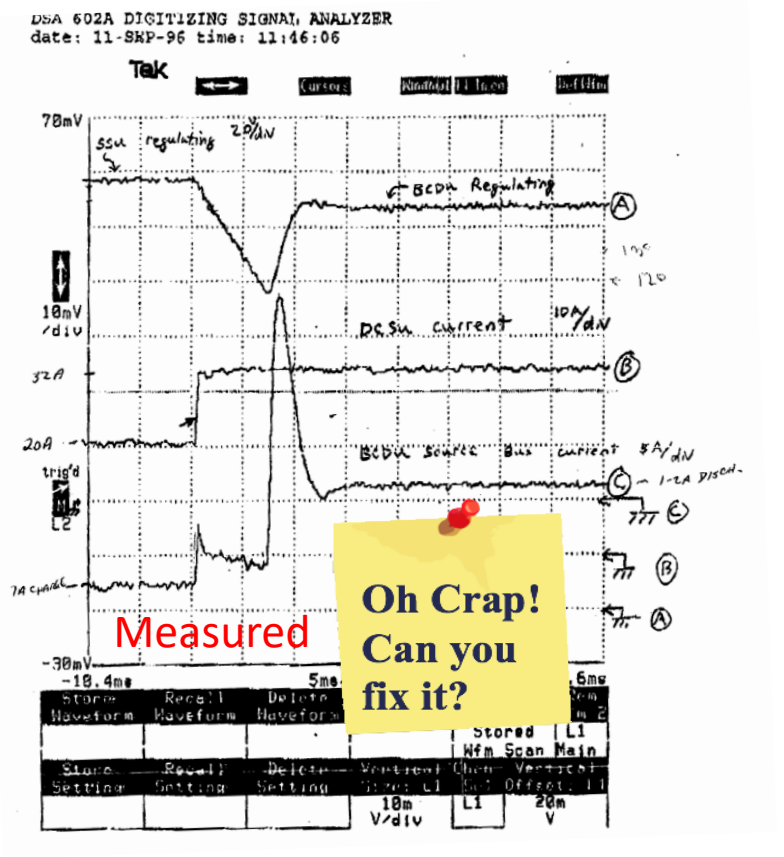
Measurement Based VRM Modeling

Speaker:

Steve Sandler, Picotest.com

BIG CHALLENGES YIELD BIG BENEFITS



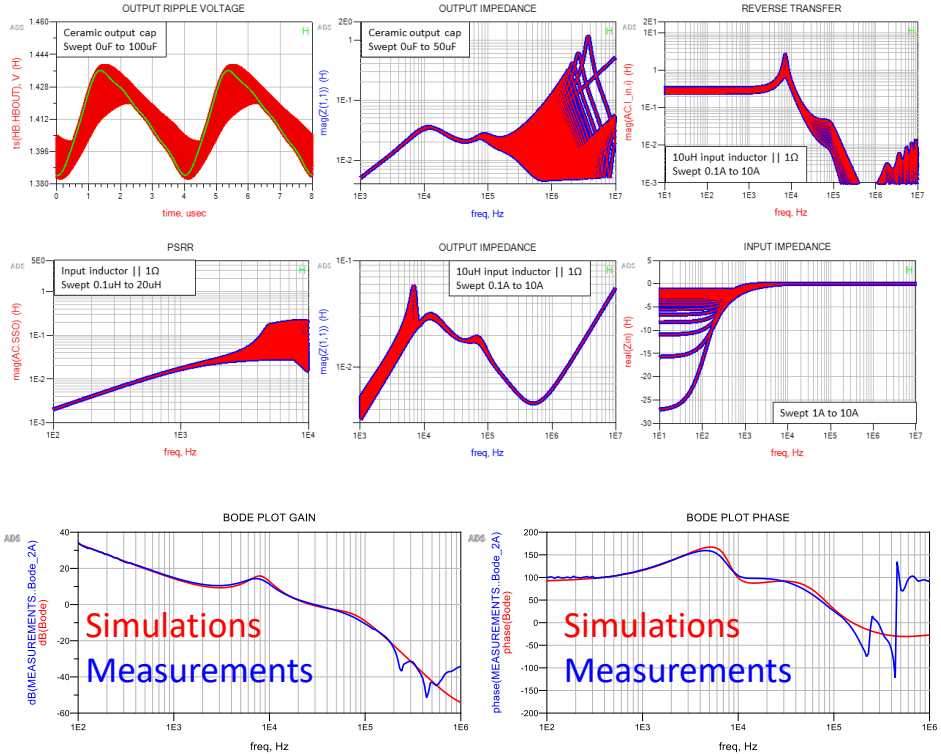


LESSONS I'VE LEARNED

- The power supply or VRM interacts with the system at both the inputs and the outputs
- A good, fast-running simulation now is better than a perfect simulation later
- The key to efficient modeling is to create parameterized, reusable blocks
- Know the limitations of the models you use
- Measurement is a key element in creating accurate models. This is even more essential when we model circuits that we can't measure

Why Full VRM Characterization is Essential, Sandler, Signal Integrity Journal July 25, 2019

Simulations



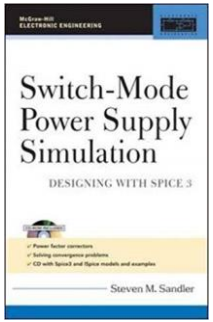
ABOUT THE MODEL I'LL SHARE TODAY

I wrote a VRM model for my own use in 1990 and published it in 1996. It's been republished three times, including once in Chinese. There were lots of great models by then, so why did I make my own?

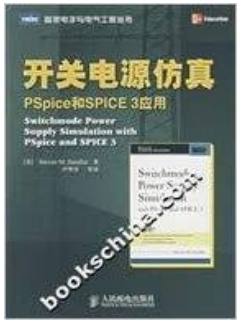
- Most models were small signal models, intended for AC simulation. Large signal was essential too!
- Separate models were used for continuous and discontinuous conduction mode. Huge problem here!
- Most models required a lot of math and time to create - I wanted a simple, quick-to-generate parameterized model
- It also has limitations, which I will share with you

1996

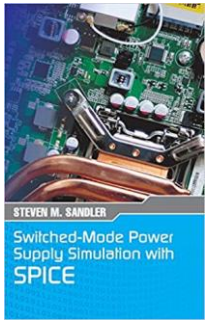
2005



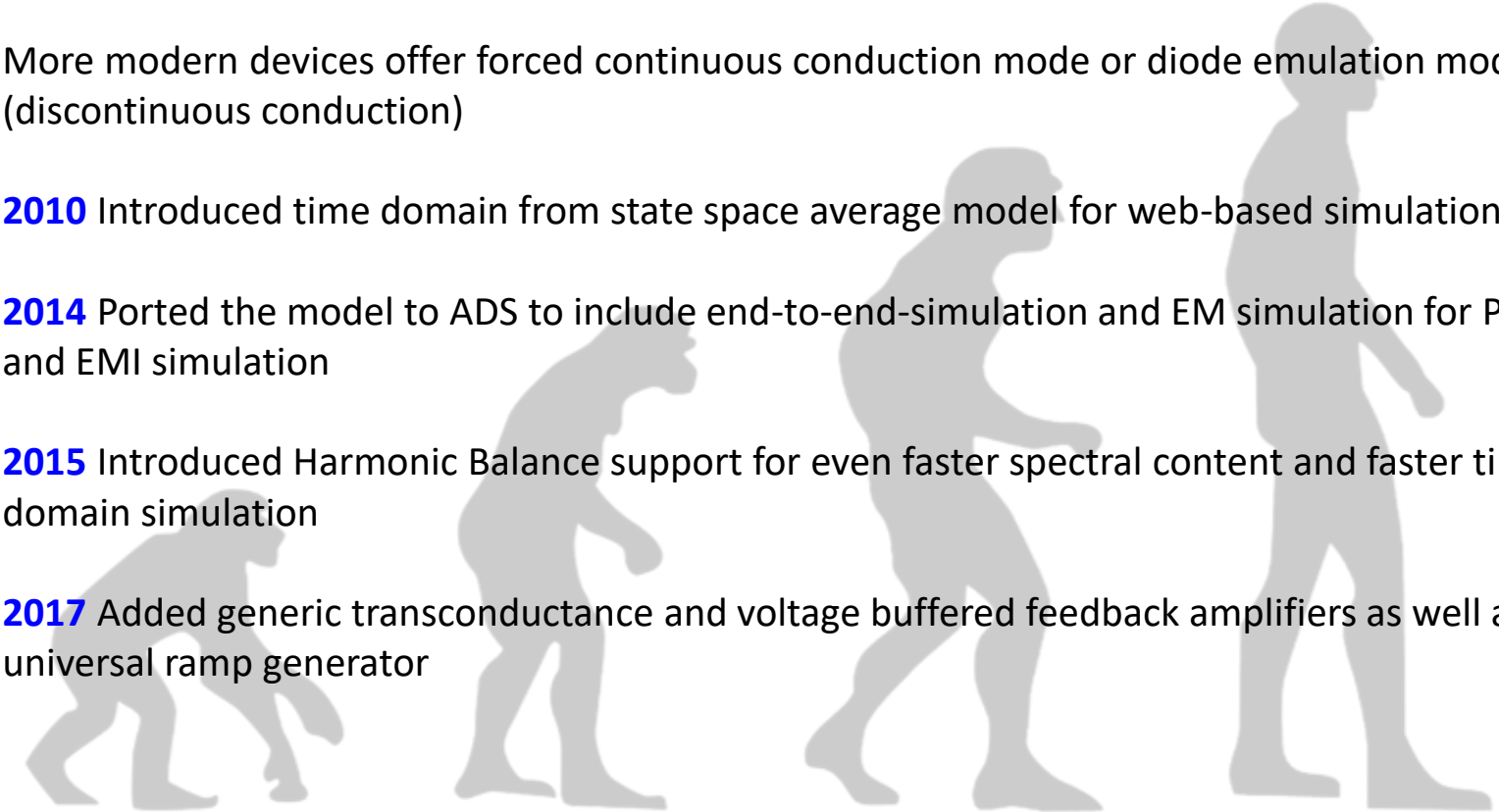
2010



2018



IT'S CONTINUOUSLY EVOLVING



More modern devices offer forced continuous conduction mode or diode emulation mode (discontinuous conduction)

2010 Introduced time domain from state space average model for web-based simulation

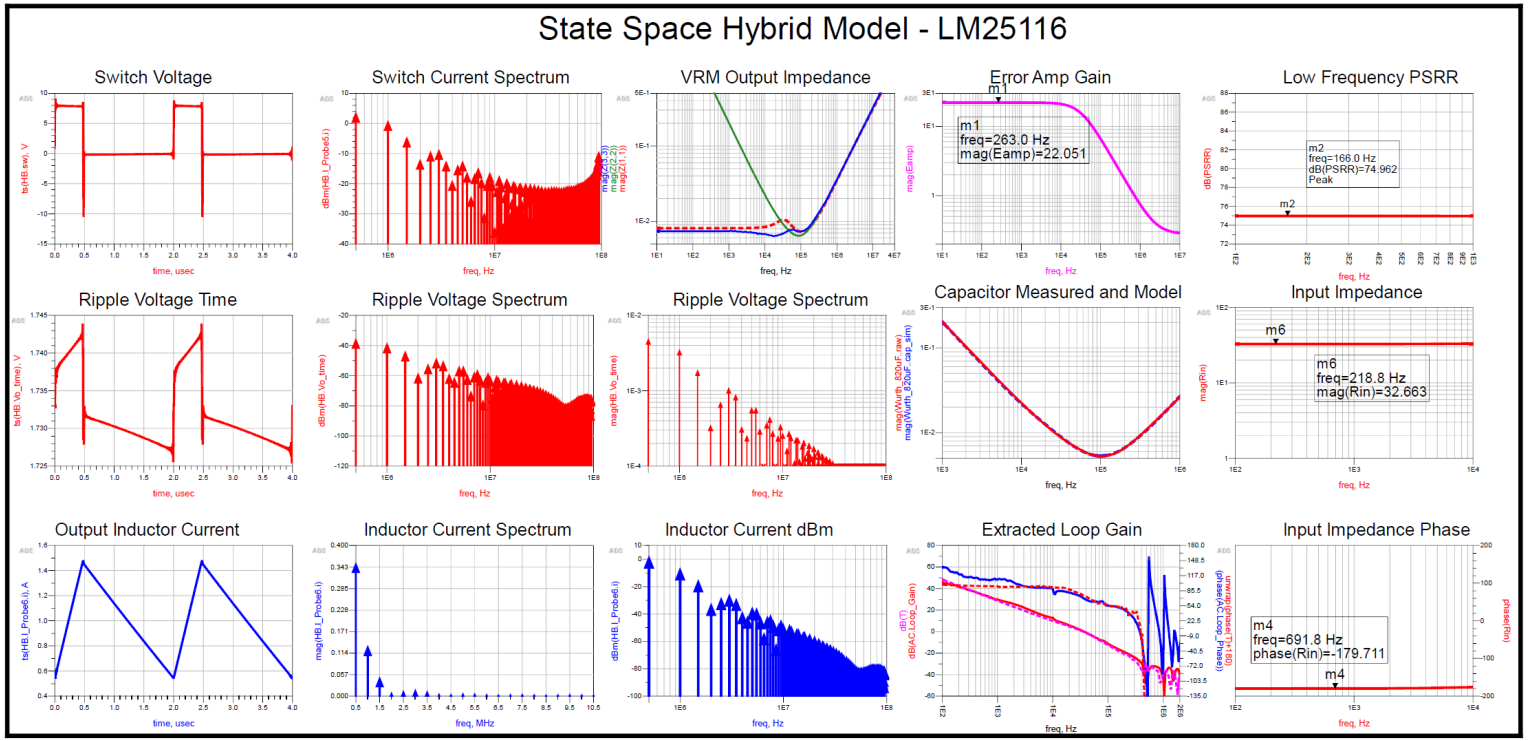
2014 Ported the model to ADS to include end-to-end-simulation and EM simulation for PCB effects and EMI simulation

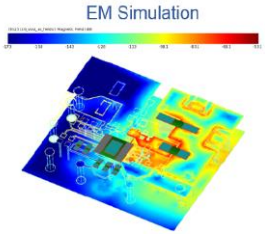
2015 Introduced Harmonic Balance support for even faster spectral content and faster time domain simulation

2017 Added generic transconductance and voltage buffered feedback amplifiers as well as a universal ramp generator

TIME, SPECTRUM AND FREQUENCY

Models Small Signal and Large Signal Behavior Simultaneously!



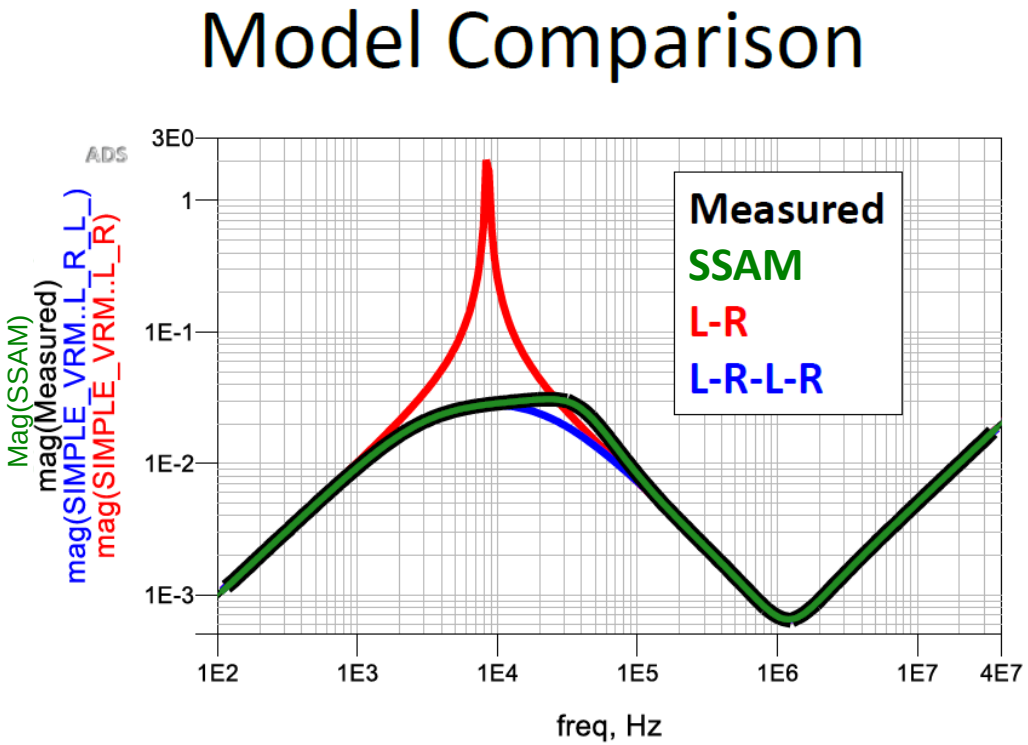


Why a State-Space Average (SSAM) VRM Model is Better

- Ideal V_{source} has wrong output impedance
- R-L model only models output impedance and not with good accuracy
- RLC model only models output impedance with no information on switching noise, PSRR, stability, etc.
- State Space Average Model does it all and it is measure based and verified for the application.
  - ✓ The math is already done and free to use! Just add the parameters.

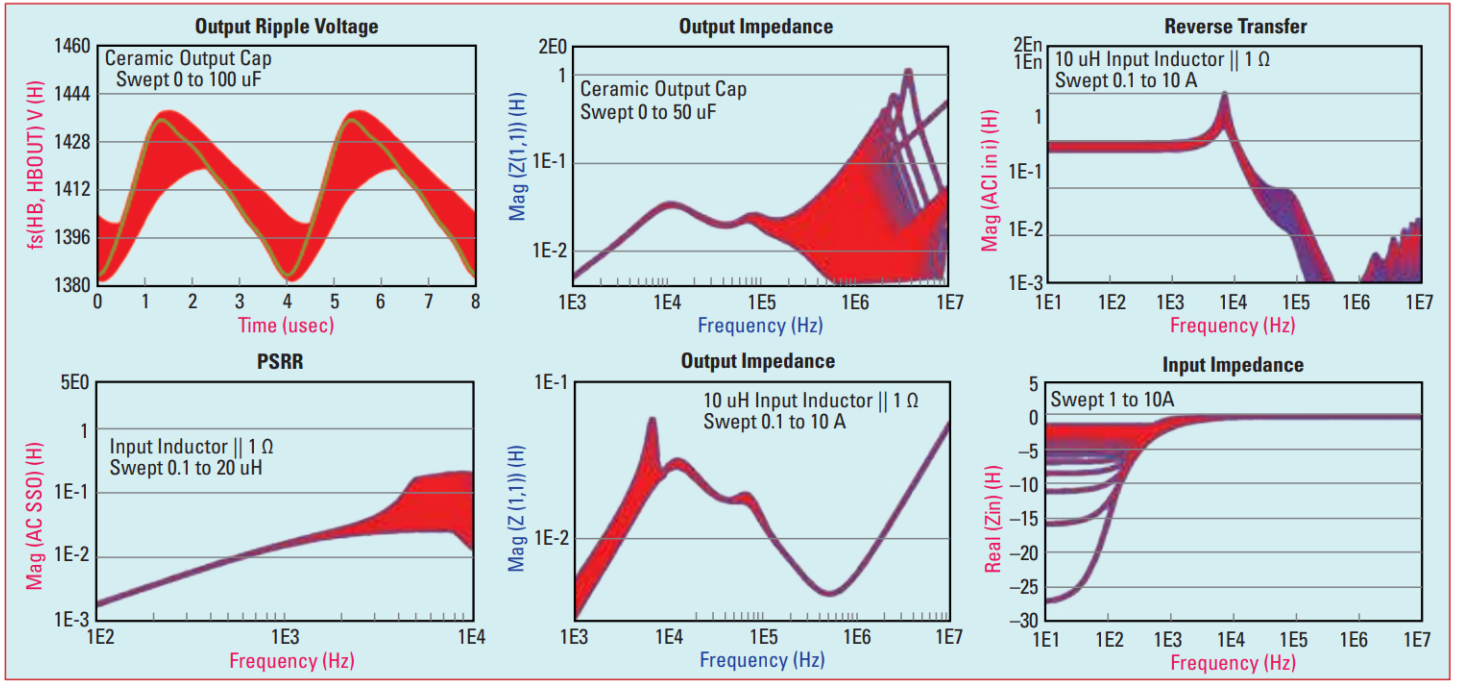
	V Source	L-R	L-R-L-R	SSAM
PDN Impedance	INCORRECT RESULT	NOT WELL	REASONABLY	Y
Switching ripple	N	N	N	Y
PSRR/Transients	N	N	N	Y
Negative resistance	N	N	N	Y
Input switching current	N	N	N	Y
Control loop stability	N	N	N	Y
Turn on overshoot	N	N	N	Y
Remote sense	N	N	N	Y

How Bad Can a Simple VRM Model Be?



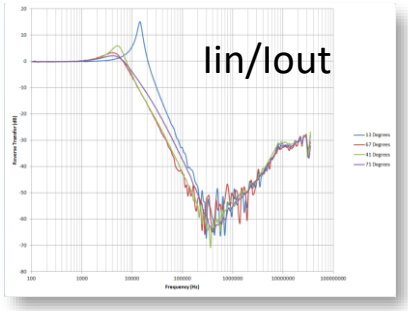
All Noise Sources with an SSAM VRM Model

State-space average behavioral VRM model predicts performance over process variations.

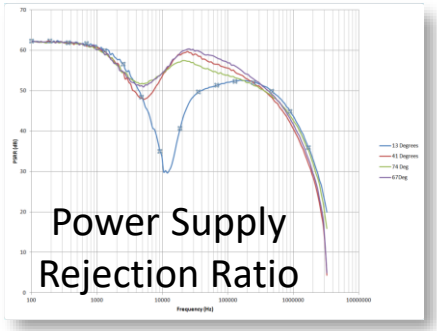


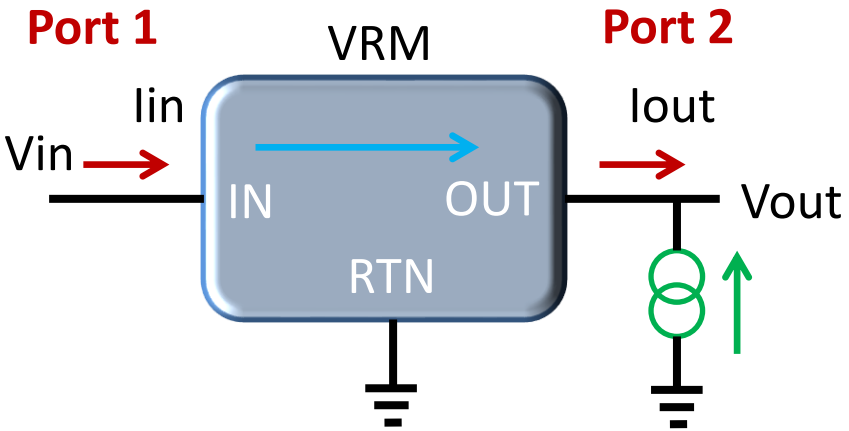
The Voltage Regulator Module (VRM) needs to consider <u>ALL</u> noise sources (large and small signal EMI)

Reverse Transfer - (S12)



PSRR - (S21)



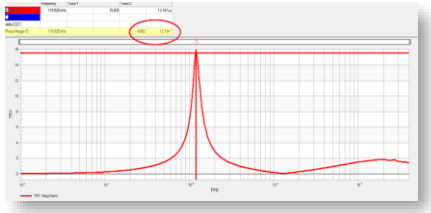


Input Impedance - (S11)

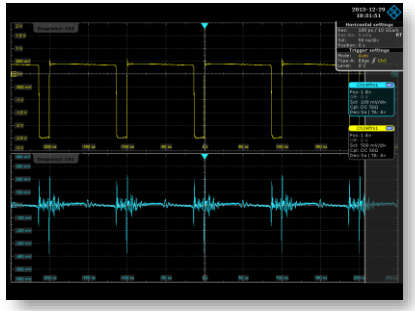
Input impedance can be NEGATIVE!

An R-L model only considers the output impedance

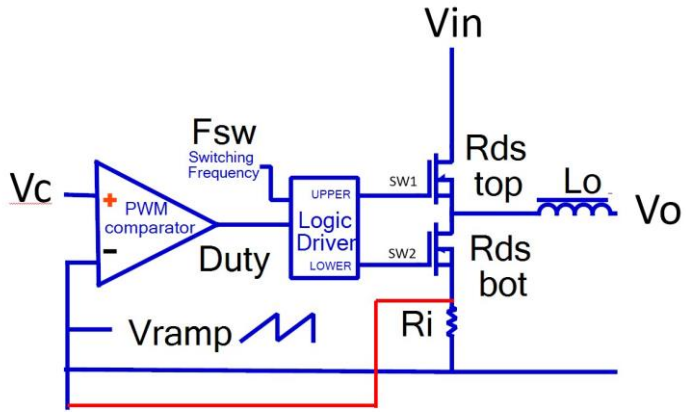
Output Impedance - (S22)

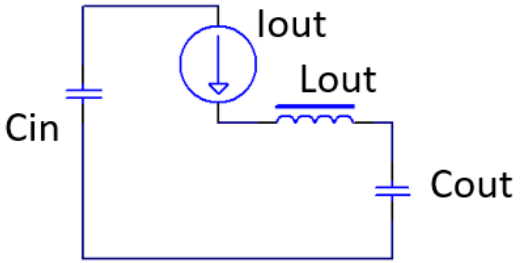


Output Noise/Spikes



What is a State-Space Average (SSAM) VRM Model





State 1: SW1 = On and SW2= Off

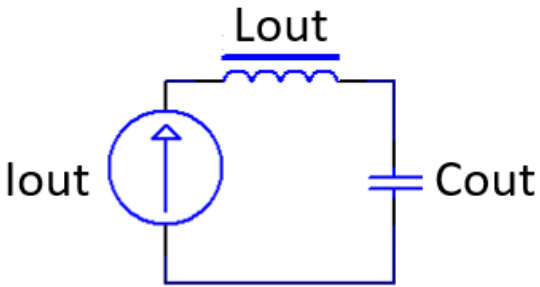
STATE SPACE AVERAGED MODEL

$$Duty = Ton\_SW1 \cdot Fsw$$

$$Vout = Vin \cdot Duty$$

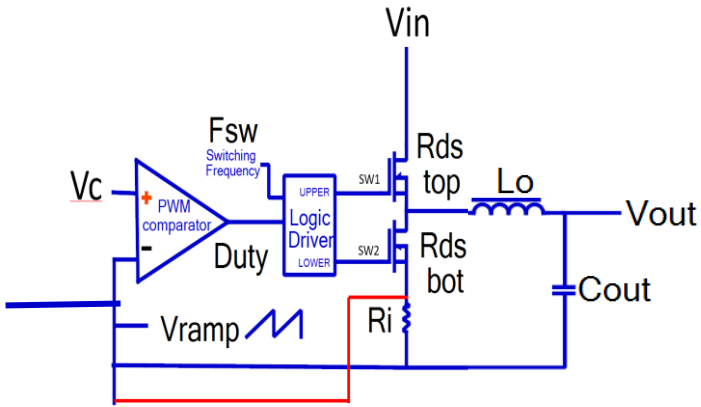
CURRENT MODE

$$Iout = k\frac{Vc}{Ri}$$



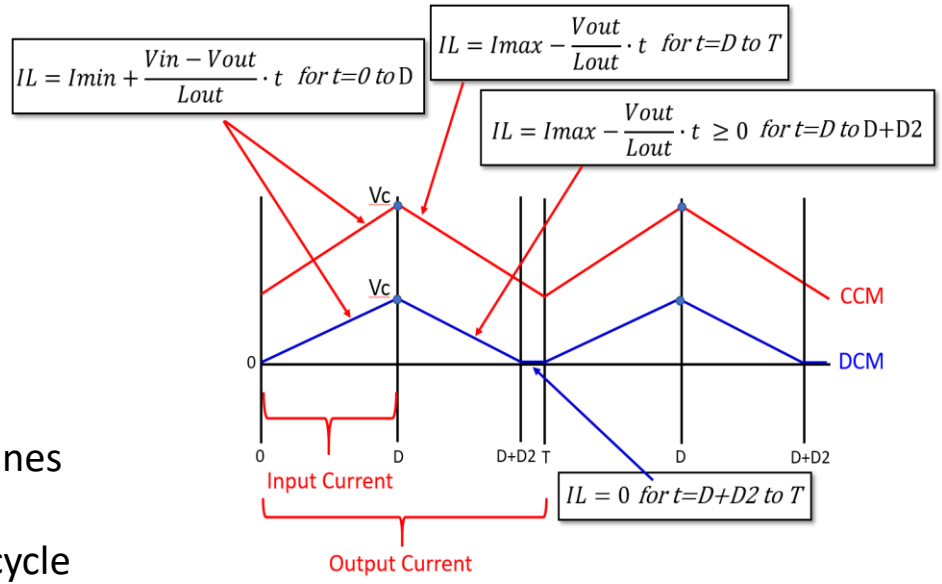
State 2: SW1 = Off and SW2= On

THE INDUCTOR CURRENT EQUATIONS



Switching models operate as state machines

There are generally 2 known points per cycle and the rest are linearly interpolated



Continuous Conduction Mode
Discontinuous Conduction Mode

DIFFERENT MODES DIFFERENT EQUATIONS

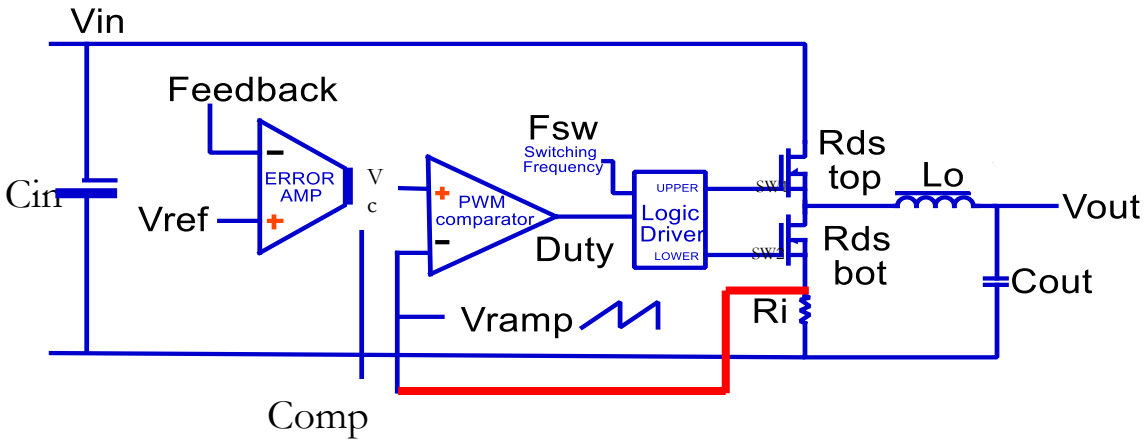
CCM	DCM
$Iout = \frac{Imin + Imax}{2}$	$Iout = \frac{Imax}{2} \cdot (D + D2)$
$Iin = \frac{Imin + Imax}{2} \cdot D$	$Iin = \frac{Imax}{2} \cdot D$
$Vout = \frac{Vin \cdot D}{1 - D}$	$Vout = \frac{Vin \cdot D}{2 \cdot D + D2}$

DC Voltages and Currents are averaged over the switching cycle

A UNIFIED STEP-DOWN REGULATOR MODEL

For a model to be helpful, it needs to be easy to implement and simulate quickly
A simple, parameterized model can represent most performance characteristics

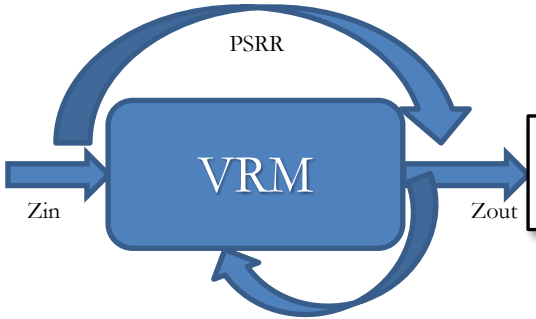
- Voltage Mode Control
- Current Mode Control
- Discontinuous Conduction Mode
- Continuous Conduction Mode
- Large Signal
- Small Signal



THE STATE SPACE EQUATIONS

Parameter	Description
Lo	Output Filter Inductance
Vc	Error Amp Output Voltage
Fsw	Switching Frequency
Vin	Input Voltage
Vo	Output Voltage
DCR	Output Filter Inductor DCR
RDSon	Mosfet RDSon
Ri	Current Sense Resistance
Vramp	Slope Comp/Ramp
Av	Feedback Amplifier Gain

$$PSRR\_dB = 20log\left[\left|\frac{Vo\cdot(Ri\cdot Vo - 2\cdot Fsw\cdot Lo\cdot Vramp}{Ri\cdot Vin^2 - 2\cdot Ri\cdot Vo\cdot Vin + 2\cdot Fsw\cdot Lo\cdot Vin\cdot Vramp + 2\cdot Av\cdot Fsw\cdot Lo\cdot Vin}\right|\right]$$



$$Rout = \frac{\frac{2\cdot Fs\cdot Lo\cdot Ri\cdot Vin}{Ri\cdot Vin - 2\cdot Ri\cdot Vo + 2\cdot Fsw\cdot Lo\cdot Vramp} + DCR + RDSon}{1 + Av\cdot\frac{2\cdot Fs\cdot Lo\cdot Vin}{Ri\cdot Vin - 2\cdot Ri\cdot Vo + 2\cdot Fsw\cdot Lo\cdot Vramp}}$$

$$Lout = \frac{Lo}{1 + \frac{2\cdot Fsw\cdot Lo\cdot Vin}{Ri\cdot Vin - 2\cdot Ri\cdot Vo + 2\cdot Fsw\cdot Lo\cdot Vramp}\cdot Av}$$

$$Bode = \frac{2\cdot Fsw\cdot Lo\cdot Vin}{Ri\cdot Vin - 2\cdot Ri\cdot Vo + 2\cdot Fsw\cdot Lo\cdot Vramp}\cdot Av$$

$$Ri \cong \frac{\Delta Vc}{\Delta Io}$$

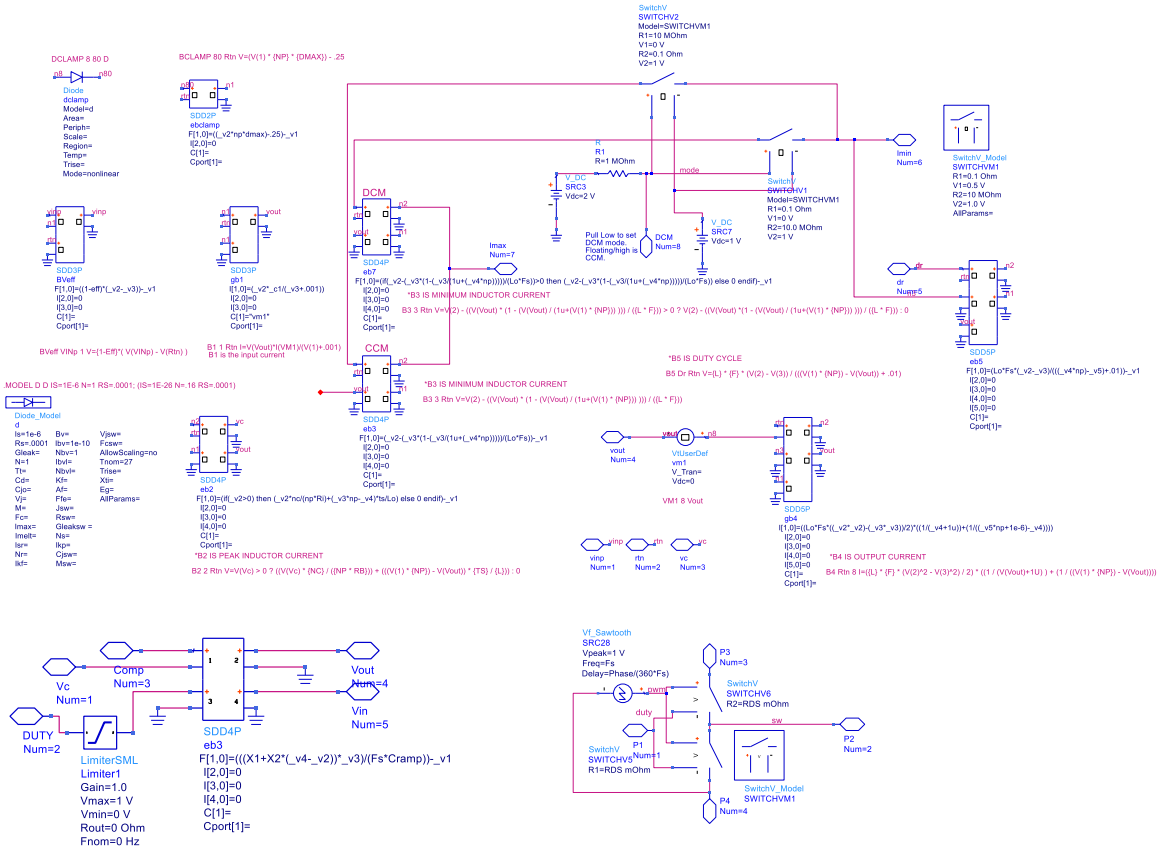
$$\frac{Vo}{Vc} = \frac{2\cdot Fsw\cdot Lo\cdot Vin}{Ri\cdot Vin - 2\cdot Ri\cdot Vo + 2\cdot Fsw\cdot Lo\cdot Vramp}$$

Frequency domain characteristics are determined by solving non-linear differential equations using a technique known as State Space Modeling

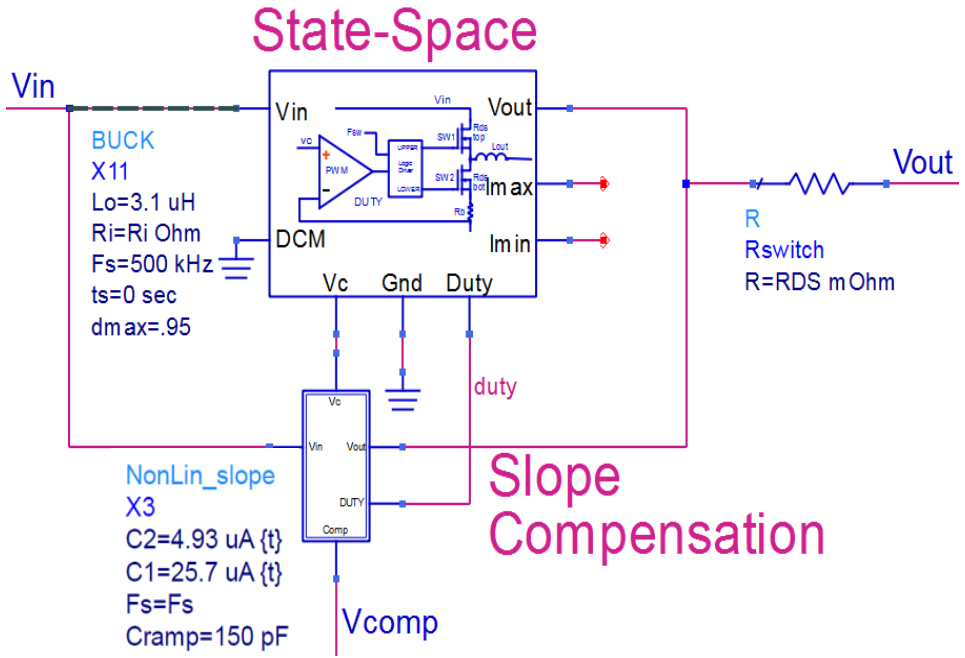
DON’T LET THE MATH SCARE YOU

The hard work of coding the math is already done for you

In fact, you don’t ever need to see these equations (though you can)



THE (LESS SCARY) PARAMETERIZED MODEL



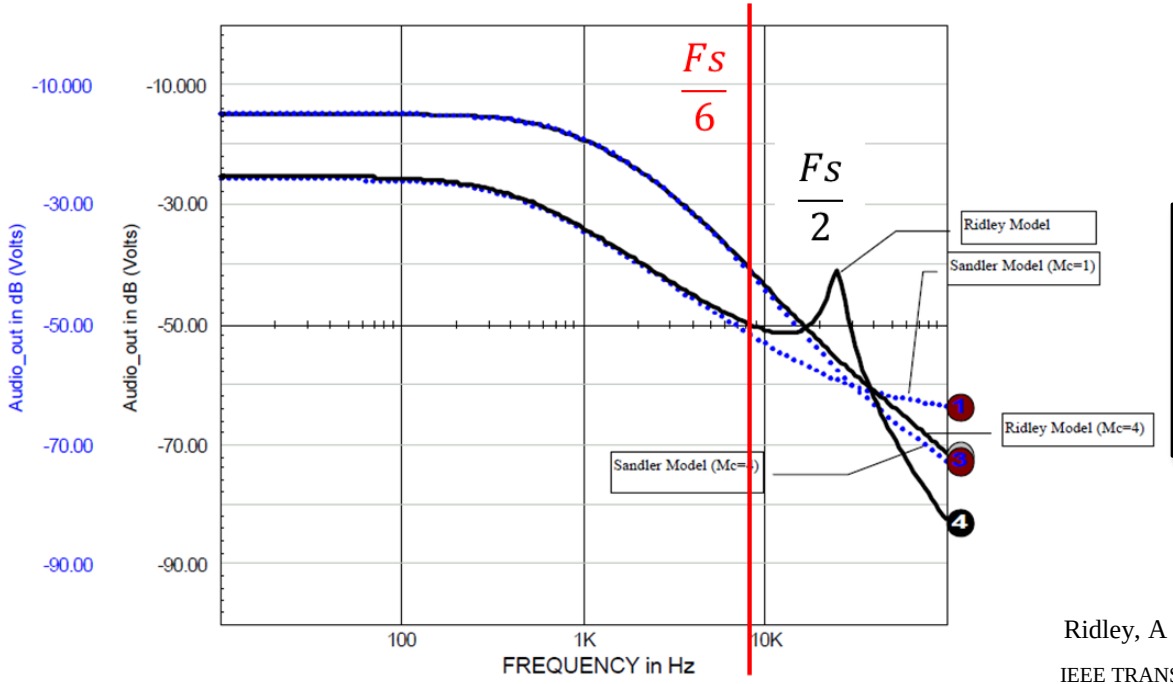
The math is inside these blocks. The required parameters are passed to the model

Just enter the parameter values, most of which are easily identified

We'll determine those that aren't easily identified using a few very simple measurements

$$Vramp = \frac{C1+C2\cdot(Vin-Vout)}{Fs\cdot Cramp}\cdot DUTY$$

Sandler State-Space Average Model Accuracy:
Predicting Audio Susceptibility with Ridley vs. Sandler

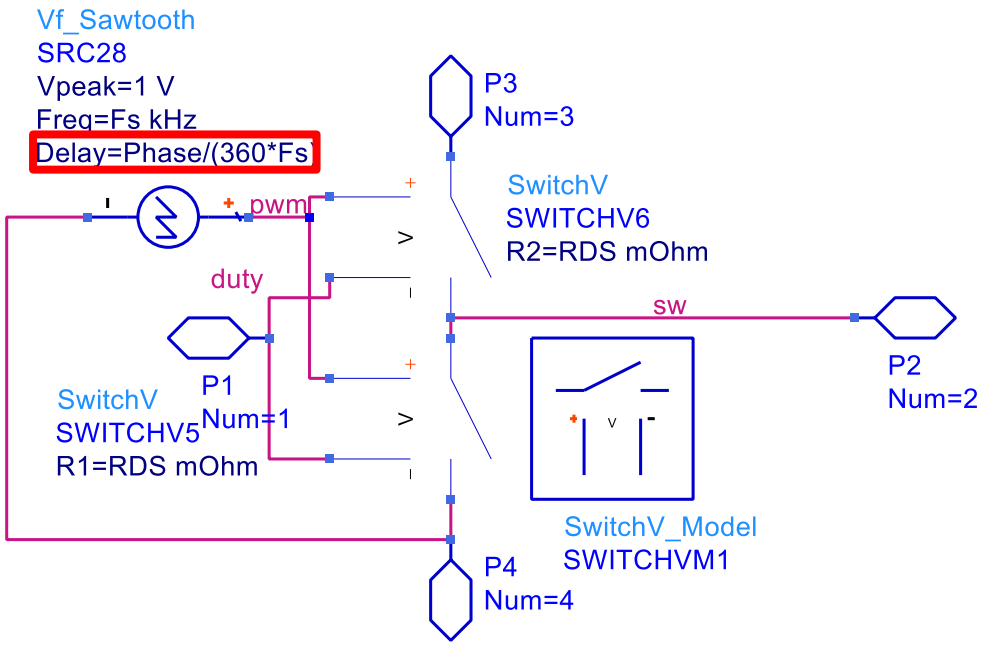


Accuracy is reduced for the Sandler State-Space Average VRM Model above Fs/6, but accurate where it matters!

Ridley, A New, Continuous-Time Model For Current-Mode Control

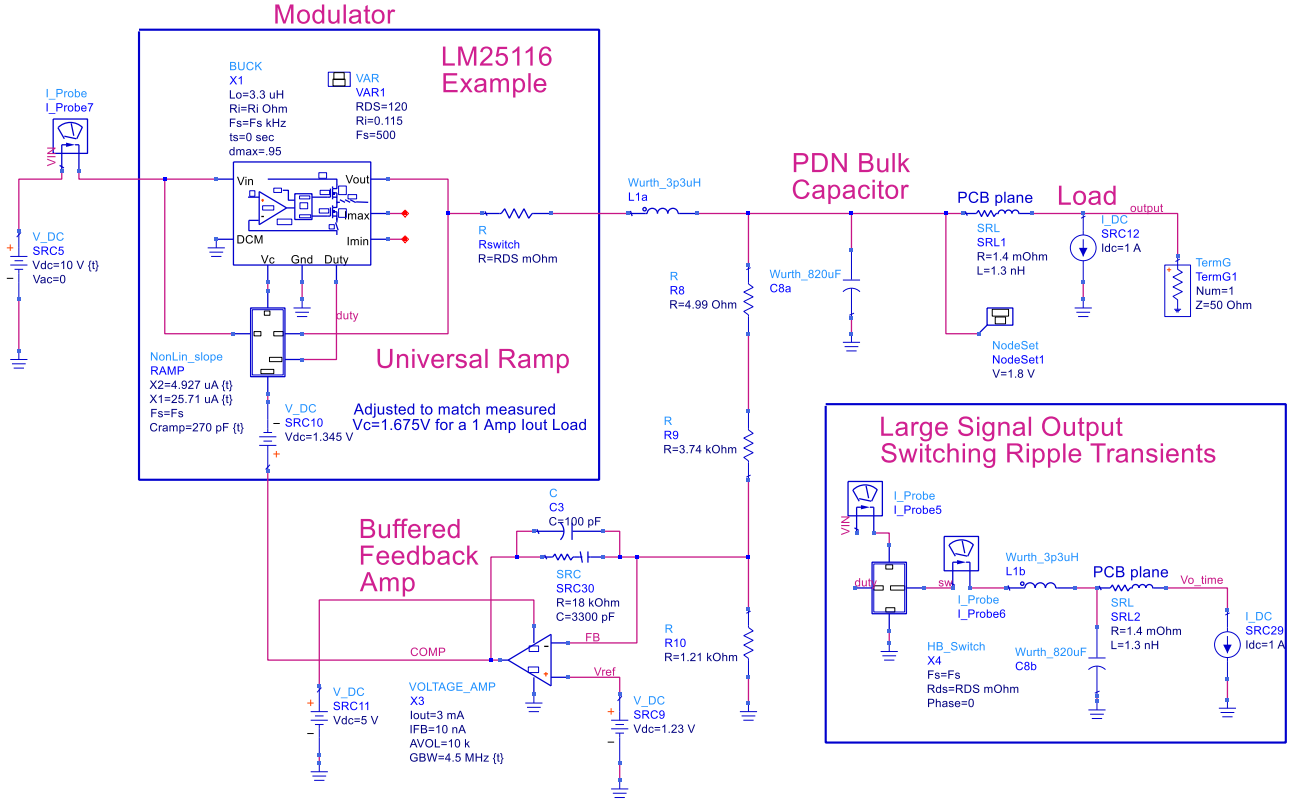
IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 6. NO. 2. APRIL 1991

ADDING TIME DOMAIN RESULTS



- The state space model knows the instantaneous duty cycle, or switch positions, at every instant in time
- A 1V ramp at the switching frequency converts the duty cycle to switch positions
- A delay is used to position independent phases in a multiphase system

COMPLETE PARAMETERIZED MODEL



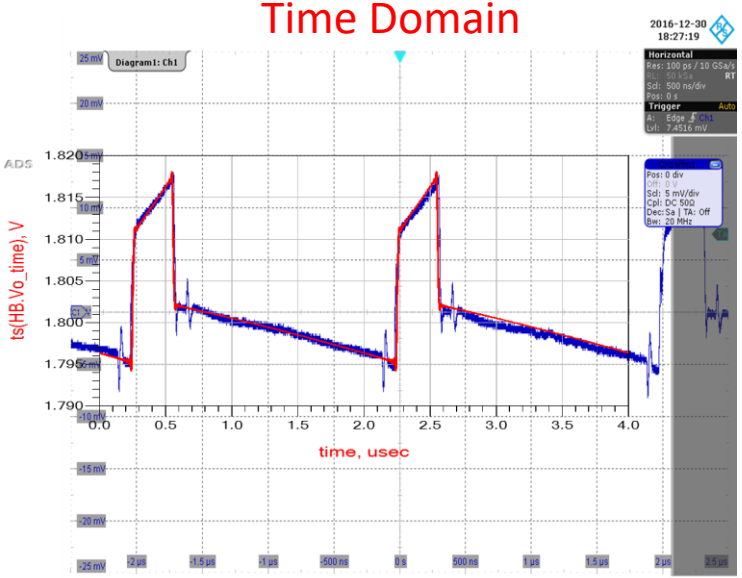
Three Separate Simulations in one Schematic

Note that the output network, including the output inductor, capacitors (and the PCB if included) must be EXACTLY replicated in the state space and large signal models.

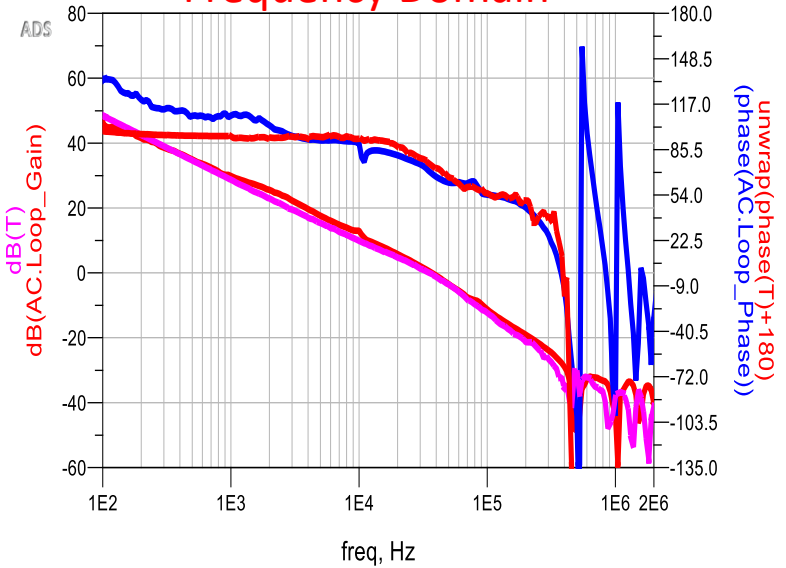
TIME DOMAIN AND FREQUENCY DOMAIN

Simulation vs. Measurement

Time Domain



Frequency Domain



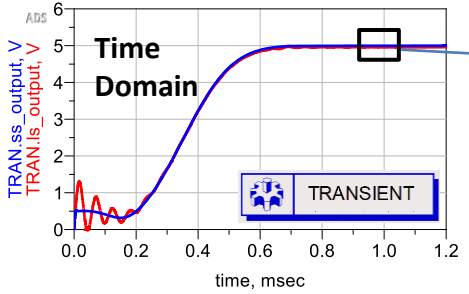
You must admit those match well, right?

Why use the Harmonic Balance Simulator with SSAM

- Fourier Theory says time domain waveforms are made up of frequency domain waveforms.
- Solving a circuit in the Frequency Domain can be much faster since it limits the frequencies and jumps to steady state.

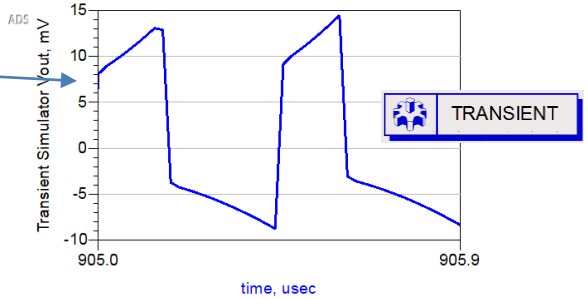
Transient must reach steady state to measure ripple.
50,000 time-steps!

Simulator Results

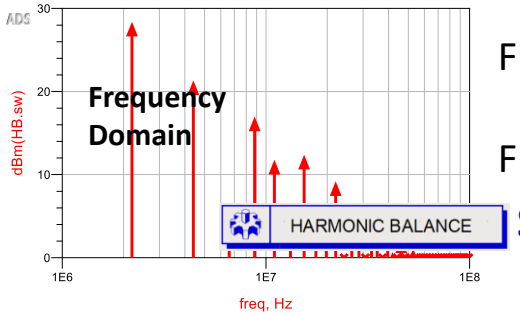


Time Domain
Transient Sim
Wait for Steady State
Minutes, Hours, **Days**

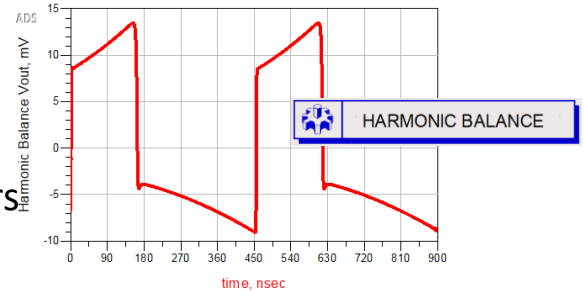
Steady State Ripple vs. Time



Harmonic Balance simulates harmonics of the switching frequency.
Only 255 Frequencies for steady state ripple!

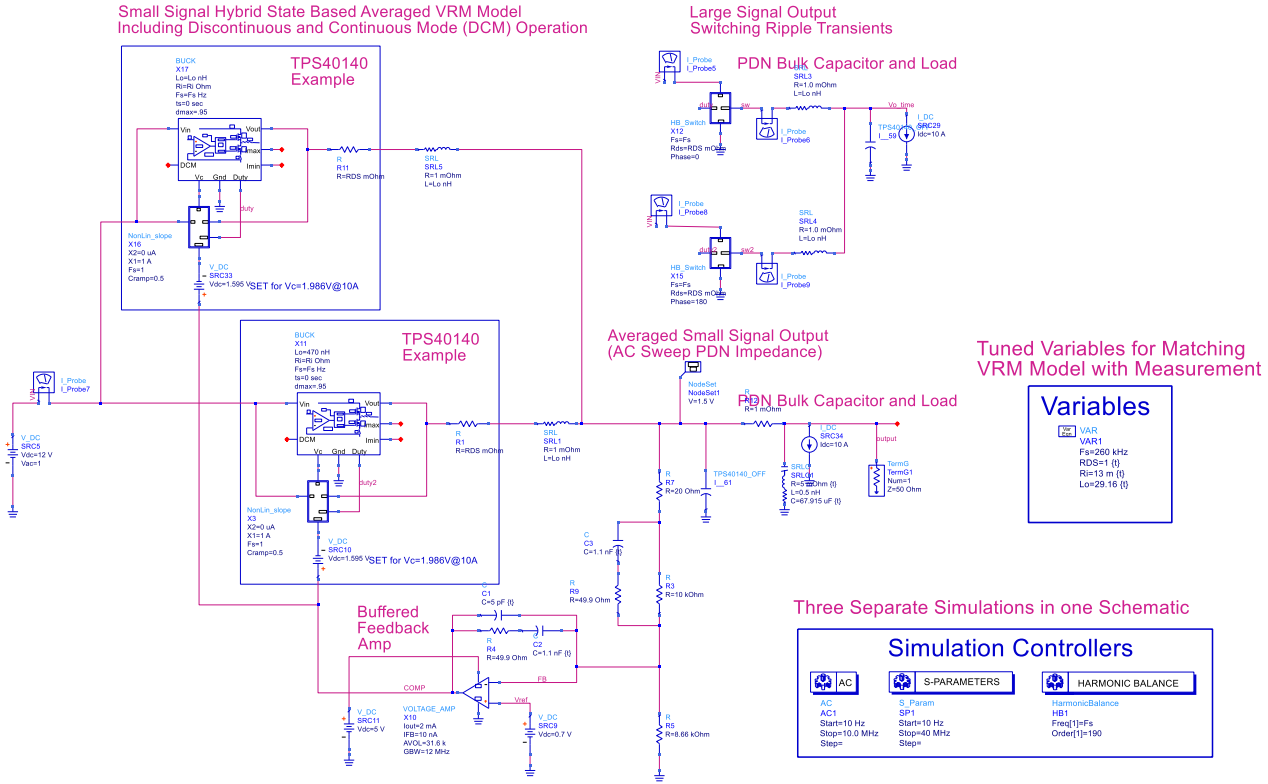


Frequency Domain
Harmonic Balance Sim
FFT jumps to Steady State
Seconds, Minutes, Hours



Data shown is for one VRM, typical PCB design has dozens of VRMs

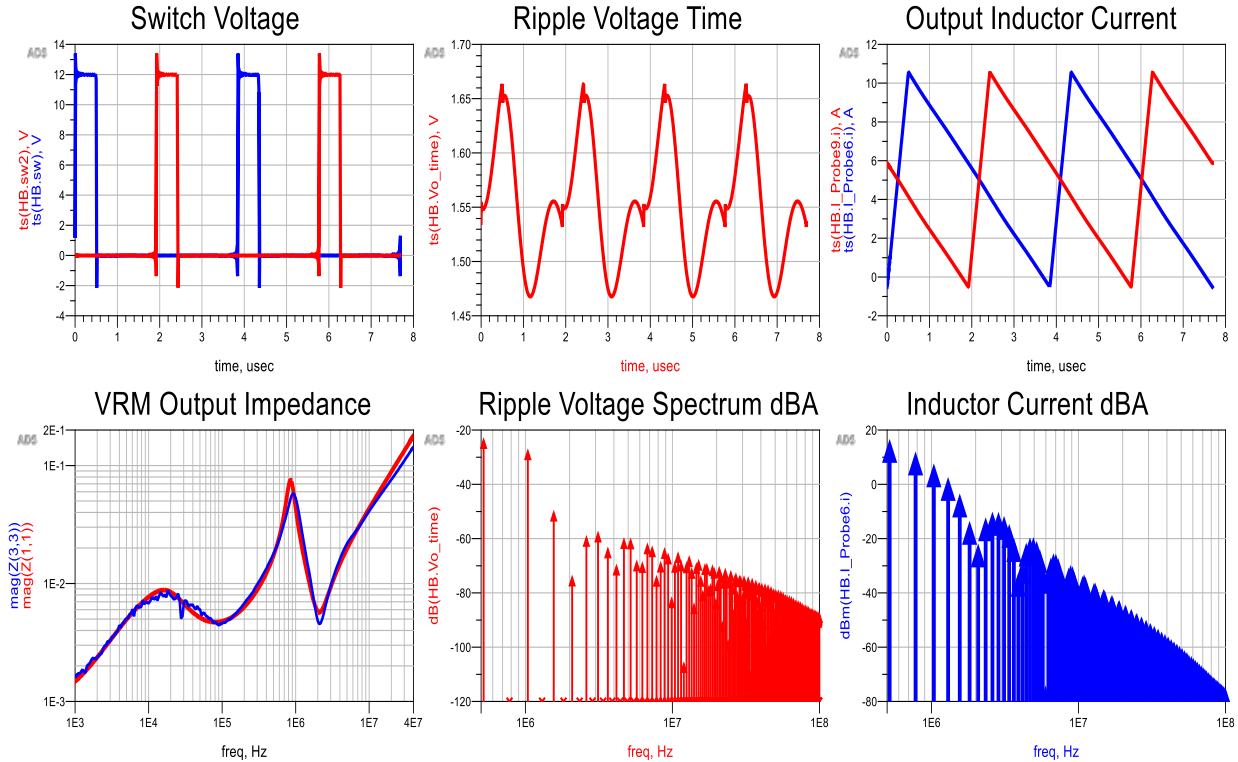
MULTI-PHASE SUPPORTABLE



- Many (if not most) systems today include multi-phase VRMs
- It's important for a generic unified model to support multiphase designs
- My model can do this with synchronized or unsynchronized VRMs, including parameterized phase relationships

N-PHASE FOR TIME, SPECTRUM, FREQUENCY

Multiphase Time, Frequency, and Spectrum Data Simultaneously



A FEW RULES MAKE THIS MODELING SIMPLE

- Ideally, select a part with feedback amplifier connections, but, at minimum, external Comp pin
- If you don’t know Lo, purchase a sample, mount it, and measure it
- If you don’t know RDSon and DCR, they are measurement, but have low impact, so it is ok to guesstimate
- Discontinuous Conduction Mode (Diode or Diode Emulation) should be in the datasheet or is selectable
- Continuous Conduction Mode should be in the datasheet or is selectable
- Vramp may be external, if so, you can measure it on a scope
- Ri may be external, but measure the change in Vcomp vs Iout even if it is external

The two parameters that can be difficult to obtain are Vramp and Ri

MODEL PARAMETERS

Parameter	Description	Comments
Lo	Filter Inductor	We likely know this, but easily measured with a VNA or Scope with FRA features
Fsw	Switching Frequency	We likely know this, but can easily measure it using an oscilloscope
Vc	Error Amp output voltage	If this is accessible it is really helpful for directly determining Ri, but also for optimizing the control loop response
Vin	Input Voltage	We should know this, since it is externally set, but can measure with a DMM
Vo	Output Voltage	We should know this, since it is externally set, but can measure with a DMM
DCR	Inductor DCR	We likely know this, but easily measured with a VNA (low impact)
RDSon	Mosfet RDSon	We likely know this, but easily measured with a VNA (low impact)
Ri	Current Sense	Often considered proprietary. This is equal to $\frac{\Delta Vc}{\Delta Io}$, but easily determined from a VNA measurement
Vramp	Slope Comp/Ramp	Often considered proprietary, but easily determined from a VNA measurement
Av	Feedback Amplifier	Often external. Not always accessible, measurable with a VNA if COMP is available
Zcap	Output Cap Impedance	We might know this, but easily measured with a VNA*

** If capacitance is mostly or all ceramic, need to measure with DC Bias applied*

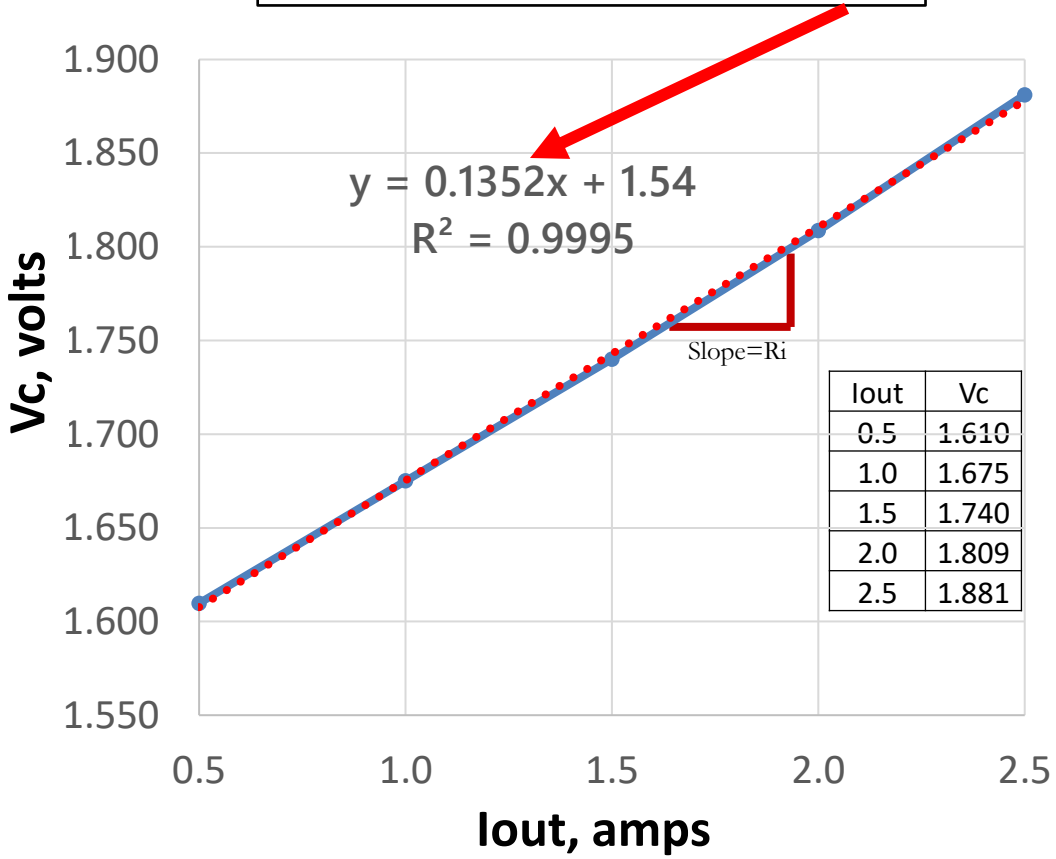
A LOW-COST CHARACTERIZATION BOARD

- Manufacturers offer EVAL or DEMO boards for many of their parts
- These don’t usually provide good measurement access
- We generally create our own low-cost characterization boards, with good measurement access, such as SMA connectors

MEASURING Ri DIRECTLY

- The measured result doesn't always agree with the datasheet
- This is often, as the case is here, due to PCB parasitics. Earlier, I told you that the PCB can impact even the DC performance
- Always measure an assembled PCB to optimize this model parameter
- For a Voltage Mode converter, the value of Ri should be very close to zero

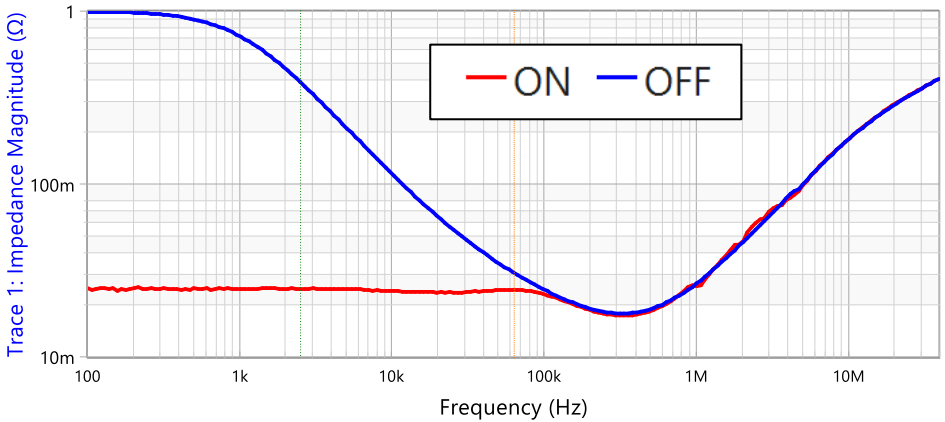
$$Ri = Rcs \cdot Acs = 10m\Omega \cdot 10 = 0.1\Omega$$



Iout	Vc
0.5	1.610
1.0	1.675
1.5	1.740
2.0	1.809
2.5	1.881

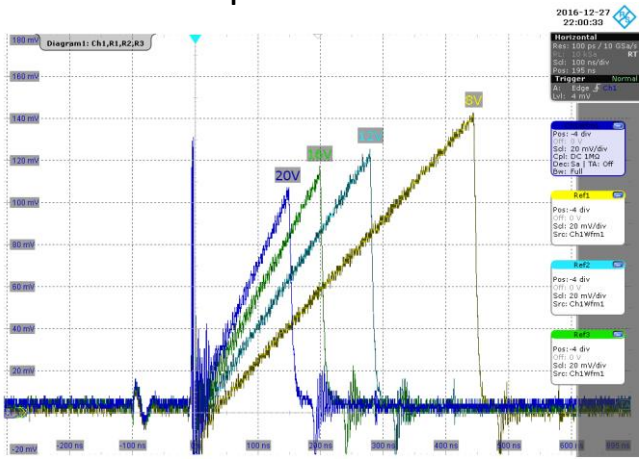
DETERMINE Ri INDIRECTLY

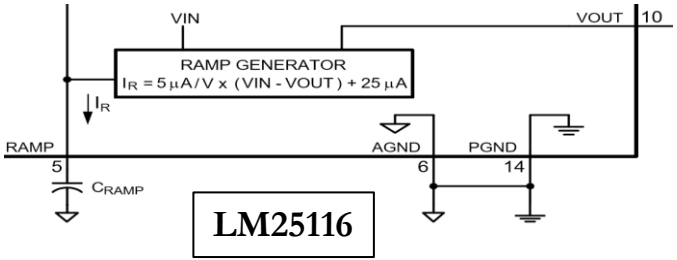
- If you can't measure PSRR then output impedance is a good second option.
- And of course, you can't have too much data, so feel free to measure both PSRR and output impedance.
- It is difficult to see the inductance in a well tuned converter. Reducing the output capacitance will make it easier to determine



ONLY VRAMP IS LEFT TO BE DETERMINED

- In some cases, the ramp is defined in the datasheet
- If the pin is accessible, it can be directly measured using an oscilloscope





$$Vramp = \frac{(Vin - Vout) \cdot 5uA + 25uA}{Fs \cdot Cramp}$$

A generic ramp generator supports constant ramp slope as well as Vin dependent (feedforward) and Vin-Vout dependent slopes

$$0.166 = \frac{X1 + X2 \cdot (8 - Vo)}{Cramp \cdot Fs} \cdot \frac{Vo}{8}$$

$$0.157 = \frac{X1 + X2 \cdot (12 - Vo)}{Cramp \cdot Fs} \cdot \frac{Vo}{12}$$

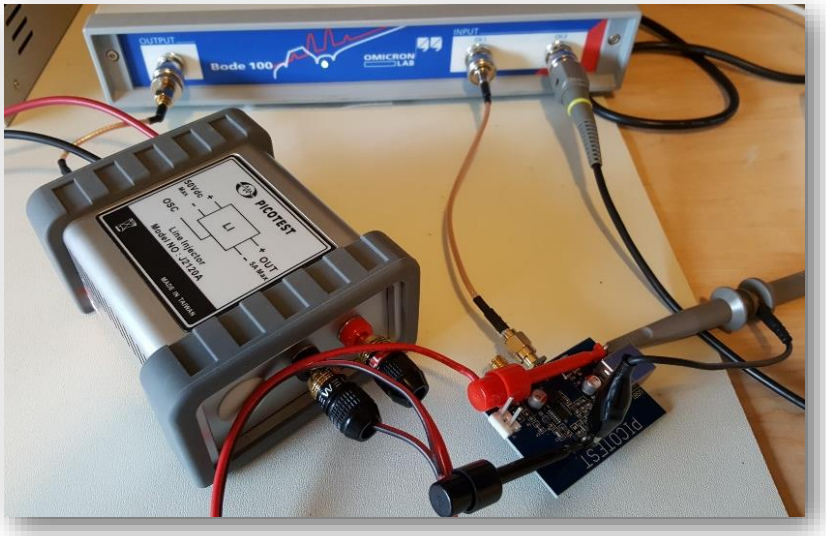
$$0.1467 = \frac{X1 + X2 \cdot (16 - Vo)}{Cramp \cdot Fs} \cdot \frac{Vo}{16}$$

$$0.133 = \frac{X1 + X2 \cdot (20 - Vo)}{Cramp \cdot Fs} \cdot \frac{Vo}{20}$$

$$Minerr(X1, X2) = \begin{pmatrix} 2.571 \times 10^{-5} \\ 4.927 \times 10^{-6} \end{pmatrix}$$

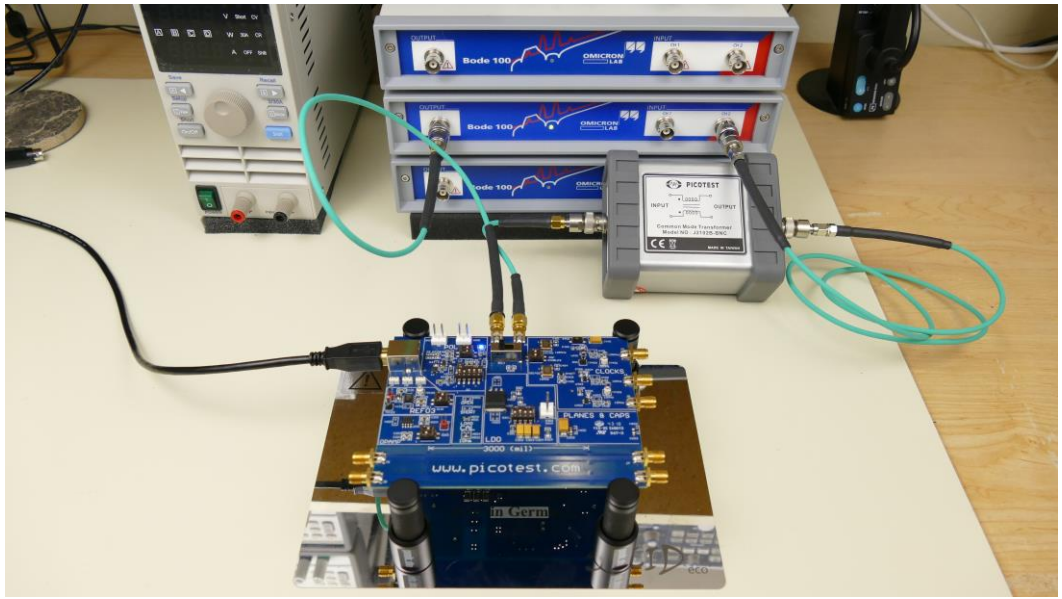
DETERMINE VRAMP WITHOUT ACCESS

- We are left with only a single unknown, Vramp
- We showed earlier that almost all closed loop performance is dependent on Vramp
- Vramp most heavily influences PSRR, so tune Vramp to match/optimize PSRR
- PSRR is a VECTOR, so be sure to measure and tune for correct magnitude AND phase!



DETERMINE VRAMP WITHOUT ACCESS

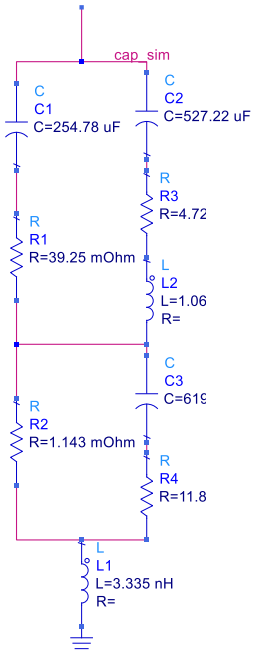
- If you can’t measure PSRR then output impedance, particularly inductance, is a good second option
- And of course, you can’t have too much data, so feel free to measure both PSRR and output impedance
- Tuning both Ri and Vramp should yield a perfect fit to the measured PSRR and output Z



MEASUREMENT BASED OUTPUT CAP MODEL

Measure

Model



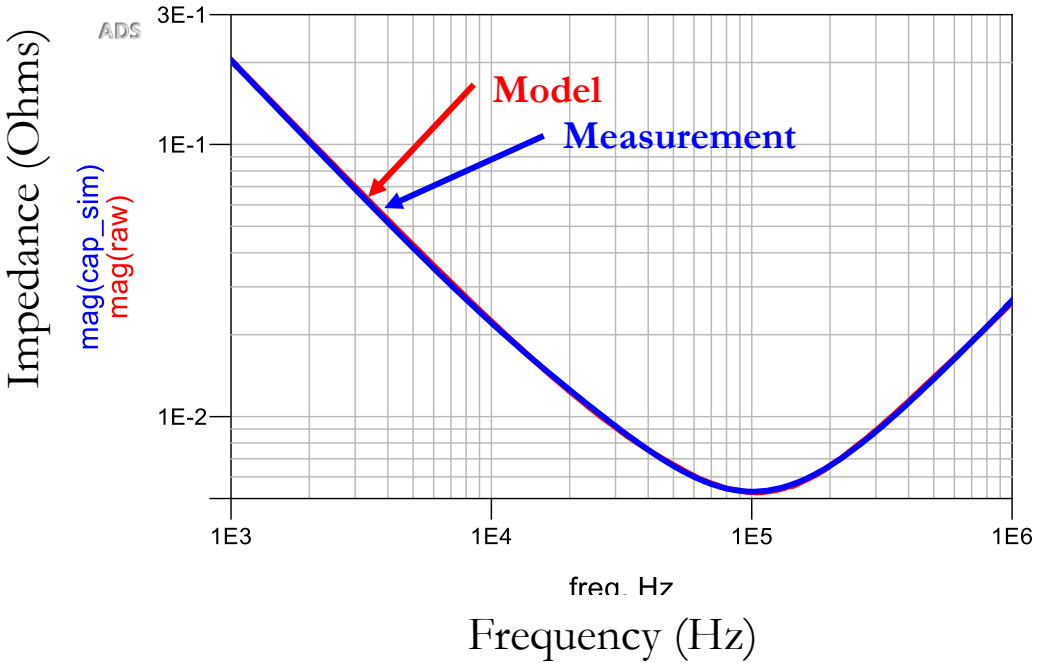
If your simulator can use S-parameters, just save the data to Touchstone format

If it can't, this video shows how to create a SPICE model from the data

http://tinyurl.com/capacitor-video

YouTube Video: How to Design for Power Integrity: Measuring, Modeling, Simulating Capacitors and Inductors

Capacitor Model Matches Measurement

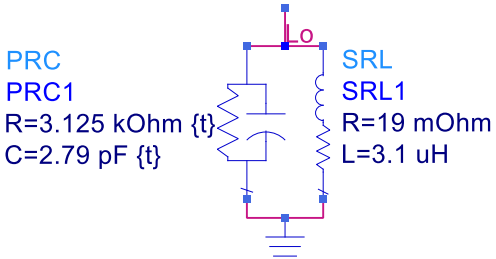


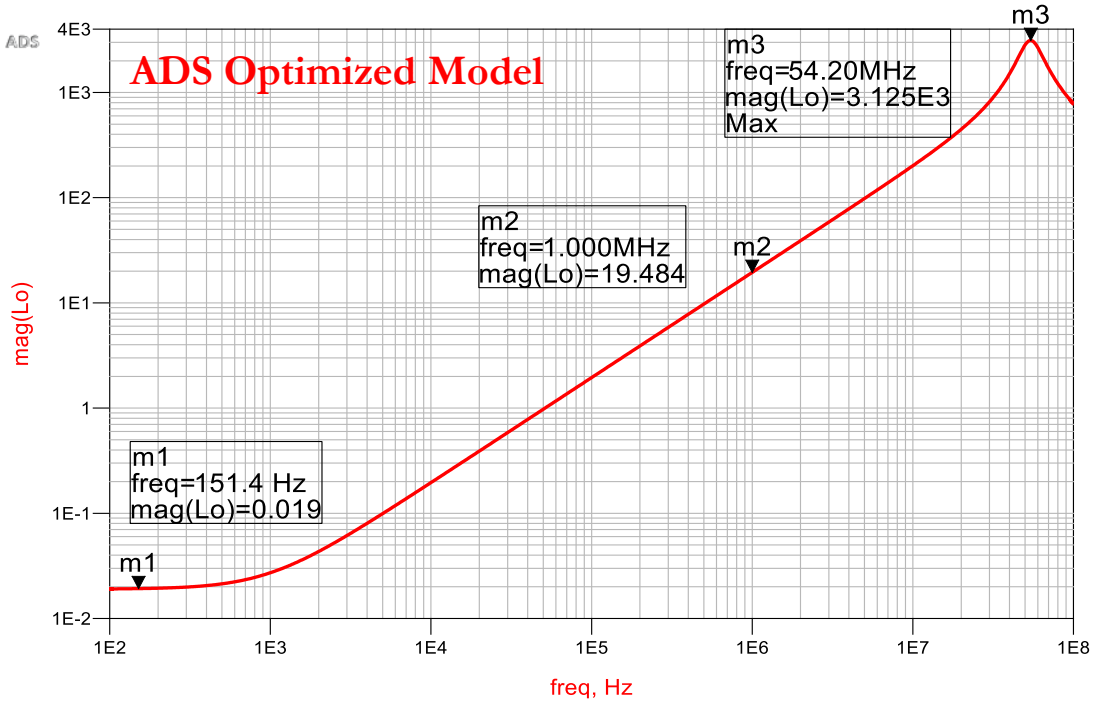
INDUCTOR MEASURMENT BASED MODEL

The datasheet values for the output inductor are usually ok, but if you want better fidelity, it's easy to measure

Measure

Model



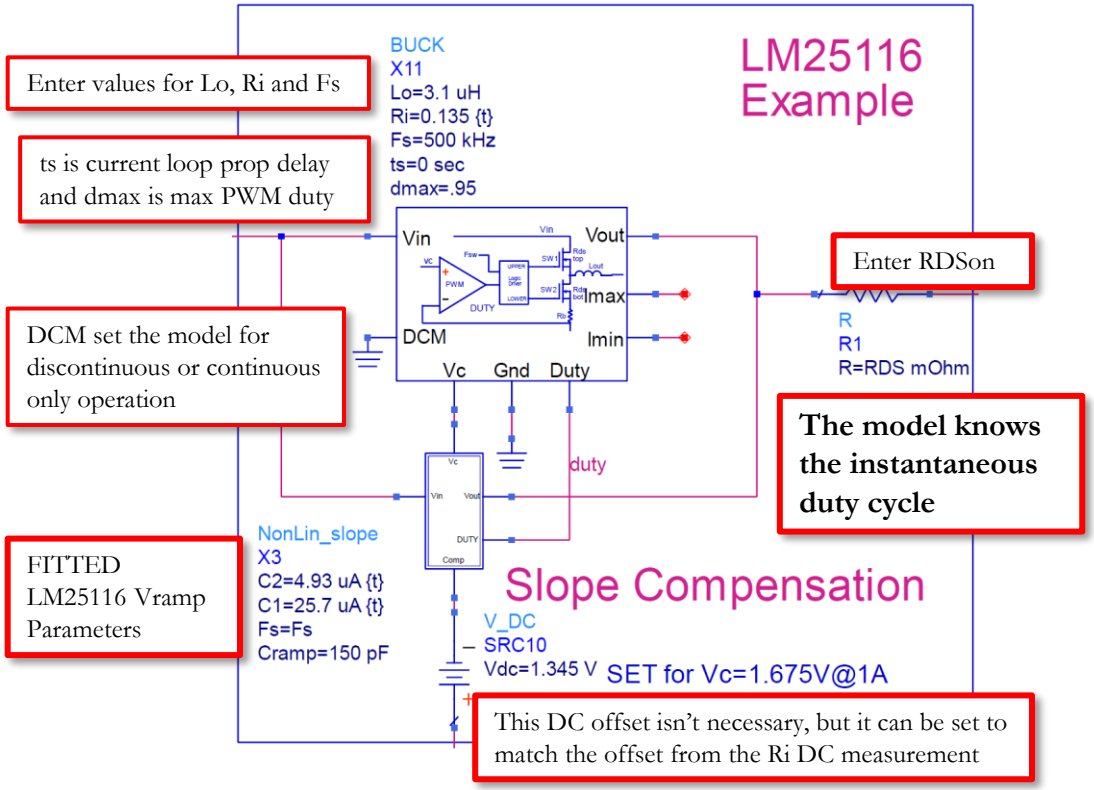


http://tinyurl.com/capacitor-video

YouTube Video: How to Design for Power Integrity: Measuring, Modeling, Simulating Capacitors and Inductors

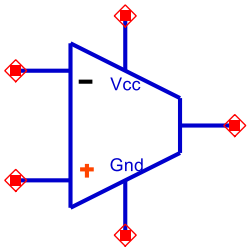
POPULATING THE MODEL

- The parameters are entered into the parameterized SPICE or ADS model
- The DCM pin is active pull up. This sets the operation to be diode/diode emulation or forced continuous conduction
- The “ts” parameter can be used for the current loop delay, but in most cases the default of 0 is ok
- The dmax defaults to 0.95 and this sets the maximum PWM duty cycle, generally listed in the datasheet



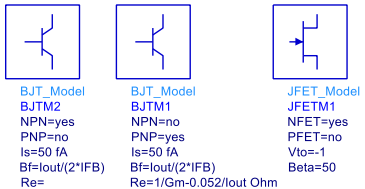
PARAMETERIZED TRANSCONDUCTANCE AMP

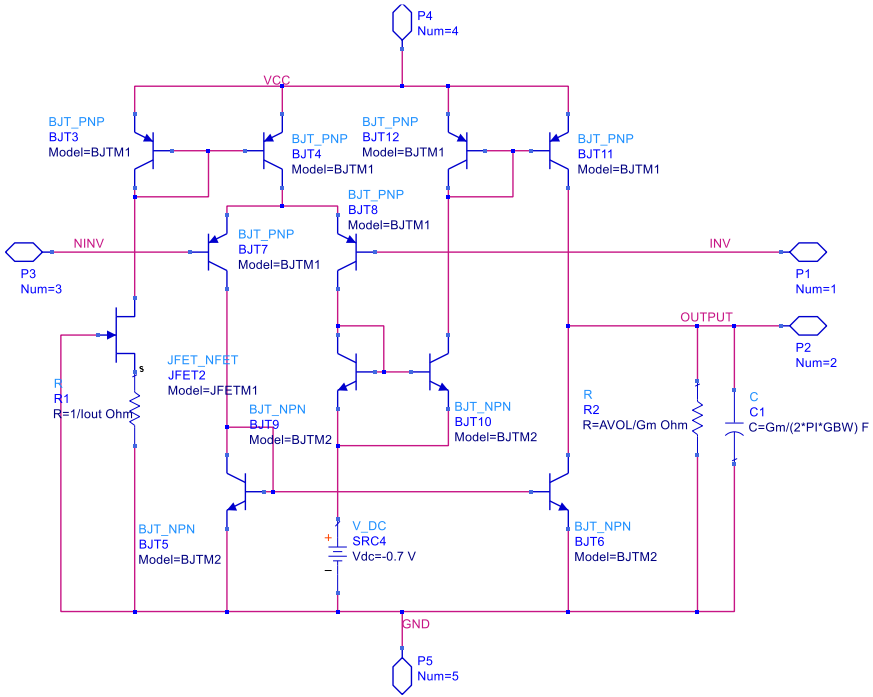
Select the appropriate, parameterized feedback amplifier – Transconductance type



The required parameters are generally available in the PWM datasheet

OTA
X1
Iout=1E-4 A
IFB=1E-4 A
AVOL=2000
Gm=510E-6
GBW=7.5E6 Hz

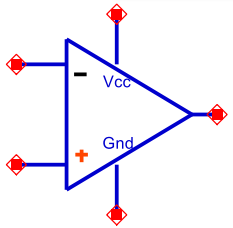




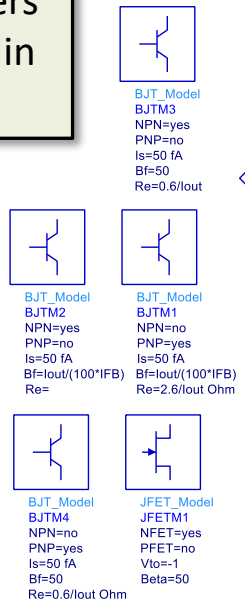
PARAMETERIZED VOLTAGE ERROR AMP

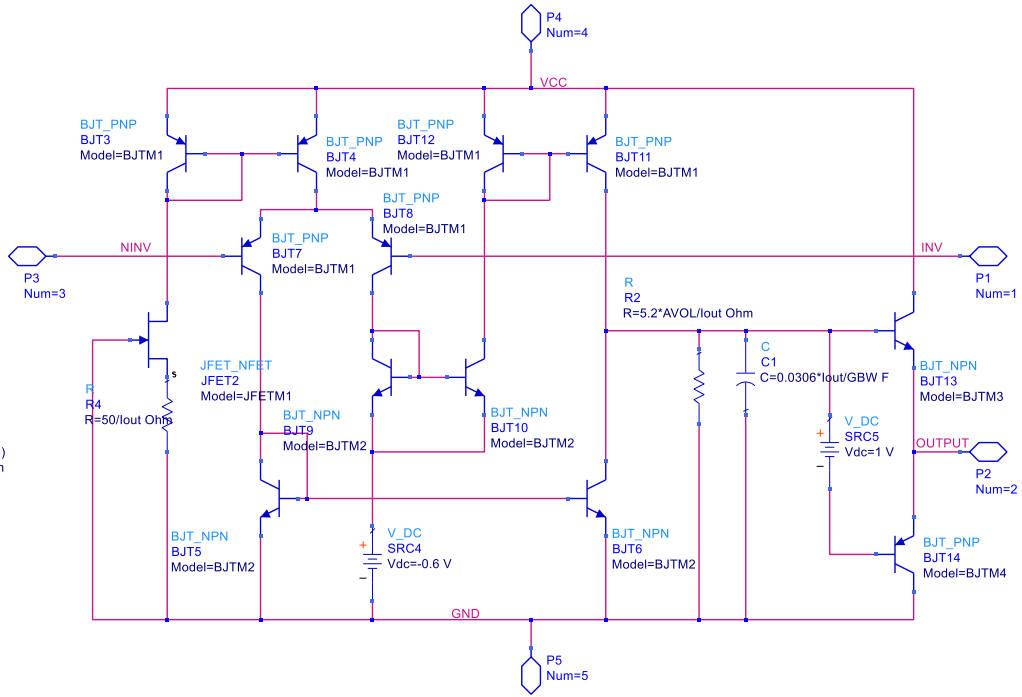
Select the appropriate, parameterized feedback amplifier – Buffered voltage type

The required parameters are generally available in the PWM datasheet



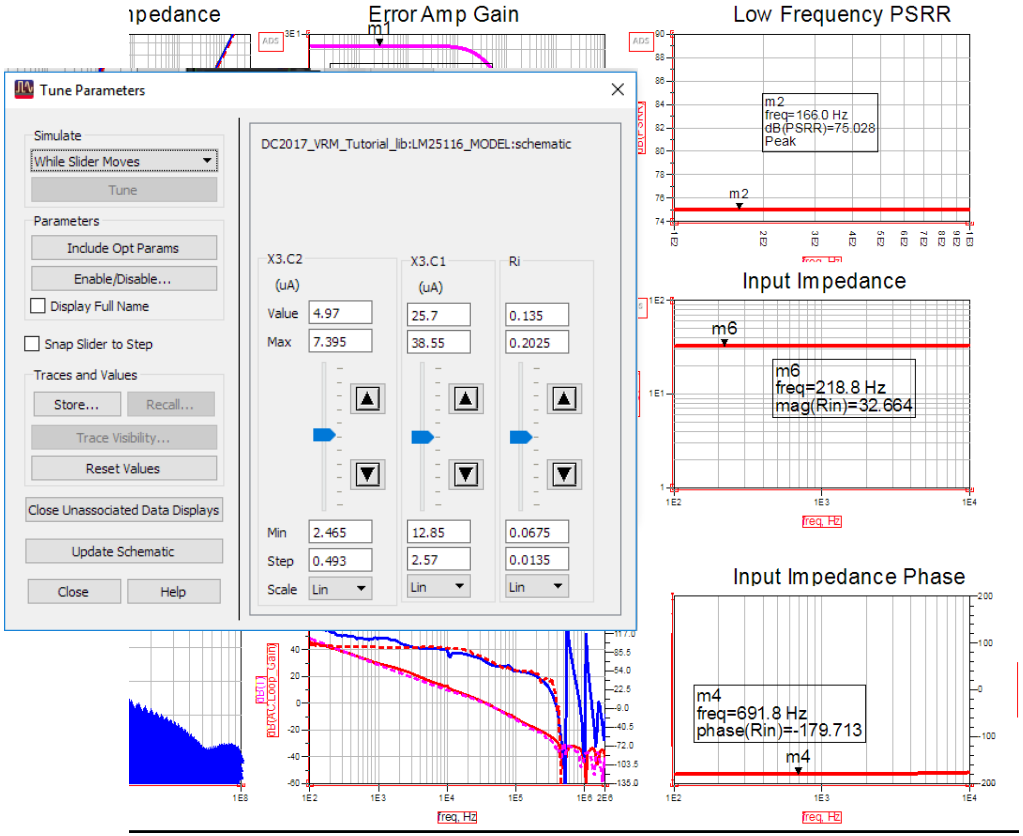
VOLTAGE_AMP
X2
Iout=3E-3 A
IFB=10E-9 A
AVOL=1E4
GBW=3E6 Hz





FINE TUNING THE MODEL

- The model should be quite good, just using our populated data
- You can fine tune the Vramp and Ri parameters to optimize the fit
- Note how well the Bode plot matches, though we didn't need it to create the model
- The ADS OPTIMIZER can be used to solve all the variables quickly and accurately

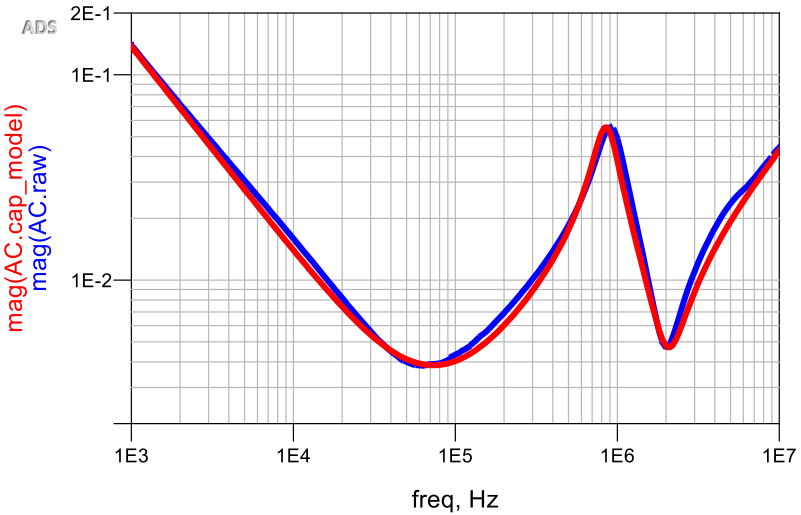


VRM ON AND OFF STATES

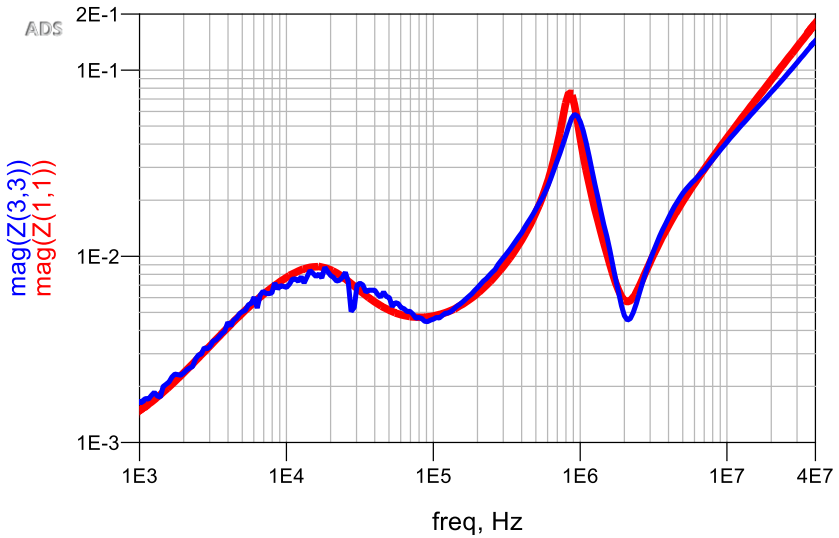
We like to measure in ON and OFF state

The two states confirms all parameters. It's important to get both conditions right.

VRM Turned Off

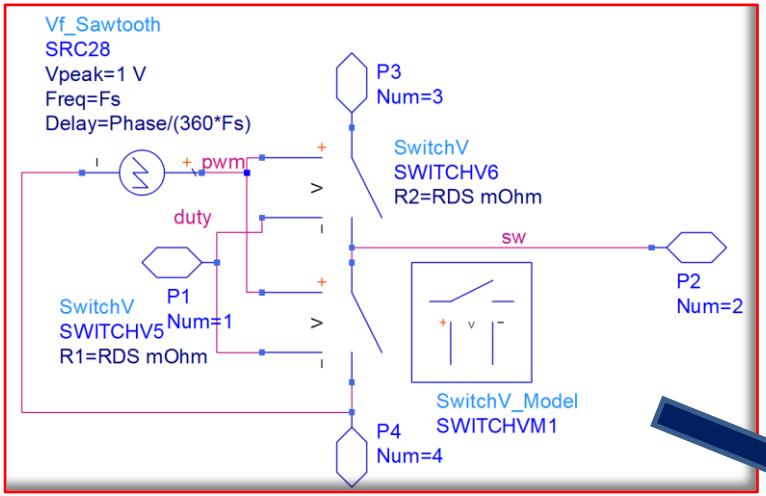


VRM Turned On

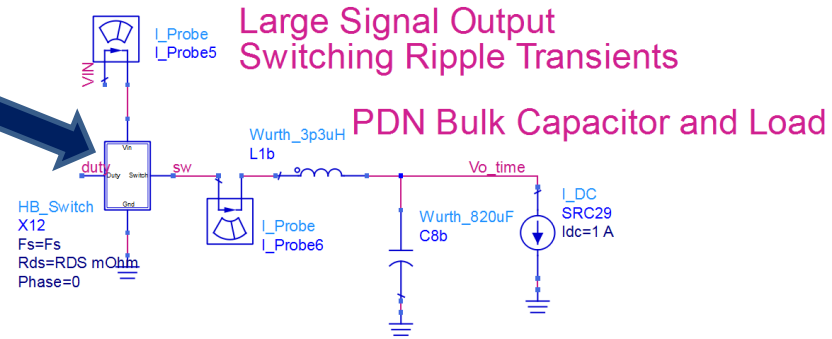


ADDING SWITCHING PARAMETERS

Pulse Width Modulated Switch

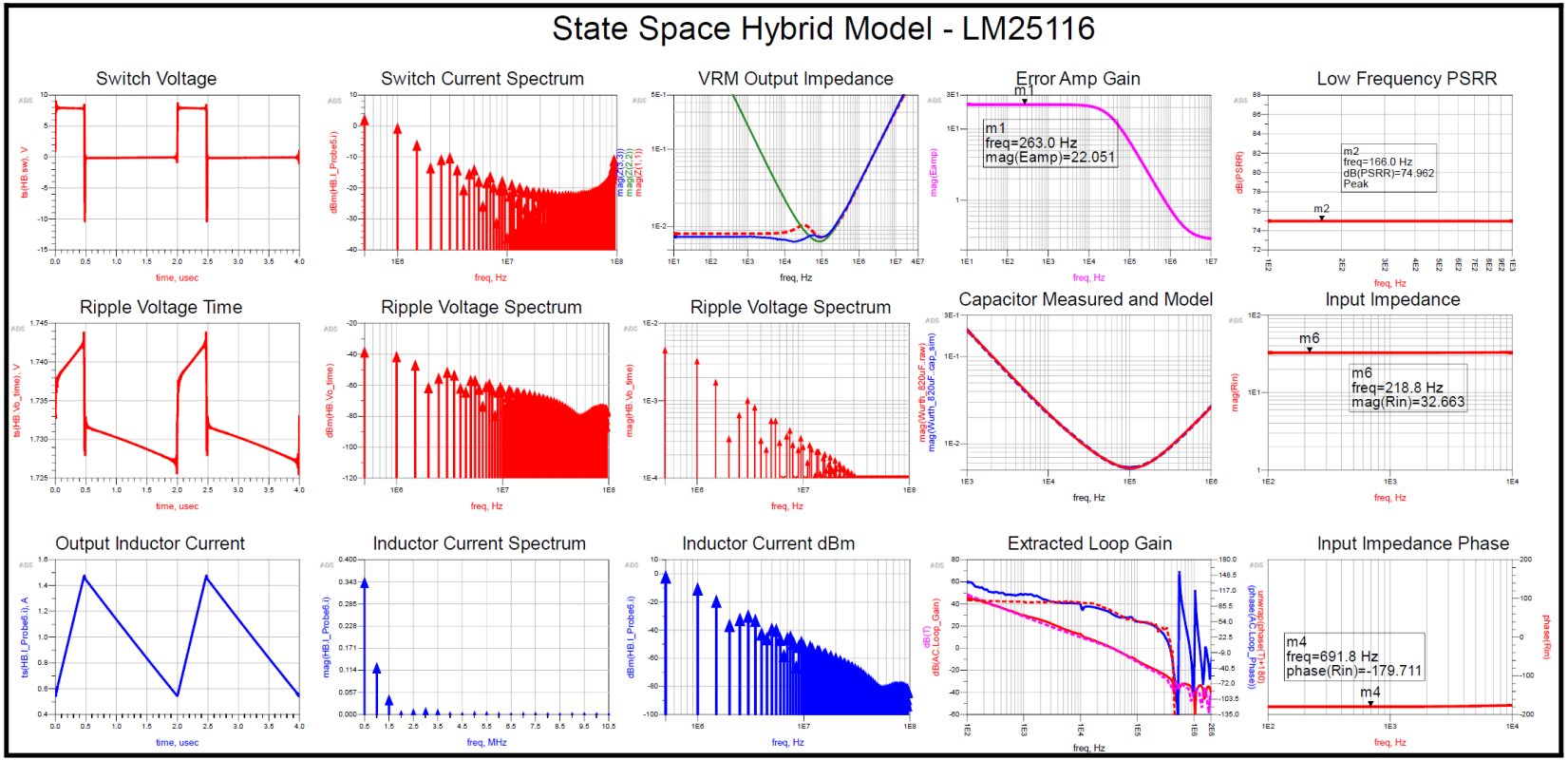


- Since the model *knows* the instantaneous duty cycle, we can replicate the output filter and create a pulse train at the switching frequency
- This half bridge model uses 1V sawtooth ramp and the switching frequency parameter to set the pulse train
- A phase delay allows multi-phase simulation using multiple half bridge models



Using SPICE, the time domain uses a transient simulator. ADS can use a much faster Harmonic Balance Simulation engine

FINAL PATHWAVE ADS PI SIMULATION

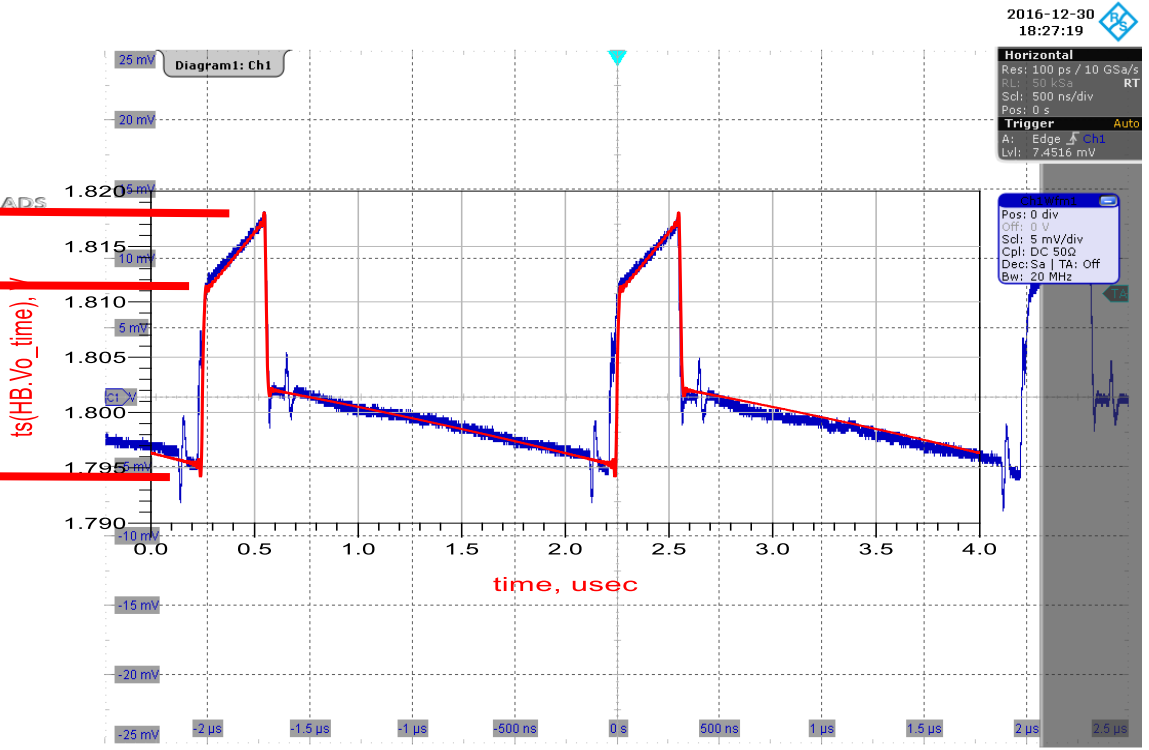


SIMULATED AND MEASURED VOLTAGE RIPPLE

The model very accurately matches the measurement results

$$\cong \Delta IL \cdot ESR$$

$$\cong \frac{Vin \cdot ESL}{Lo}$$

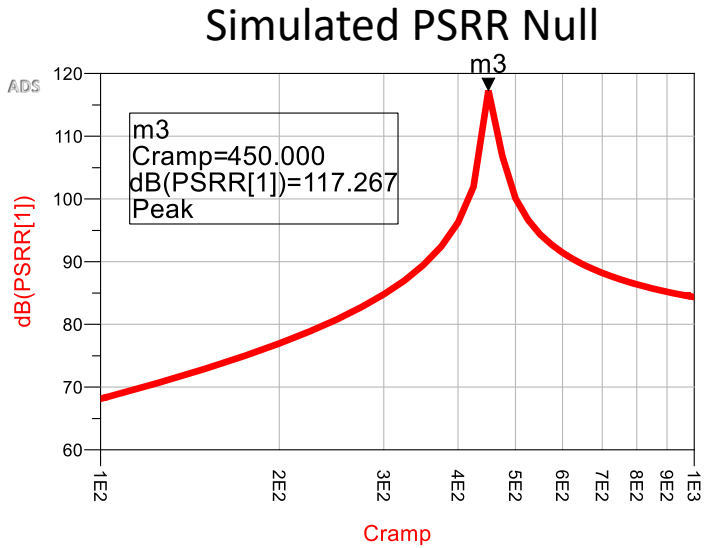


OPTIMIZING PERFORMANCE

- With the completed model, all parameters can be simulated, including negative input resistance, output impedance, PSRR, transient response, ripple voltage, switch voltage, etc
- If using an EM simulation, the printed circuit board effects can also be included
- The model can also be used to optimize performance of any, and all parameters

PARAMETER SWEEP

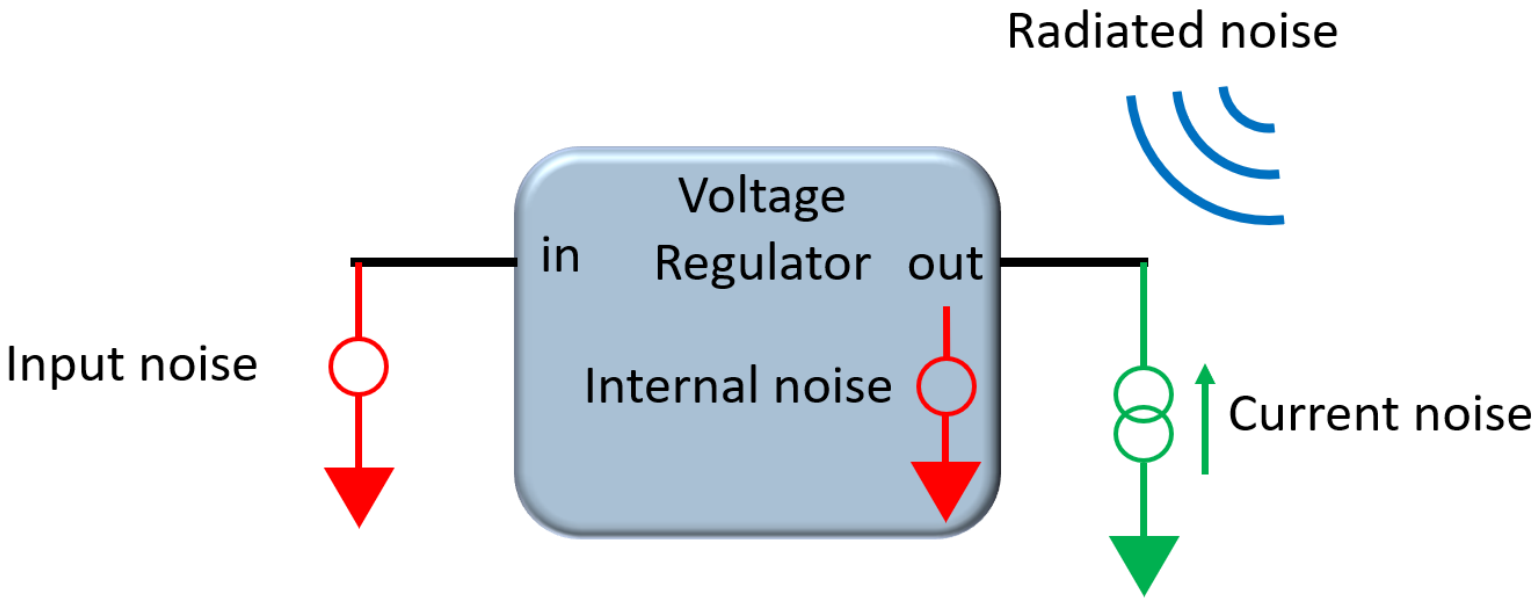
```
ParamSweep
Sweep1
SweepVar="Cramp"
SimInstanceName[1]="AC1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=100
Stop=1000
Step=25
```



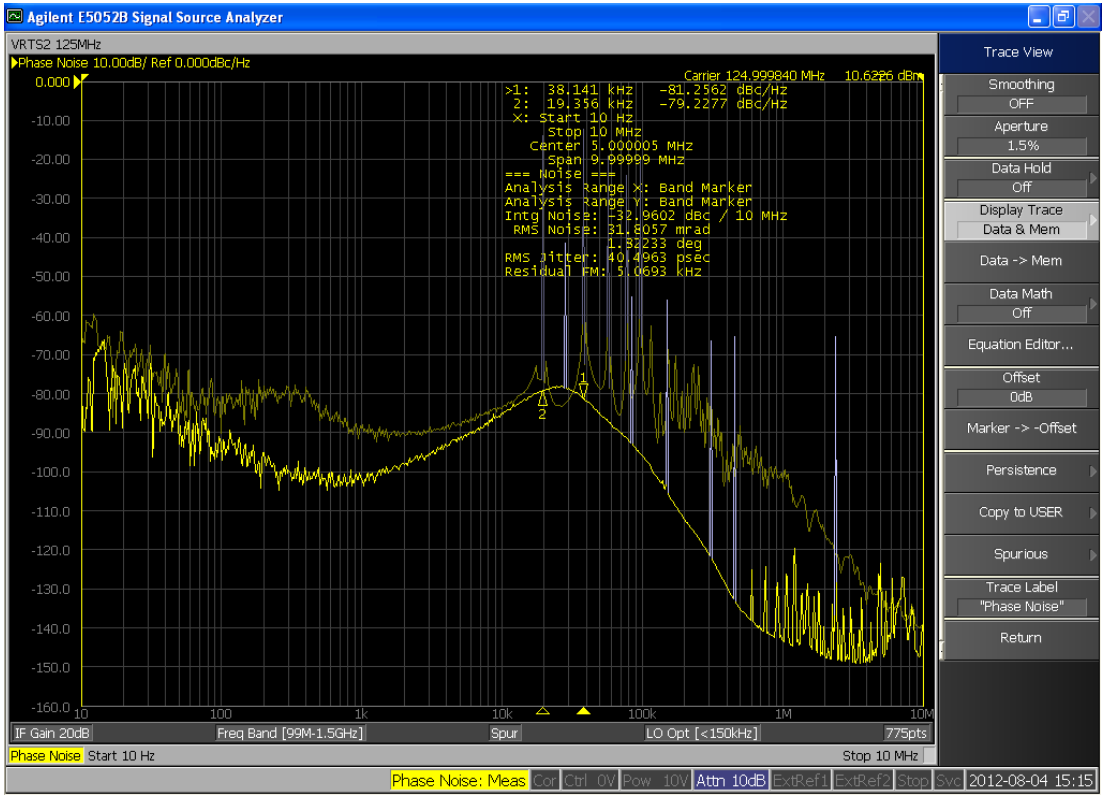
PSRR of the Current Mode converter includes a null
PSRR can easily be optimized if the ramp is adjustable

NOTE THIS IS SECOND ORDER, SO PAY ATTENTION TO PHASE

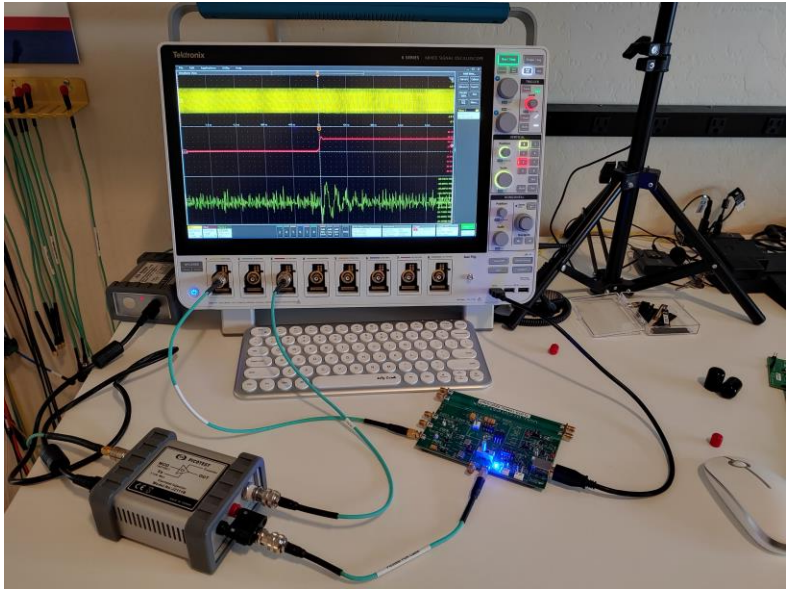
The VRM is a Noise Source AND a Noise Hub

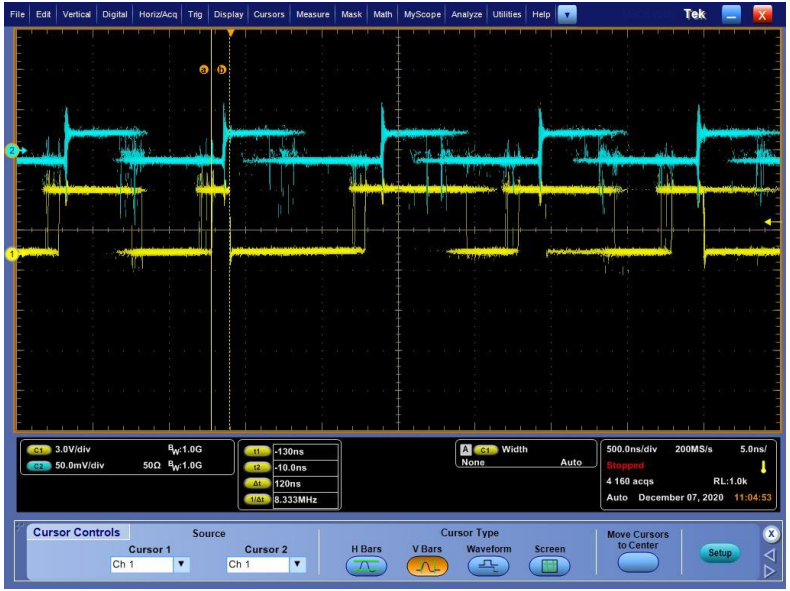


Pay Attention to the System Level Noise

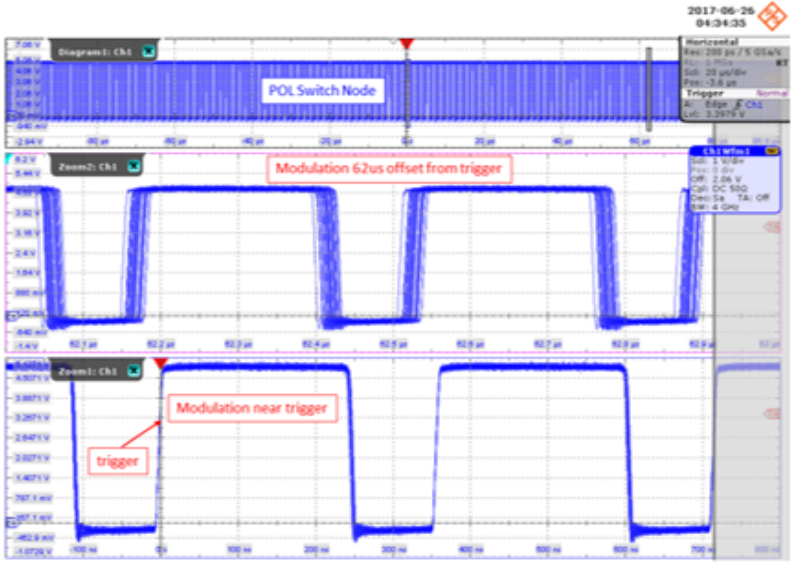


Can’t Assess PI in Isolation



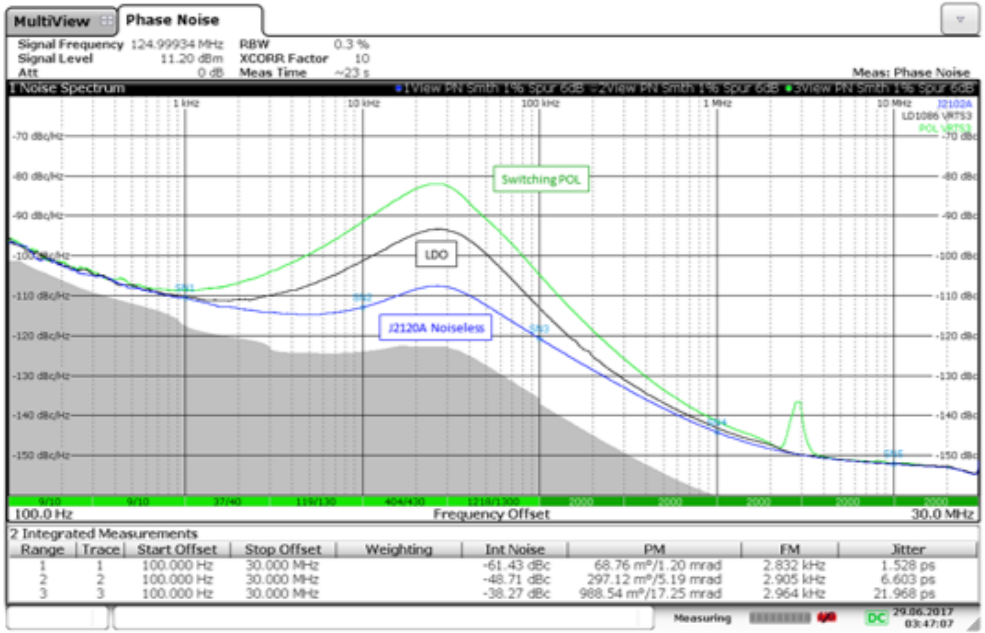


And Unintentional Spread Spectrum



Many switching power supplies use less than stellar oscillator circuits, resulting in switching frequency jitter

The switching frequency jitter results in power supply noise, which in-turn results in oscillator jitter - **Jitter-Induced Jitter**



Remember

- Vendor models are hard to obtain and rarely valid for your design, so be sure to measure what you buy and create a measured model.
- VRM State Space Average behavioral models can predict small signal and large signal behavior and run fast in Harmonic Balance for transient results.
- Measuring VRM on/off impedance vs. frequency is a simple yet powerful measurement for tuning simulation models to correlate with measurement.

AGENDA

Power Integrity Basics – VRM + PDN + Digital Load
presented by Heidi Barnes

Measurement Based VRM Modeling
presented by Steve Sandler

Building a Power Delivery Digital Twin - TI TPS7H4003 SSAM Case Study
presented by Benjamin Dannan

APEC

S12: How Power Integrity is Changing the World of Power Electronics

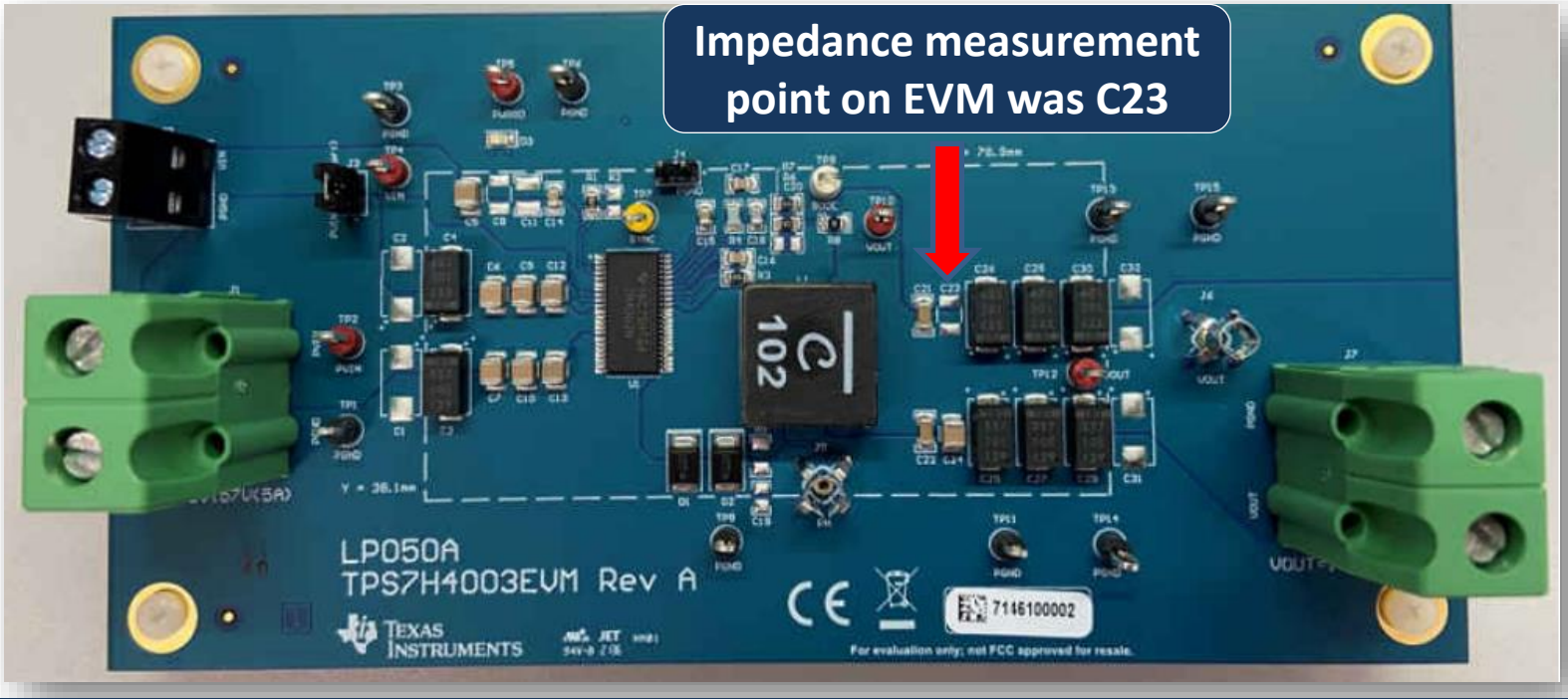
Building a Power Delivery Digital Twin - TI TPS7H4003 SSAM Case Study

Speaker:

Benjamin Dannan

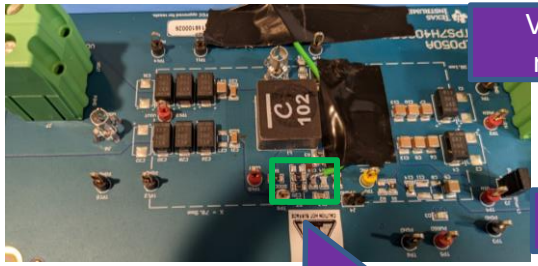
"Now, let's show the process on an actual VRM of how to populate the SSAM model"

Measurement Platform – TI TPS7H4003 Evaluation Module



TPS7H4003 is a radiation tolerant VRM for LEO and GEO applications

Measure Ri Directly on TPS7H4003 VRM

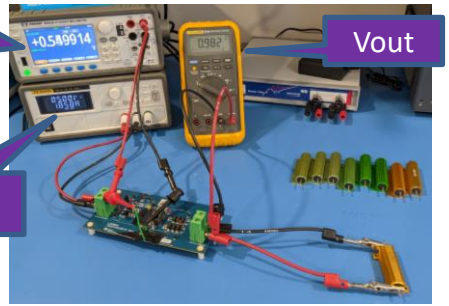


Vcomp result

VRM Vin

Solder wire on VRM Vcomp pin

Measurement Setup

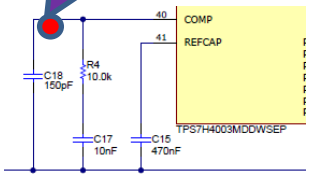


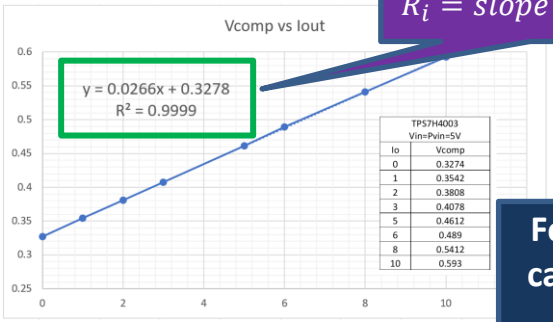
Vout

Io	Vcomp
0	0.3274
1	0.3542
2	0.3808
3	0.4078
5	0.4612
6	0.489
8	0.5412
10	0.593

Plot Vcomp vs. Iout results to determine R_i

Solder point @ C18





$R_i = slope = 26.6\ m\Omega$

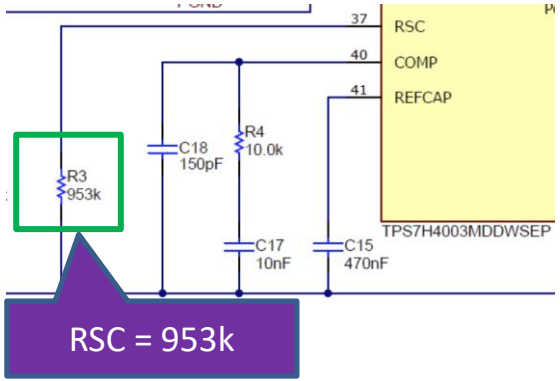
For Ri we only care about the slope!

This measurement requires a VRM with external Vcomp access

The measured result doesn't always agree with the datasheet

Estimating TPS7H4003 V_{RAMP}

From TPS7H4003 EVAL Schematic



RSC = 953k

From TPS7H4003 Datasheet

COMP to Iswitch gm[3]	COMP = 0.5 V	–55℃	28	38	49	S
		25℃	29	40	50	
		125℃	30	41	52	

$R_i = 1/40 = \mathbf{25\ m\Omega}$

Per TPS7H4003 Datasheet

$$RSC = \frac{24000}{f_{SW}} + \frac{1040}{SC} - 30$$

Solve for Slope Comp (SC)

TPS7H4003 f_{sw} = 500 kHz → SW_period = 2us period

$$SC = 1.1A/us \quad (1)$$

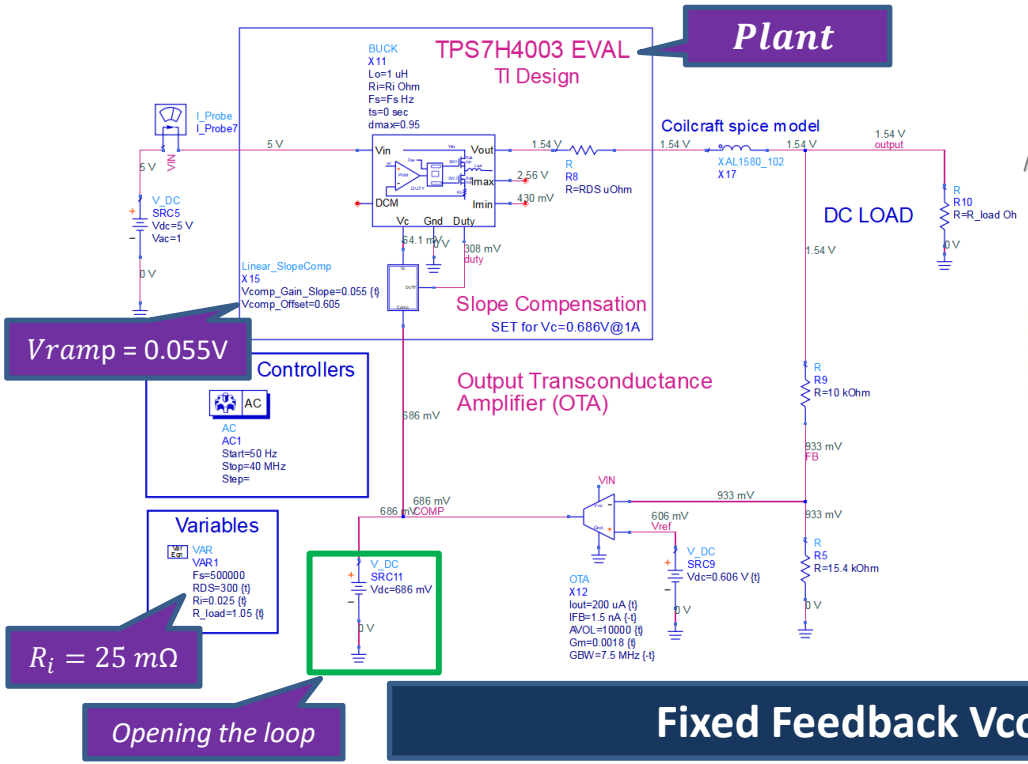
$$SC_{per\ duty\ cycle} = SC \cdot SW_{period} = 1.1A/us \cdot 2us = 2.2A/100\%\ duty\ cycle \quad (2)$$

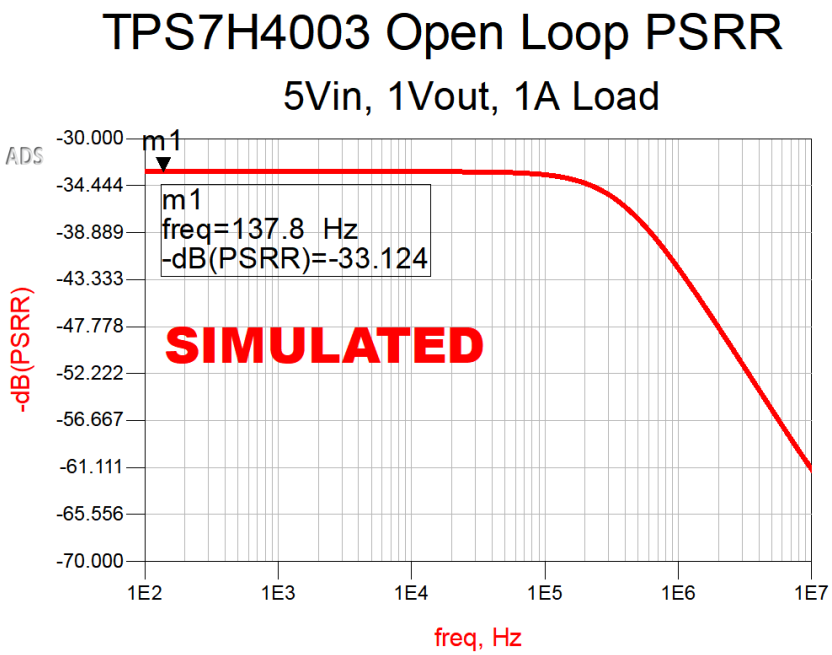
$$V_{RAMP} = SC \cdot R_i = 2.2A \cdot 0.025\Omega = 0.055V \quad (3)$$

VRM vendors do not always make this information available to populate the model

Simulating the Open Loop Plant Gain

Showing Plant Open Loop Gain using datasheet Vramp and Ri Values

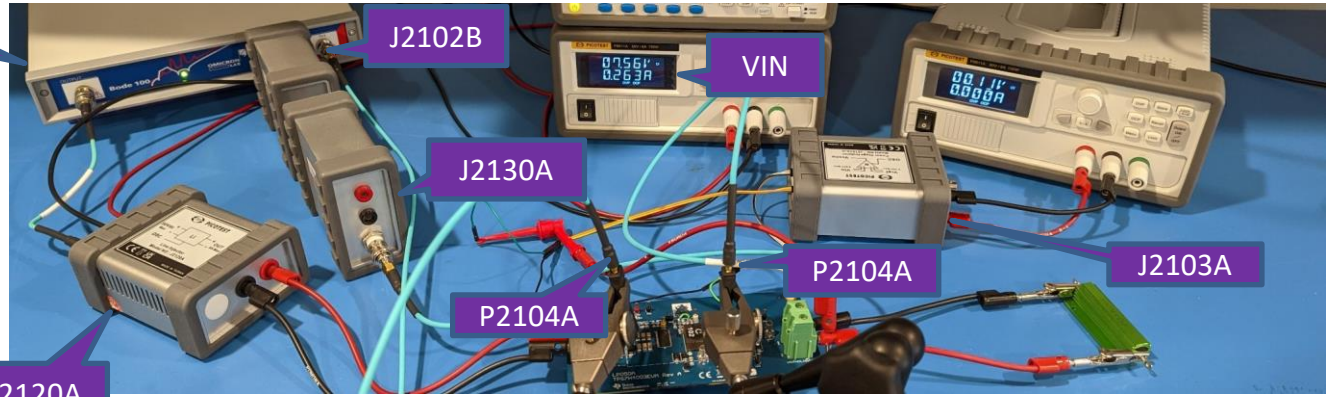




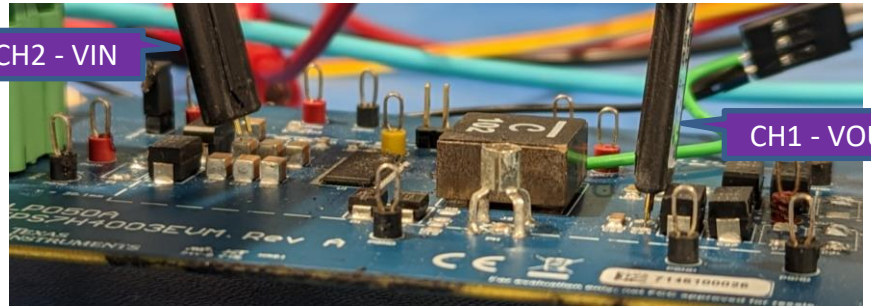
Fixed Feedback Vcomp for a given load

PSRR Setup with the TPS7H4003

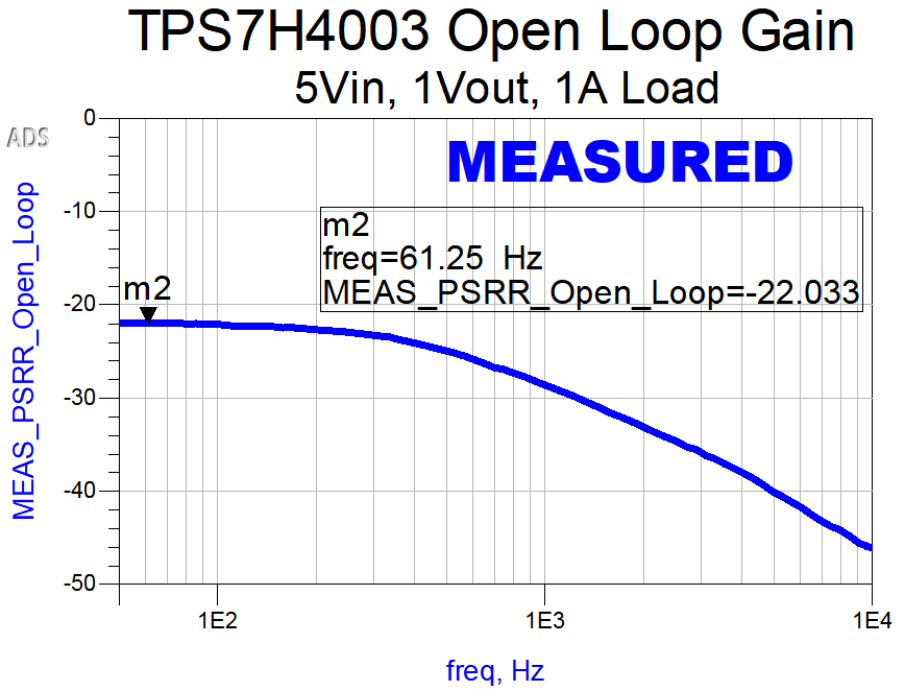
Let’s measure the open loop plant gain and closed loop PSRR

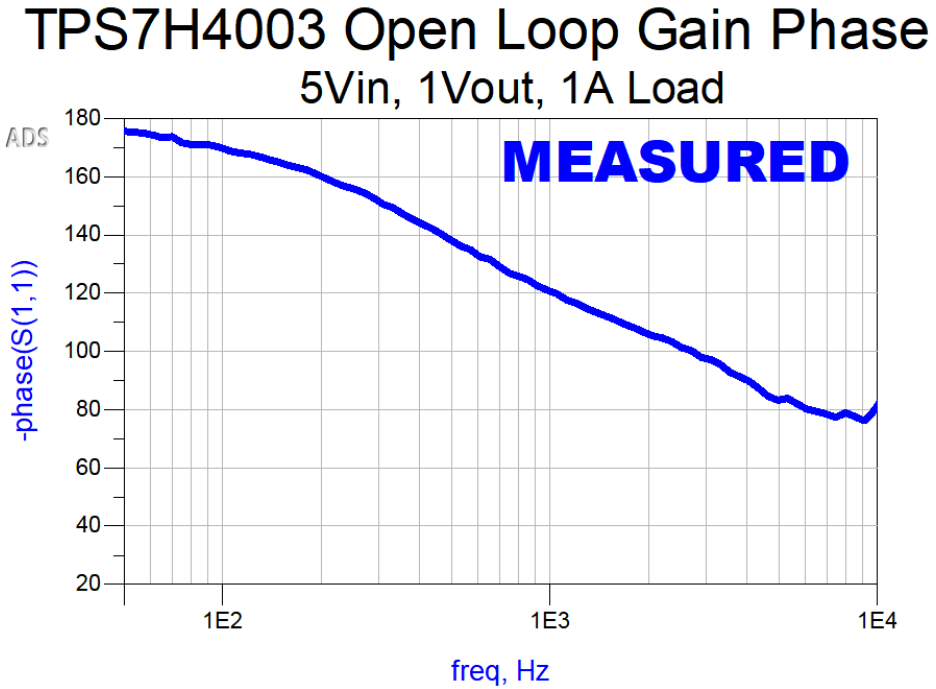


Now, let’s measure this!

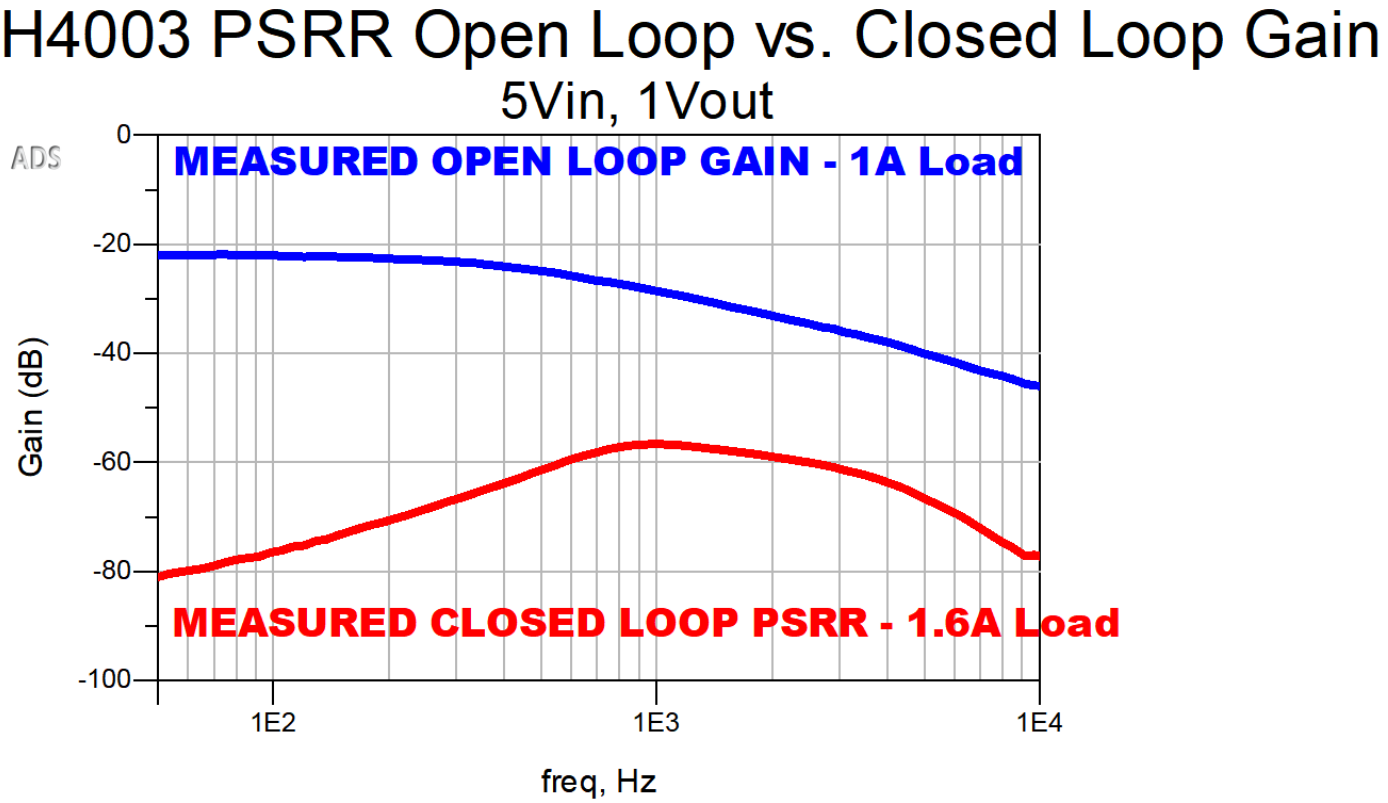


Open Loop PSRR – TPS7H4003 Gain Magnitude and Phase

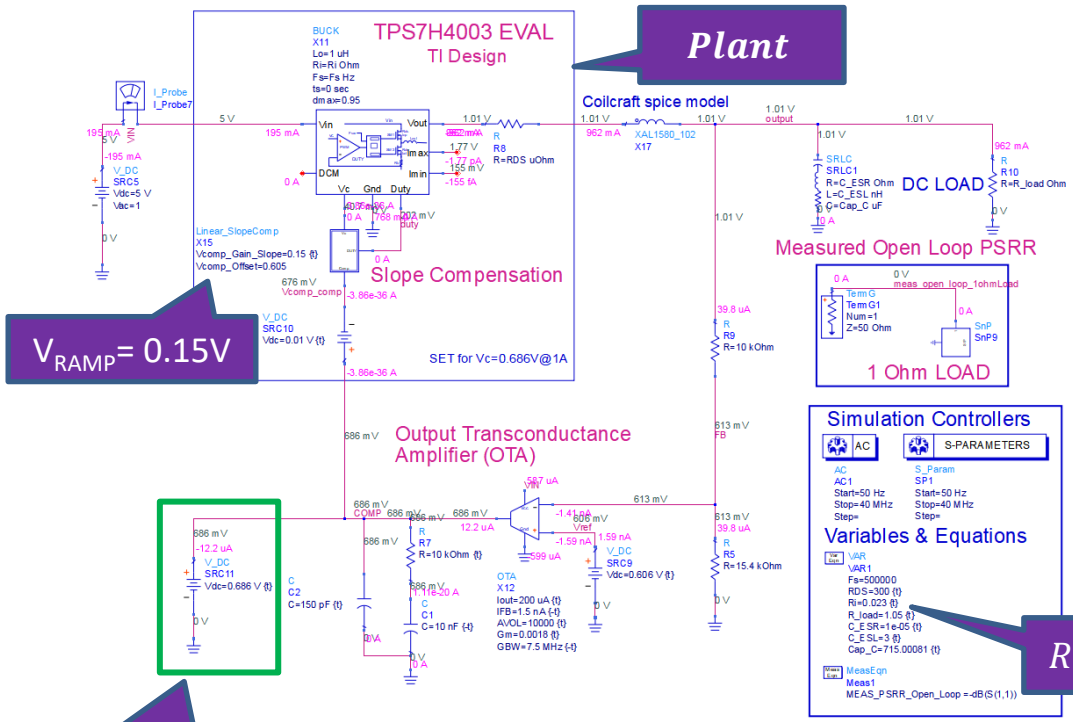


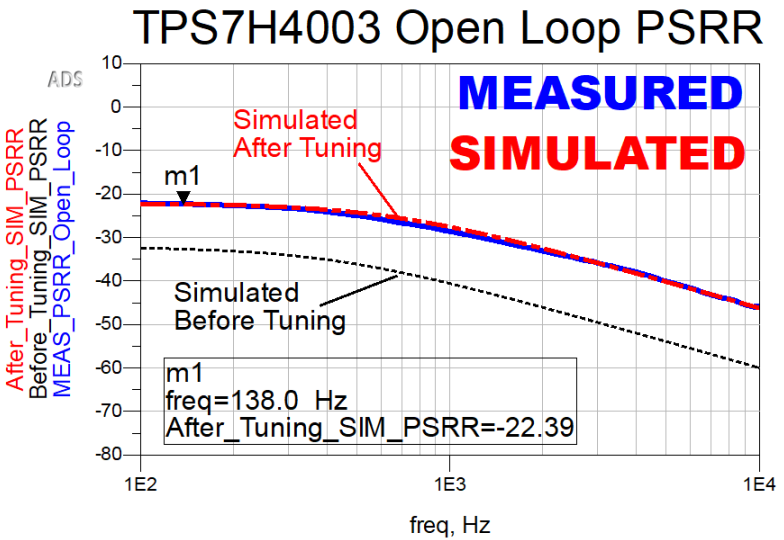


Measuring PSRR TPS7H4003 Open and Closed Loop



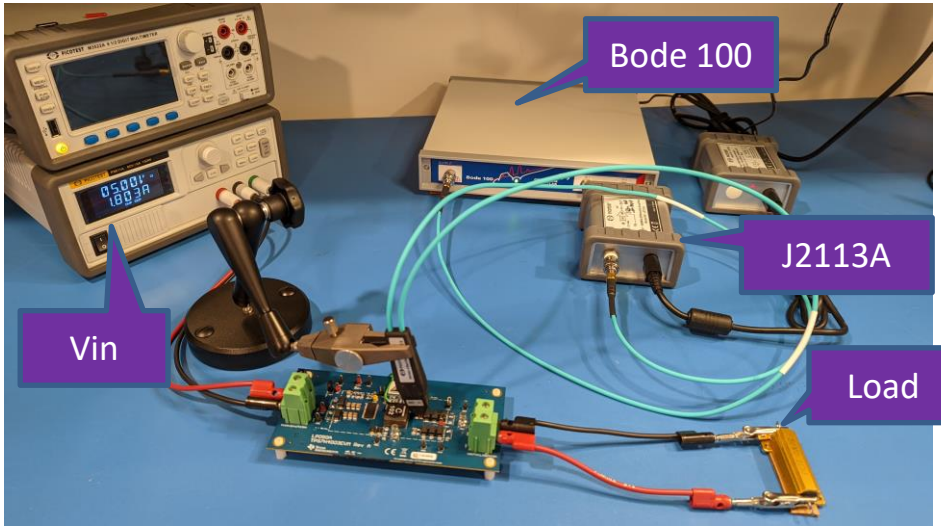
PSRR changes with load, so measure Open Loop

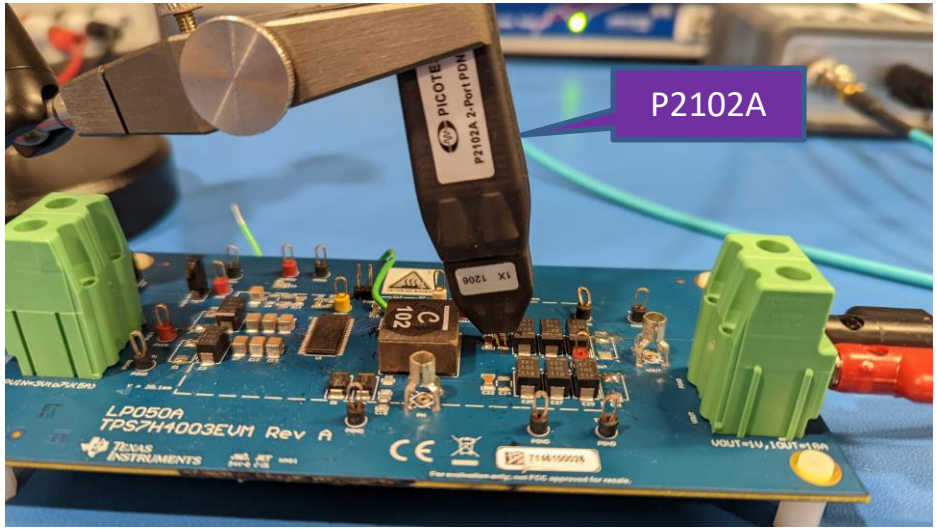




After tuning to match measurement, V_{RAMP} = 0.15V

Measuring VRM Output Impedance





Measure the VRM ON and OFF impedances

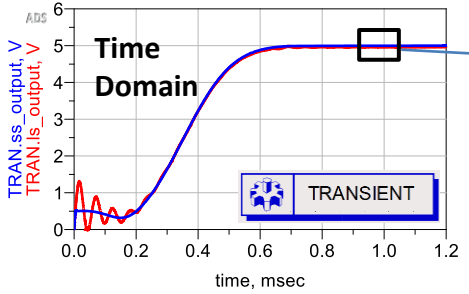
When doing a 2-port impedance measurement, it is important to remove the capacitor to prevent AC coupling between the 2 ports on the probe, which can cause measurement error

Why use the Harmonic Balance Simulator with SSAM

- Fourier Theory says time domain waveforms are made up of frequency domain waveforms.
- Solving a circuit in the Frequency Domain can be much faster since it limits the frequencies and jumps to steady state.

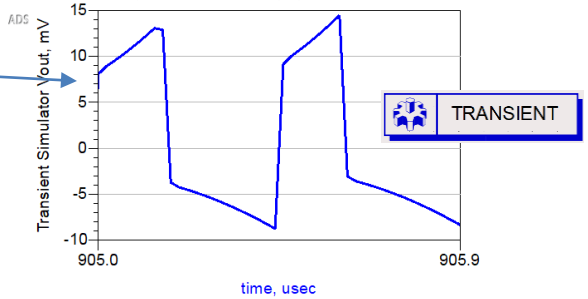
Transient must reach steady state to measure ripple.
50,000 time-steps!

Simulator Results

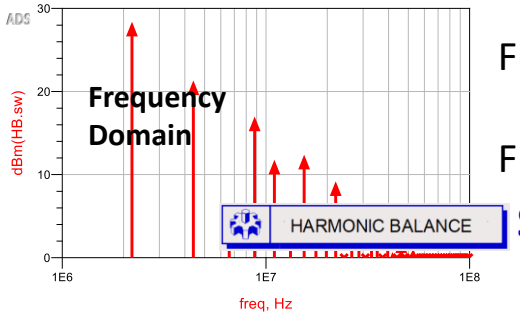


Time Domain
Transient Sim
Wait for Steady State
Minutes, Hours, **Days**

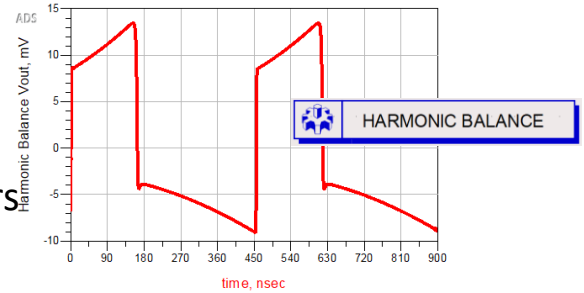
Steady State Ripple vs. Time



Harmonic Balance simulates harmonics of the switching frequency.
Only 255 Frequencies for steady state ripple!



Frequency Domain
Harmonic Balance Sim
FFT jumps to Steady State
Seconds, Minutes, Hours

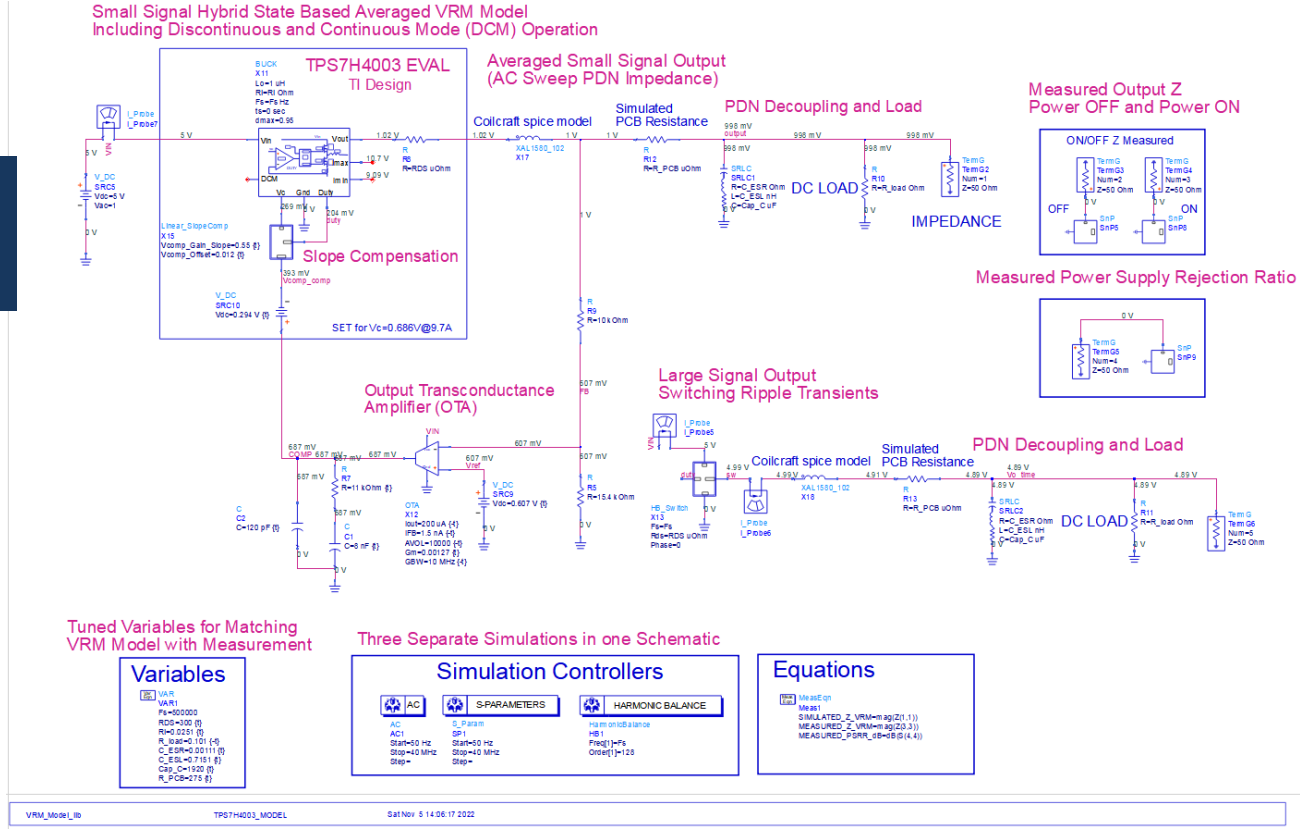


Data shown is for one VRM, typical PCB design has dozens of VRMs

State-Space Average Model TPS7H4003 EVM – TI Design

Does not include PCB effects

Put it all together in the Sandler SSAM VRM Model

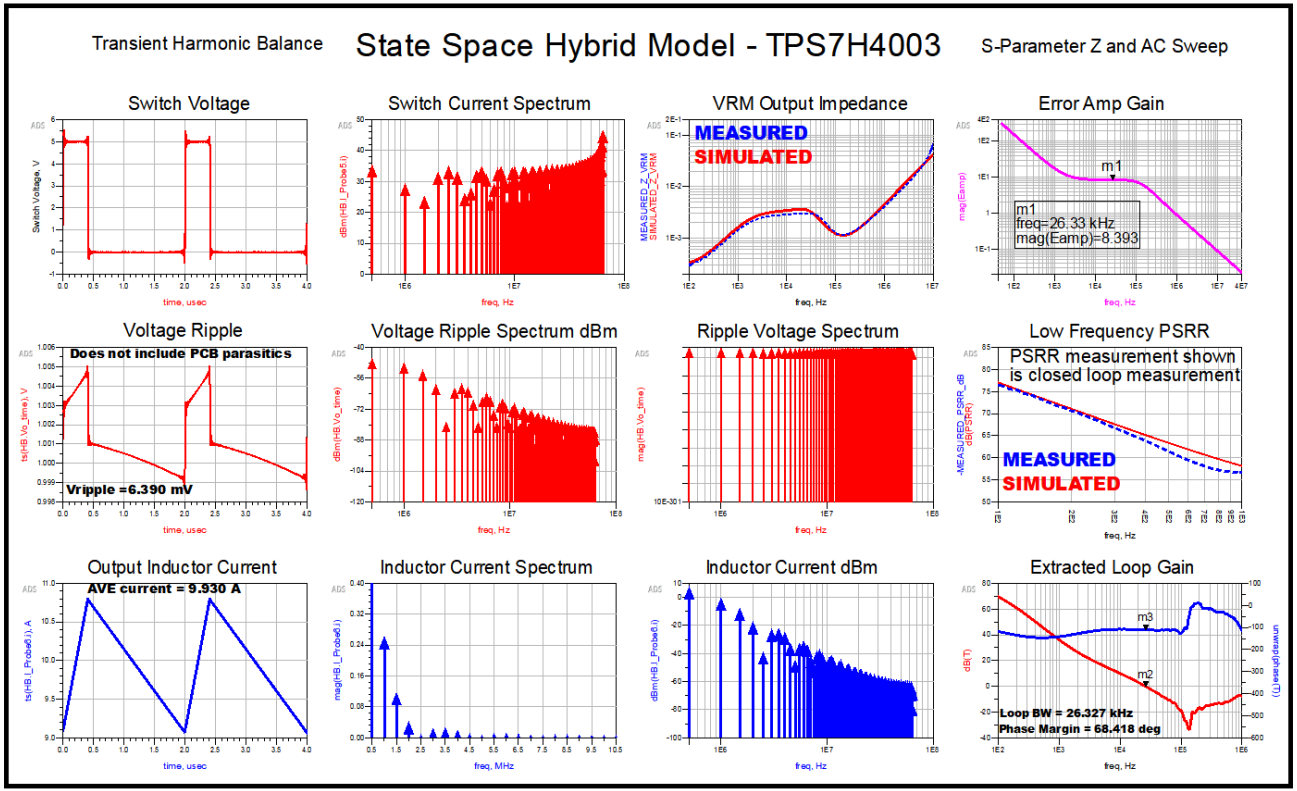


TPS7H4003 State-Space Average Model Results

Does not include PCB effects

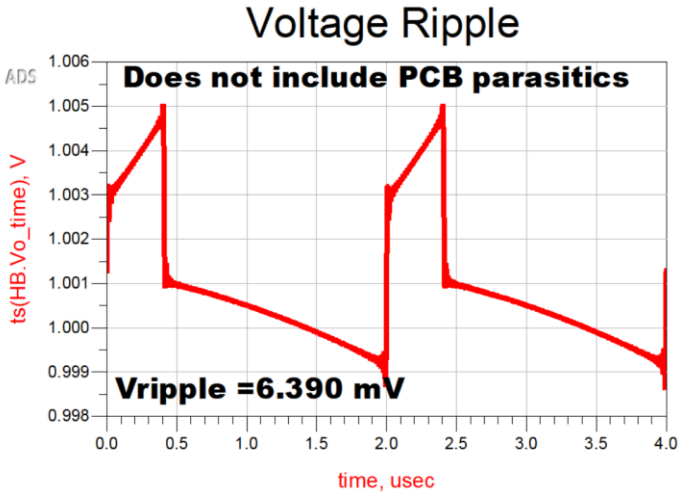
Simulation matches measurement…
Model is good!

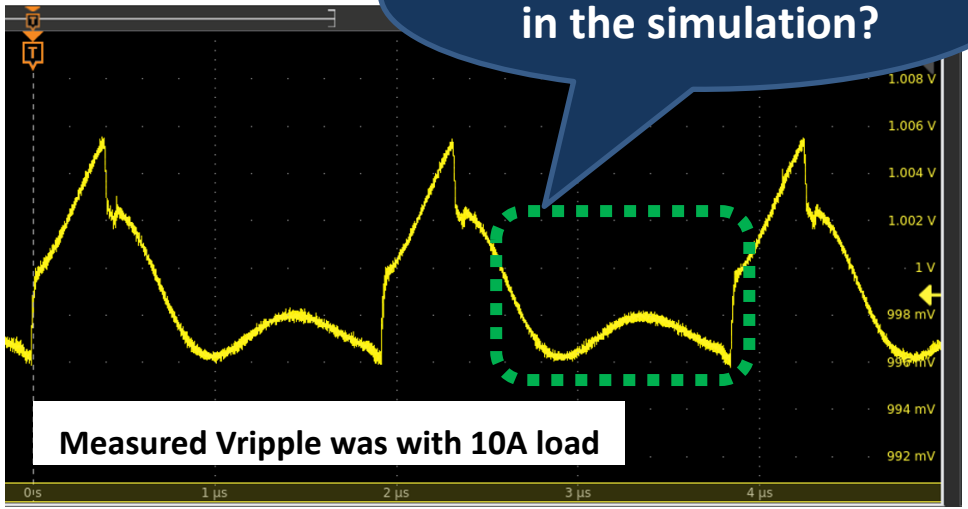
We're finished!
Or are we?



TPS7H4003 VRM Output Voltage Ripple

Simulation vs. Measurement





Comparing the simulated voltage ripple to the measurement

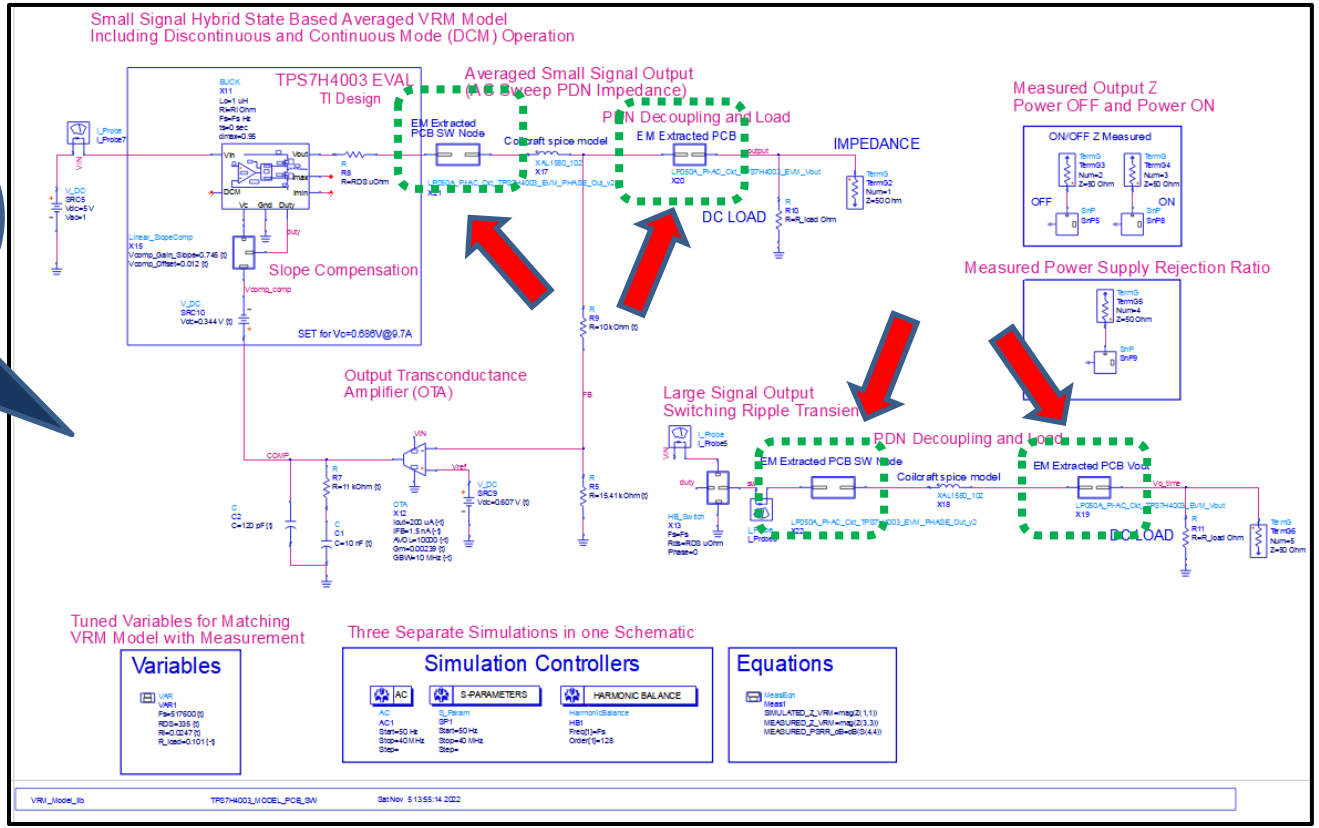
Simulated Vripple with 9.8A load

Measurement point

State-Space Average VRM Model TPS7H4003 EVM – TI Design

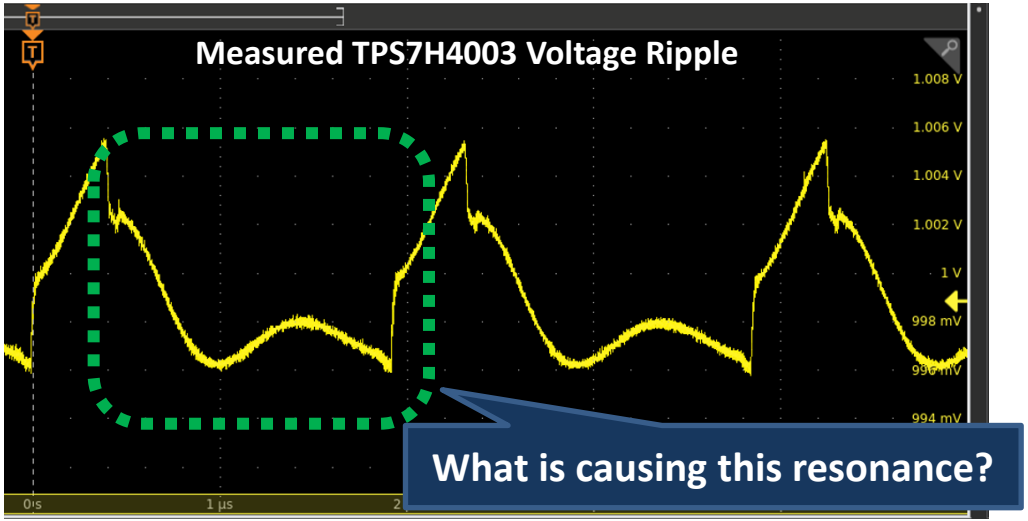
Does include PCB effects

Let's add the PCB effects to our model and see what happens to the voltage ripple

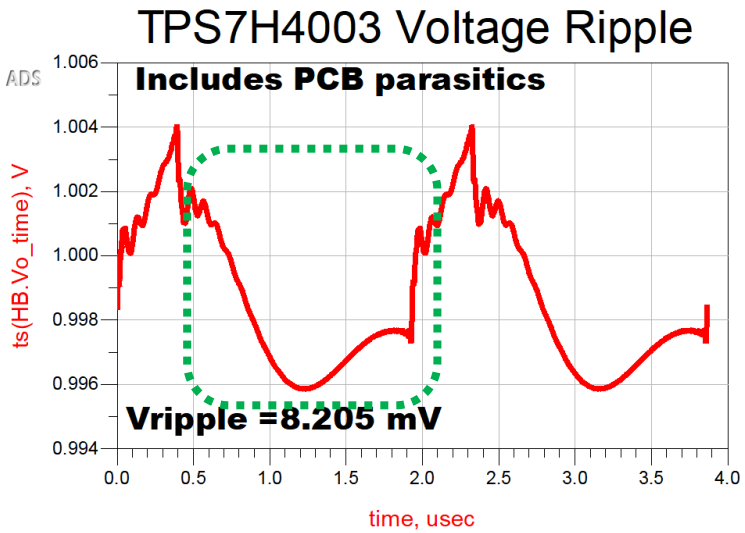


TPS7H4003 VRM Output Voltage Ripple

Measurement vs. Simulation with included PCB effects

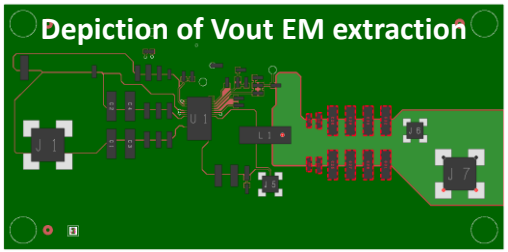


Simulated TPS7H4003 Voltage Ripple using State-Space Average VRM Model



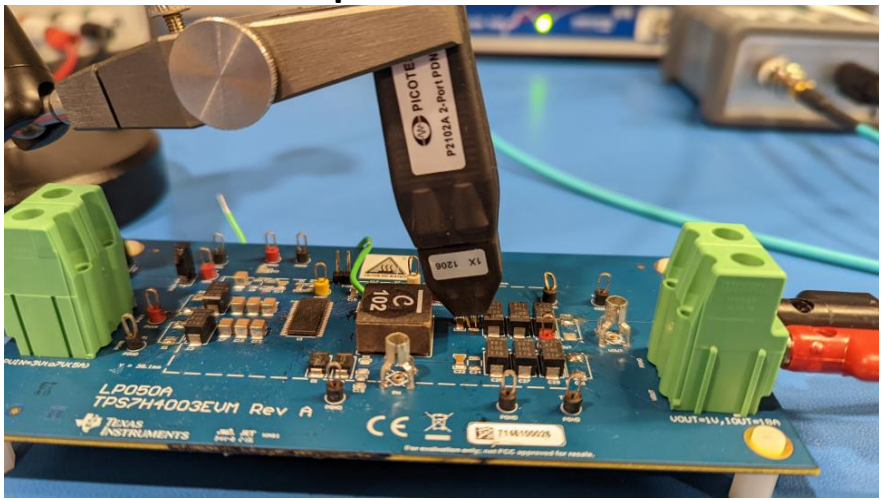
All extracted PCB artwork was from Keysight PathWave PIPro

Extracted PCB Artwork, the extracted Switch node is not depicted

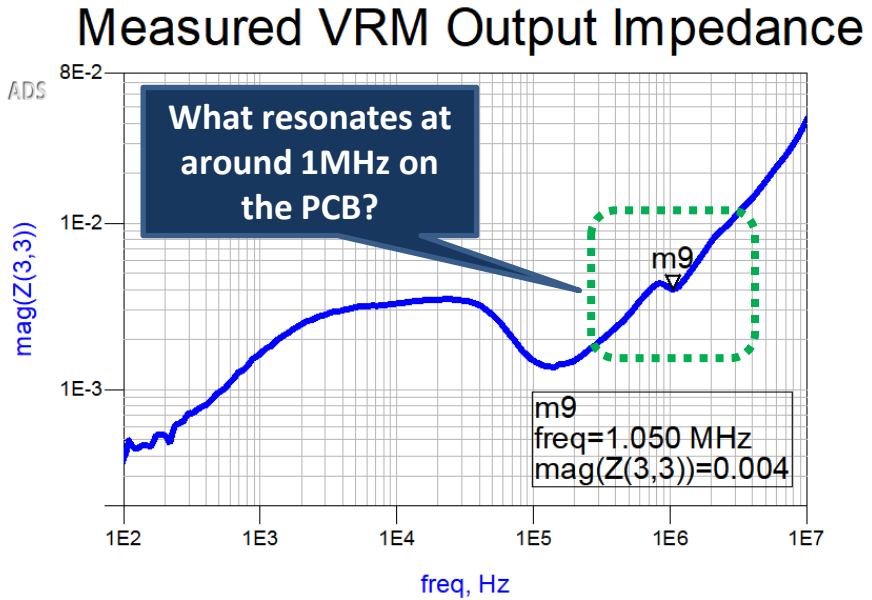


Exploring the PCB Effects seen in the Output Ripple

Output Impedance Measurement Setup with 2-port PDN Probe



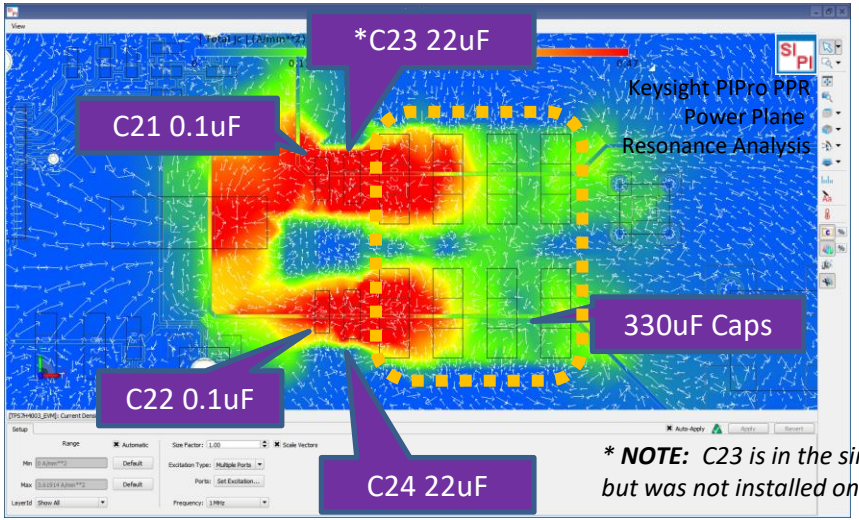
Measurement Point at C23



Output impedance measurement shows 1MHz resonance

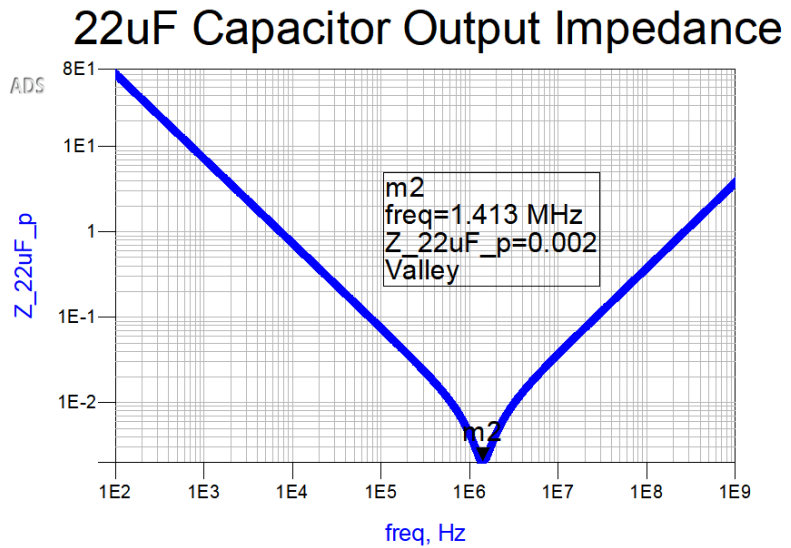
TPS7H4003 VRM – Investigating the Current Density on the PCB

Current Density Plot is created with 1MHz Resonance Frequency



** **NOTE:** C23 is in the simulation, but was not installed on the PCB*

22 uF Cap resonances at 1 MHz!



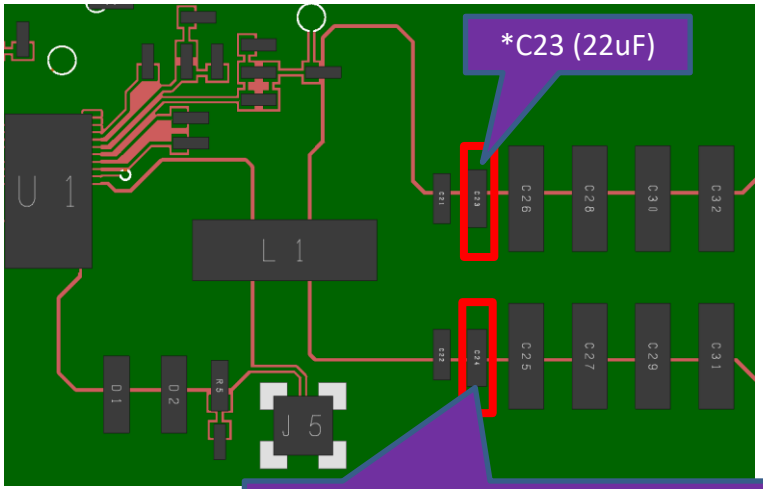
Multiple Caps are resonating at 1MHz, but only one is the culprit

Further Analysis 22uF vendor spice model confirms C24 is the potential resonance point on the PCB…..

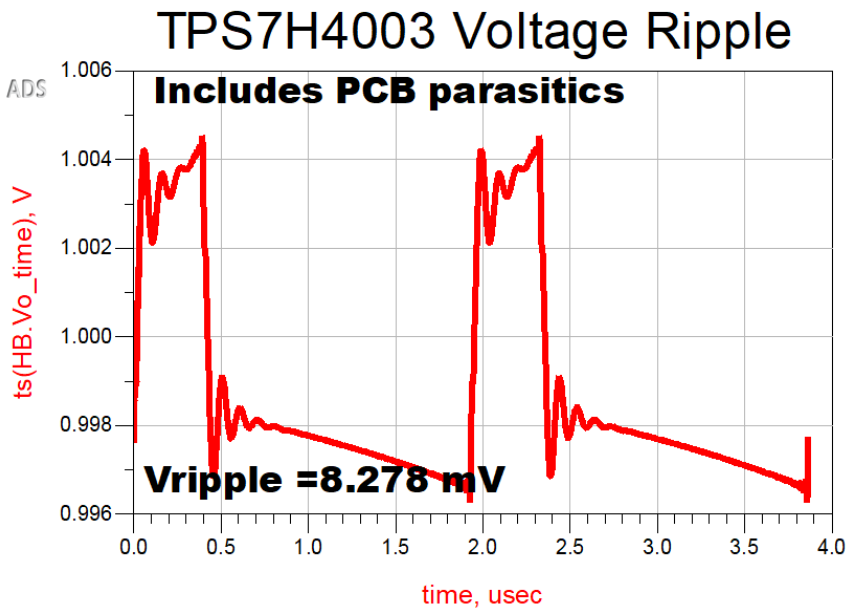
The 22uF Cap (C24) looks be our problem, right?

TPS7H4003 VRM – Removing the 22uF Capacitor

What happens if we remove the 22uF cap (C24)?



Simulated Vripple with 9.8A load



Removing a single capacitor removed the resonance seen in the output voltage ripple!

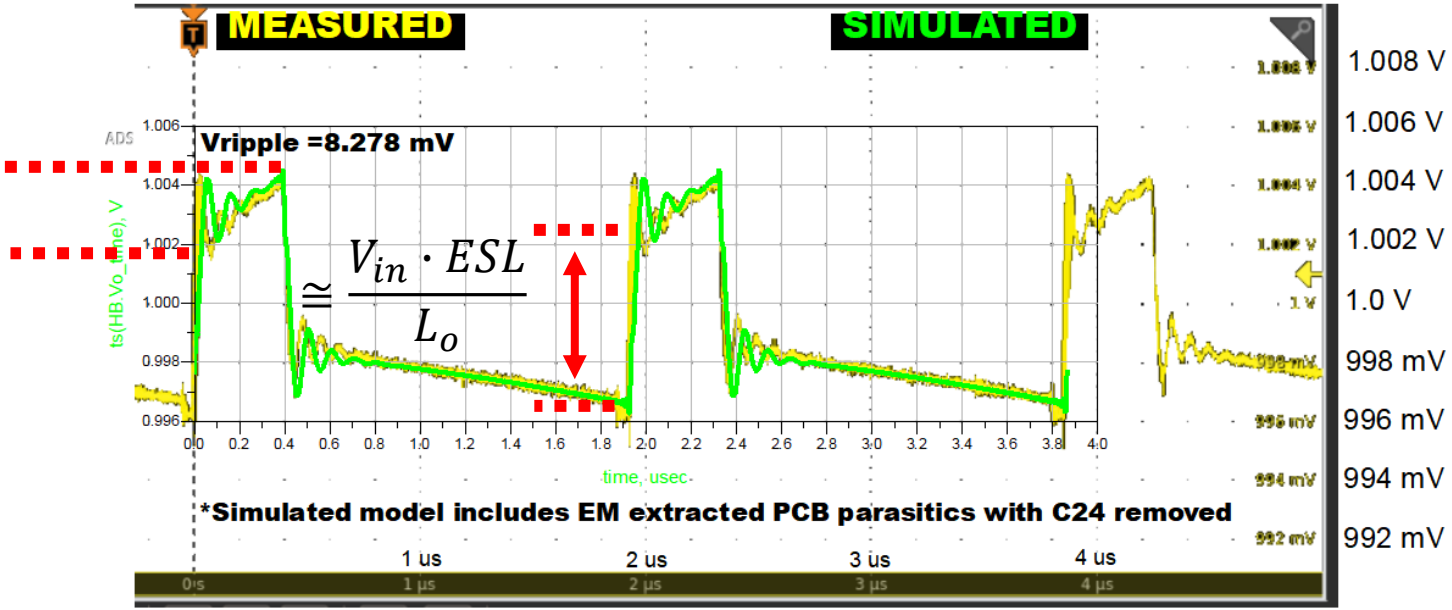
Simulating with PCB effects matters for getting the answer right!

Fine Tuning the TPS7H4003 EVM SSAM VRM Model – Digital Twin

Voltage Ripple - TPS7H4003 VRM EVAL PCB

Measurement vs. Simulated State Space Average Model

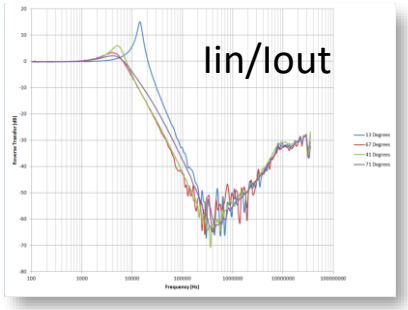
$$\cong \Delta I_L \cdot ESR$$



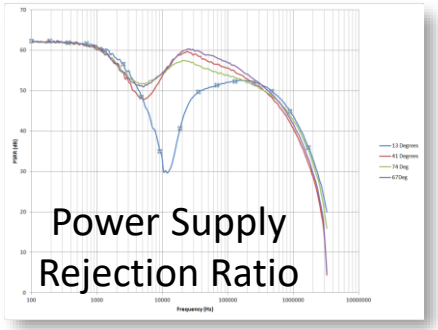
The model accurately matches the measurement

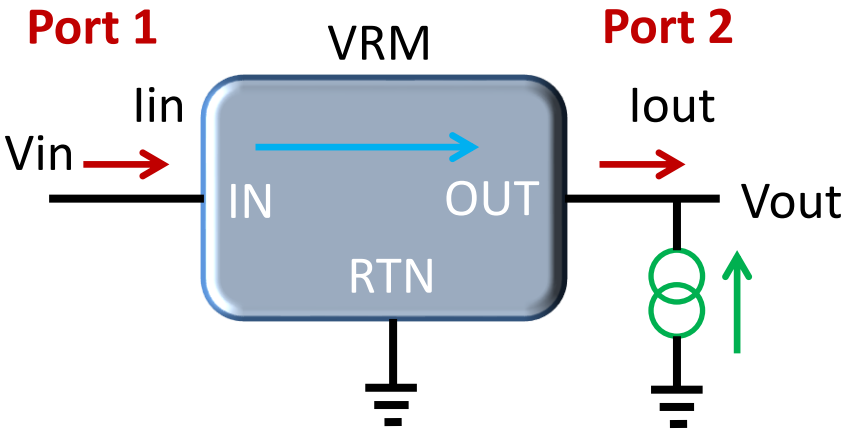
The Voltage Regulator Module (VRM) needs to consider <u>ALL</u> noise sources (large and small signal EMI)

Reverse Transfer - (S12)



PSRR - (S21)



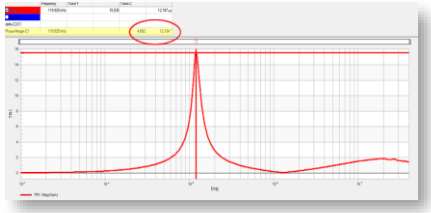


Input Impedance - (S11)

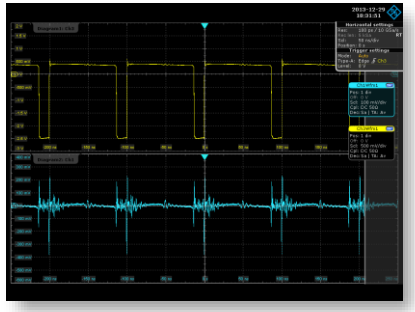
Input impedance can be NEGATIVE!

An R-L model only considers the output impedance

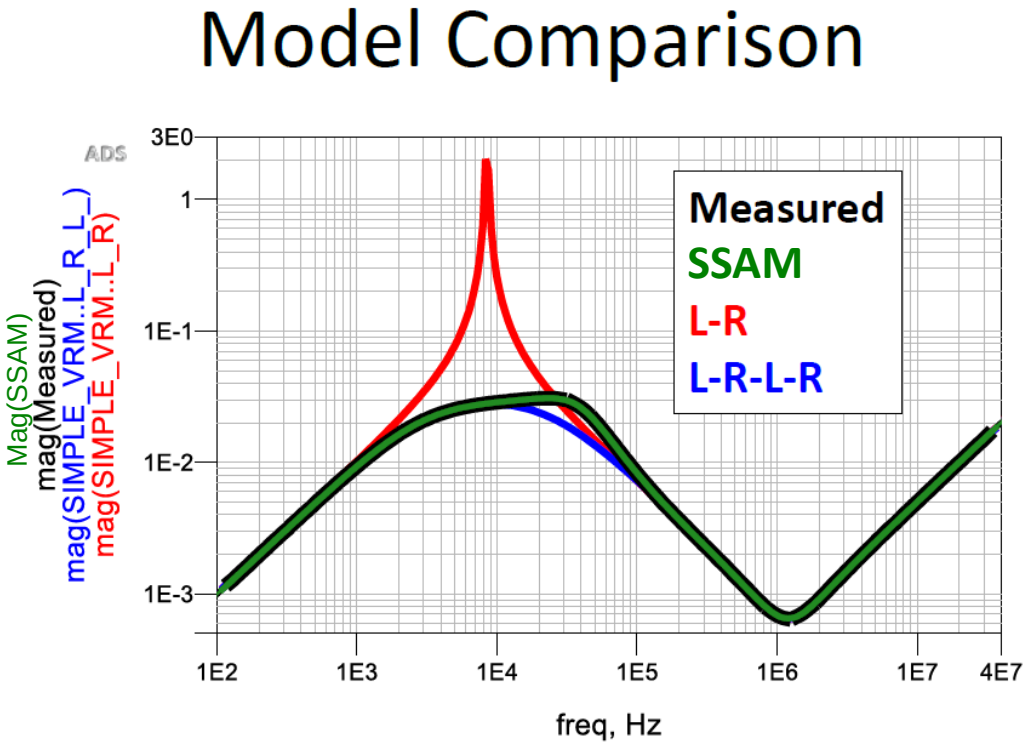
Output Impedance - (S22)



Output Noise/Spikes



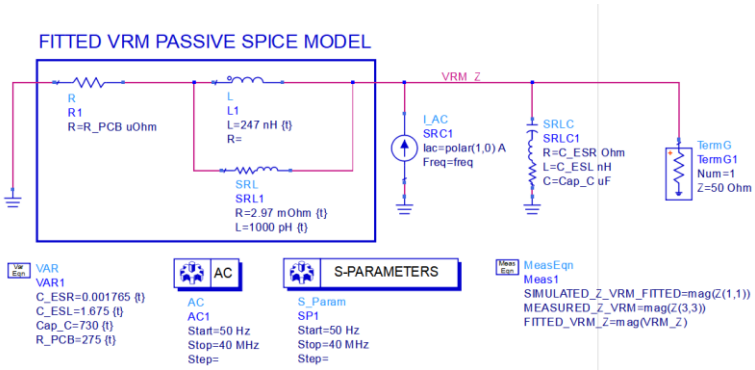
Evaluating the Results.. How much better is the SSAM VRM Model?

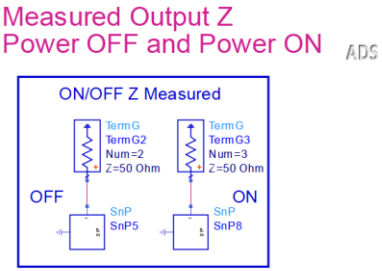


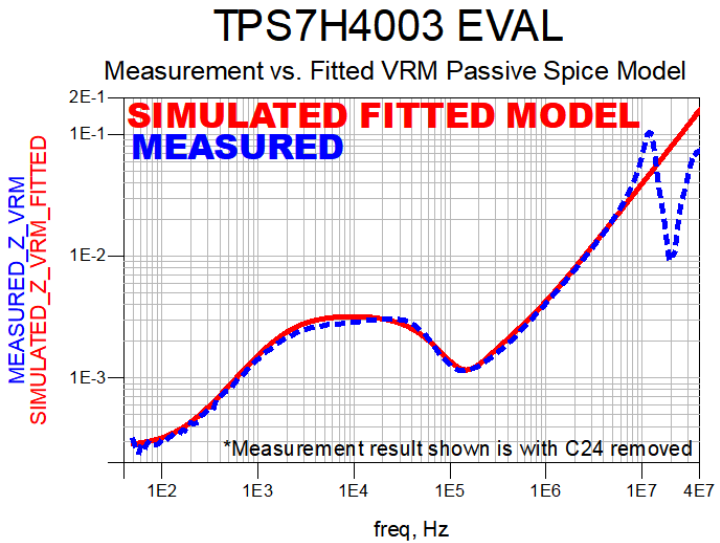
TPS7H4003 Measurement vs. Fitted Passive Spice Model

How much do we care about simulation with the PCB effects with the State-Space Average Model?

To answer that question, we need to first create a fitted passive spice VRM model



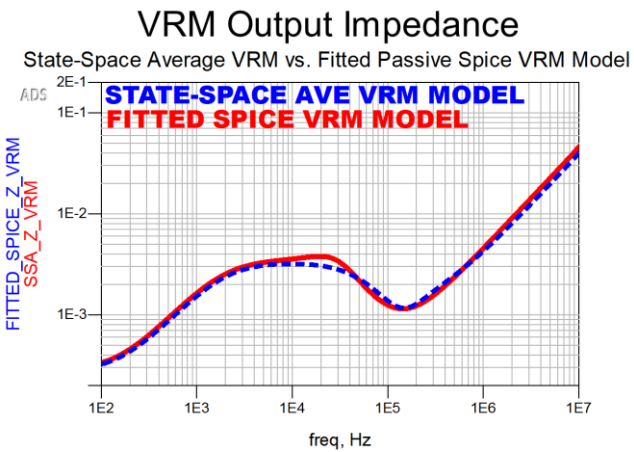




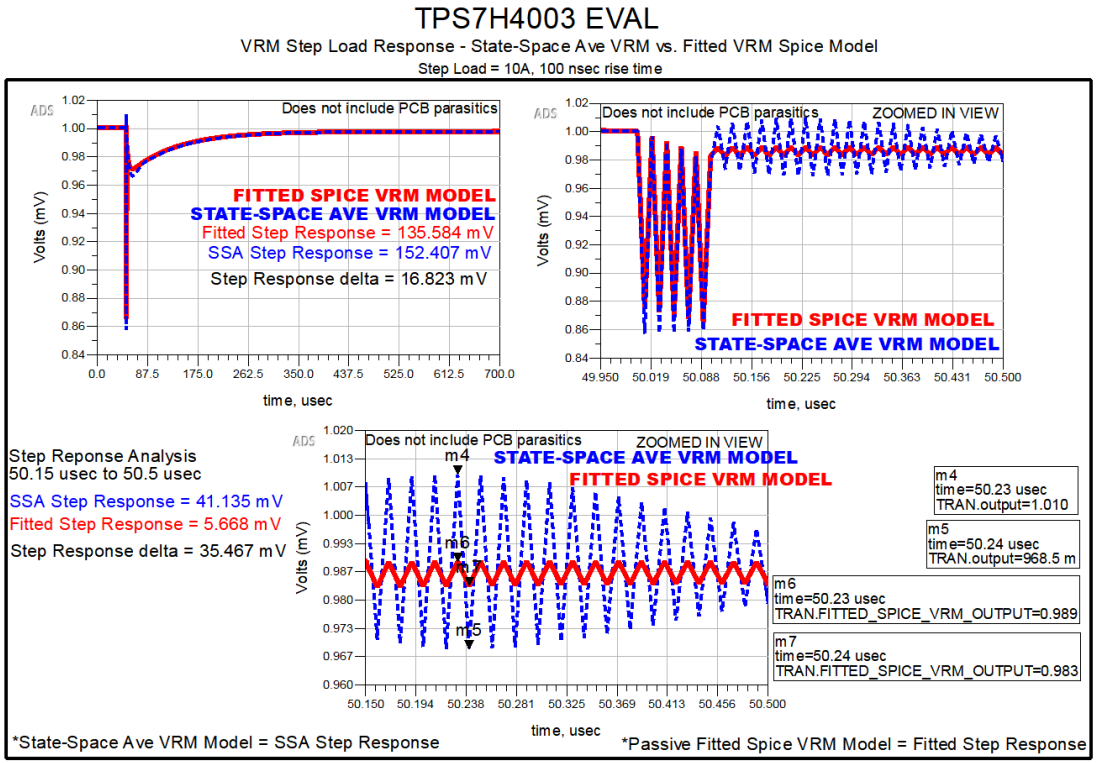
TPS7H4003 EVM with SSAM vs. Fitted Passive SPICE Model Step Response

10A, 100nsec step load without PCB effects

Comparing the step response between the State-Space Average Model and the Fitted Passive Spice VRM model



Output Impedance Correlates between both models



86% Change in transient step response between both models *without PCB Effects*

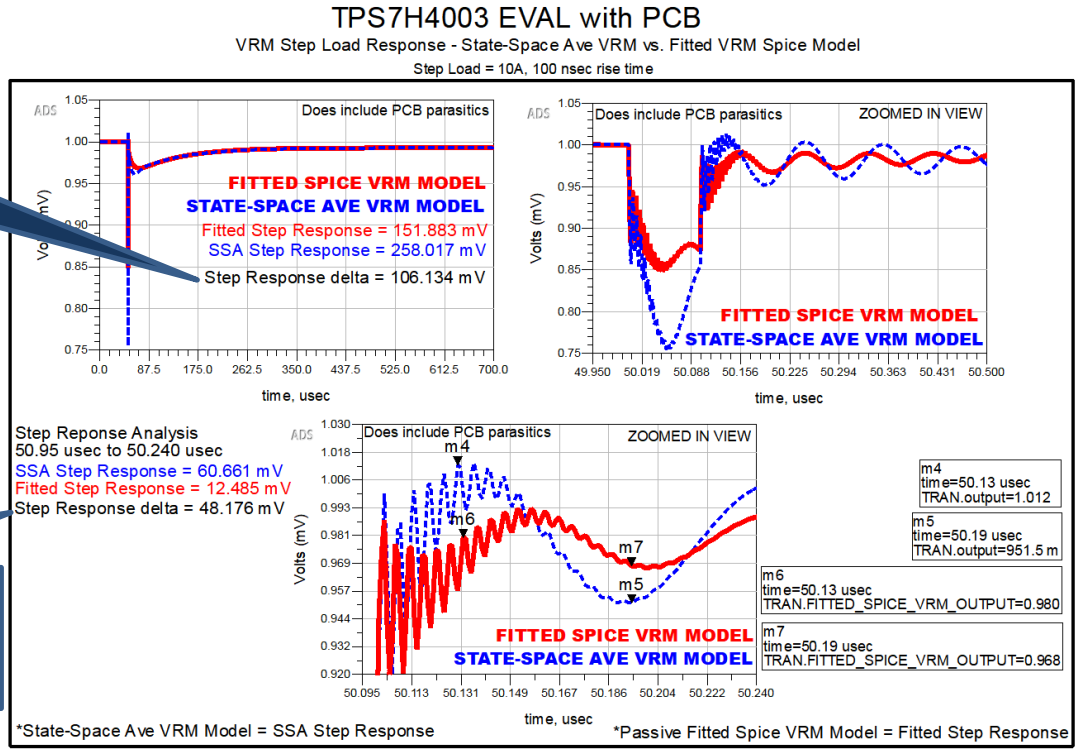
TPS7H4003 EVAL with SSAM vs. Fitted Passive Spice Model Step Response

10A, 100nsec step load with PCB effects

41% change in transient response from SSAM VRM model

Now let's include the PCB effects and compare the results again

79% change in transient response from SSAM VRM model

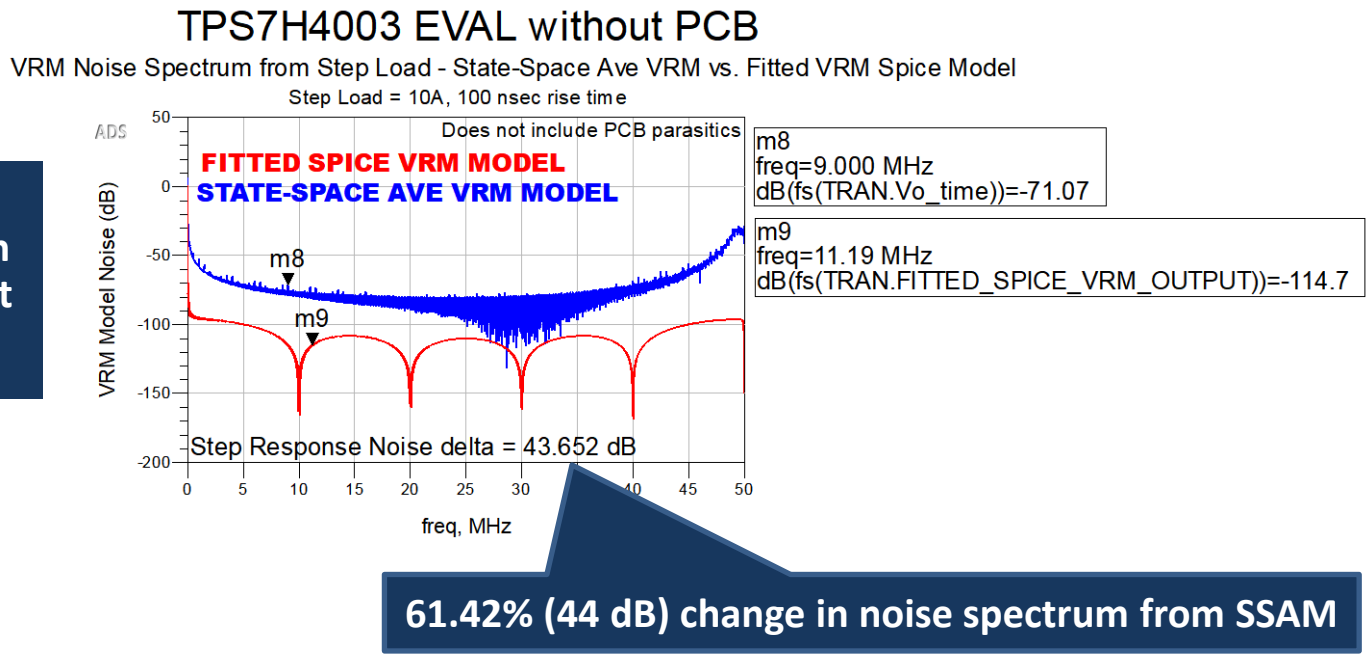


79% Change in transient step response between both models *with PCB Effects*

TPS7H4003 EVM with SSAM vs. Fitted Passive Spice Model Noise Spectrum from Step Response

10A, 100nsec step load <u>without</u> PCB effects

Let's compare the results in the noise spectrum without the PCB effects

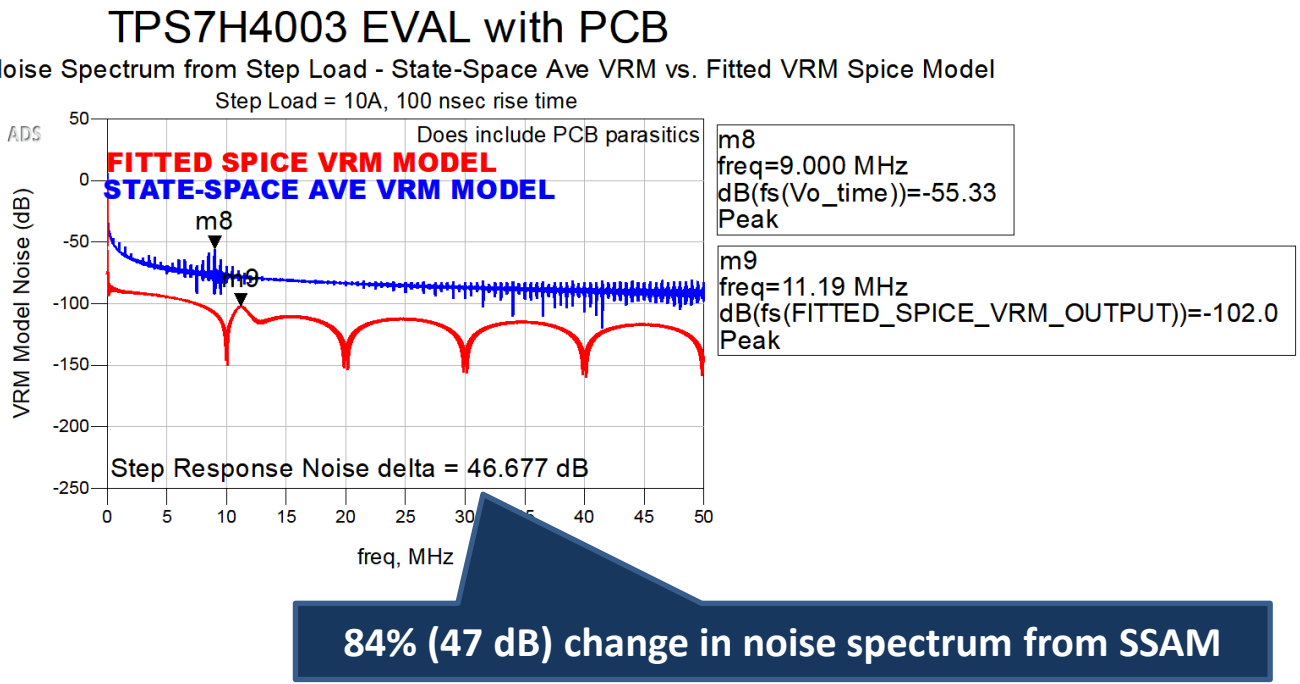


61% (44 dB) Change in transient step noise spectrum response between both models *<u>without PCB Effects</u>*

TPS7H4003 EVM with SSAM vs. Fitted Passive Spice Model Noise Spectrum from Step Response

10A, 100nsec step load <u>with</u> PCB effects

Now let's include the PCB effects and compare the results in the noise spectrum

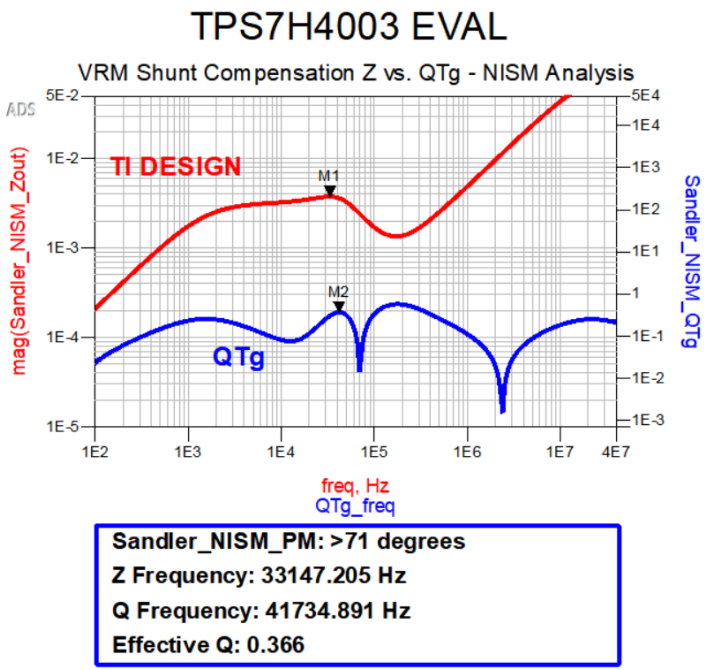


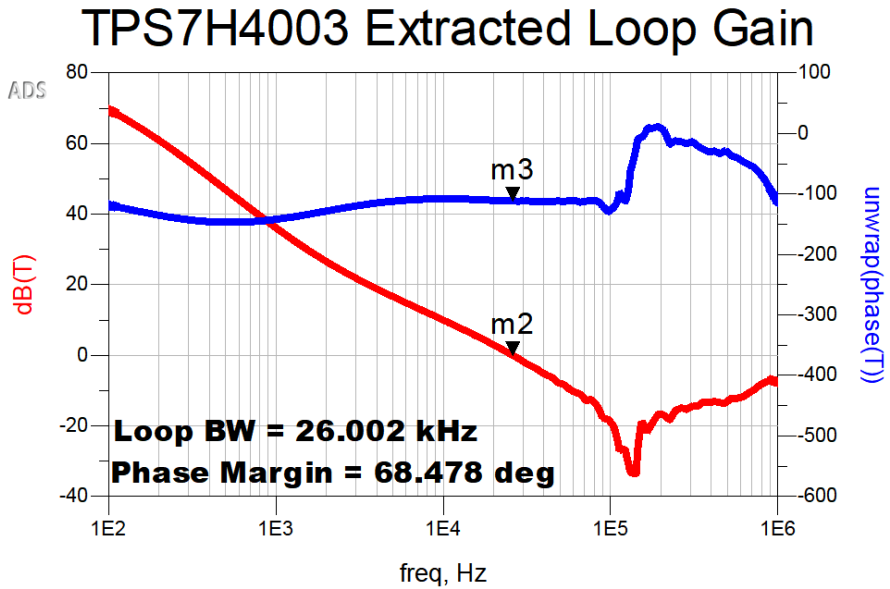
84% (47 dB) change in noise spectrum from SSAM

84% (47 dB) Change in transient step noise spectrum response between both models *<u>with PCB Effects</u>*

…..And Picotest NISM works in ADS also!

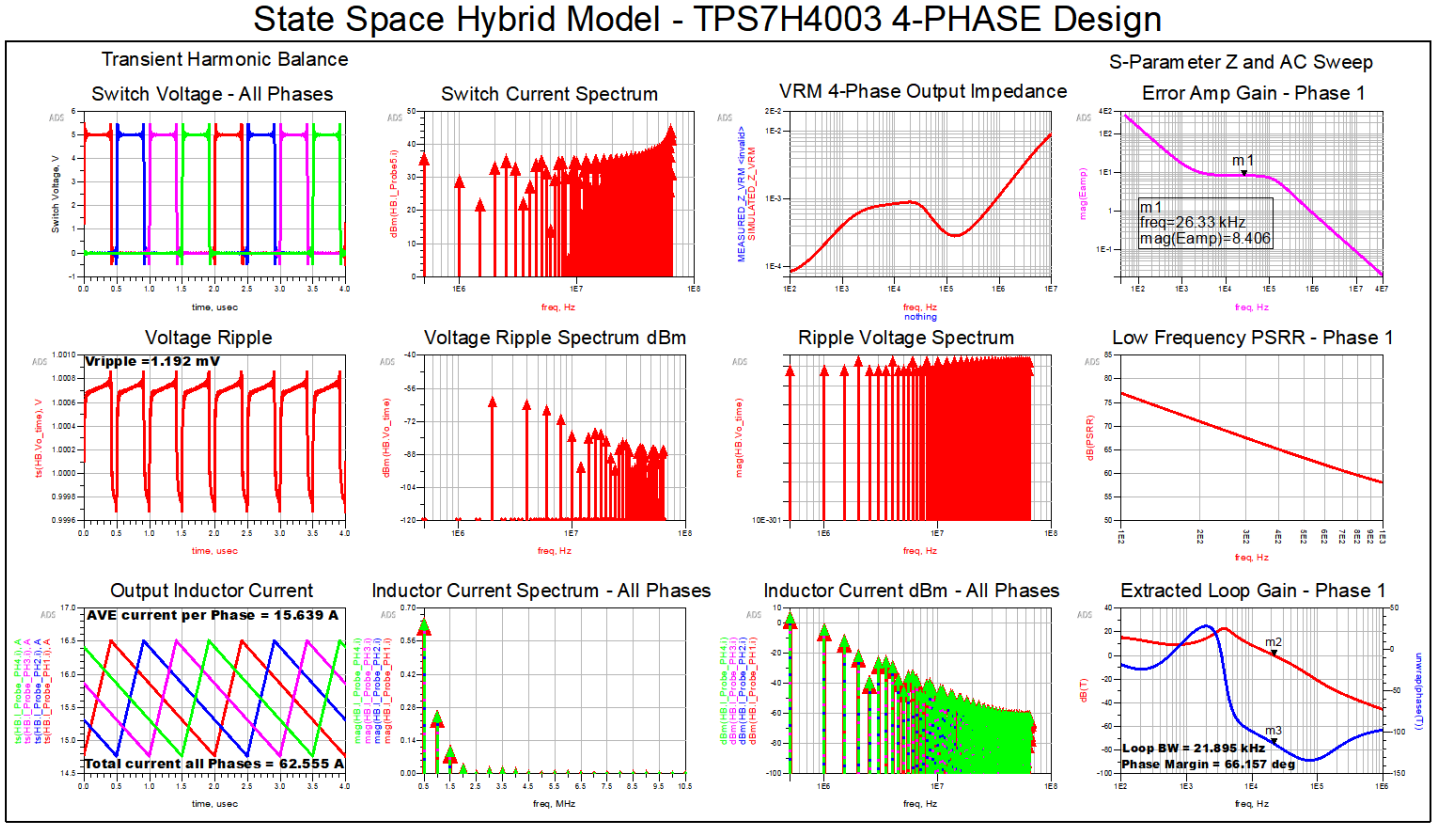
NISM* can be used for stability analysis of your VRM State-Space Average Model design with your PDN



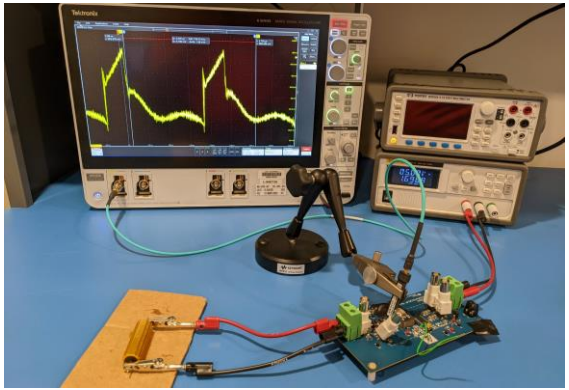


***Picotest Non-Invasive Stability Measurement (NISM)**

…. And it works for Multi-Phase and PMICs…



Call to Action



- Designers need to stop using the L-R, L-R-L-R VRM SPICE models for PI simulations!
  - The SSAM includes all 5 VRM noise sources for significantly higher fidelity
- The delineation between Power Integrity and Power Electronics needs to end!
  - PE designs need to include PCB EM with their VRM designs!
- Learn to make these simple measurements and try this for yourself
- Download the ADS workspace to see the model and simulations https://www.picotestonline.com/Designcon2023

- **How to Design for Power Integrity: Selecting a VRM**

Conclusion and Summary

- Accurate simulation results require a high-fidelity VRM model and the PCB effects!
- It takes 4 measurements to build an accurate Sandler State-Space Average VRM model
  - However, these State-Space Average Models do not need to be perfect!
- The Sandler State-Space Average VRM Model is…..
  - Easy to populate for VRMs
  - Supports EM simulations
  - Supports many modes and multi-phase
- A poor fidelity State-Space Average Model is significantly better than a good R-L VRM model

References

1. DesignCon 2017 Slides – Characterizing and Selecting the VRM by Steve Sandler
2. DesignCon 2017 Paper – Characterizing and Selecting the VRM by Steve Sandler
3. H. Barnes, J. Carrel, S. Sandler, “A Method for Dynamic Load Current Testing with a Benchtop Power Supply”, DesignCon 2020.
4. H. Barnes, J. Carrel, S. Sandler, “Capacitor Placement Strategies for Optimum Power Integrity” DesignCon 2021.
5. H. Barnes, J. Carrel, S. Sandler, “Practical Methods of Estimating Dynamic Current for Calculating PDN Target Z”, DesignCon 2022.
6. Bode 100 PSRR Application Note
7. Techniques for Accurate PSRR Measurements
8. Measurement Based VRM Modeling
9. Picotest P2102A-1X 2-port PDN Transmission Line Probe
10. Application Note - 2-Port Impedance Measurement using the P2102A Probe and Bode 100 VNA
11. Picotest J2113A Semi-Floating Differential Amplifier
12. Picotest J2102B Common Mode Transformer
13. Picotest BNC-BNC 0.25m PDN Cable
14. Picotest J2120A Line Injector
15. Bode 100 VNA
16. TPS7H4003-SEP data sheet, product information and support | TI.com
17. TPS7H4003EVM Evaluation board | TI.com
18. TPS7H4003-SEP Radiation-Tolerant 3-V to 7-V Input 18-A Synchronous Buck Converter in Space Enhanced Plastic datasheet
19. Non-Invasive Stability Measurement
20. AMD-Xilinx ZCU104 Evaluation Kit: https://www.xilinx.com/products/boards-and-kits/zcu104.html
21. S. Sandler, “How to Design for Power Integrity” Keysight sponsored YouTube Video Series: http://www.keysight.com/find/how-to-videos-for-pi
22. PathWave ADS: Power Integrity Simulation Workflow with PIPro https://www.youtube.com/watch?v=iUzGrovf6Wo
23. Keysight PathWave PIPro – https://www.keysight.com/us/en/product/W3034E/pathwave-pipro.html

Thank you!

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QUESTIONS?