Improved Methodology to Accurately perform System Level Power Integrity Analysis Including an ASIC die

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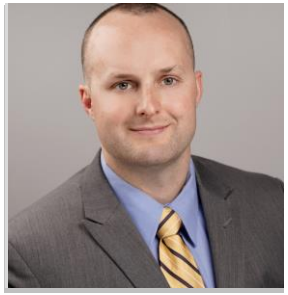
SPEAKERS



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Benjamin Dannan is a Technical Fellow and a Staff Digital Engineer at Northrop Grumman Mission Systems. He has a BSEE from Purdue University, a Masters of Engineering in Electrical Engineering from The Pennsylvania State University, and graduated from the USAF Undergraduate Combat Systems Officer training school with an aeronautical rating. He received the prestigious DesignCon best paper award in 2020 and is also a Keysight Certified Expert in ADS.

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Will McCaffrey is a Principal Digital Hardware Engineer at Northrop Grumman Mission Systems. He holds a BSEE from Rochester Institute of Technology in Rochester NY, and currently pursuing a MSEE at Johns Hopkins University. Since 2018 he has designed hardware interconnects for a CubeSat, designed several DDR4 implementations on high speed mixed-signal PCBs as well as designed his own high-speed mixed signal PCB. His interest is in high-speed digital design and SI/PI simulations.

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Jim Kuszewski is a Technical Fellow and a Consulting engineer at Northrop Grumman Mission Systems. He holds a BSEE from Michigan State University and a MSCS from the Johns Hopkins University. Jim is the founder of the Northrop Grumman Mission Systems Signal Integrity / Power Integrity Community of Practice. He has also worked on design automation, system security and product integrity initiatives. Currently Jim oversees many programs which use high density, multi-gigabit speed SerDes, DDR memory, mixed signal, fine pitch, and high-power dissipation digital components as well as multi-chip module substrate design.

Today's Key Takeaways

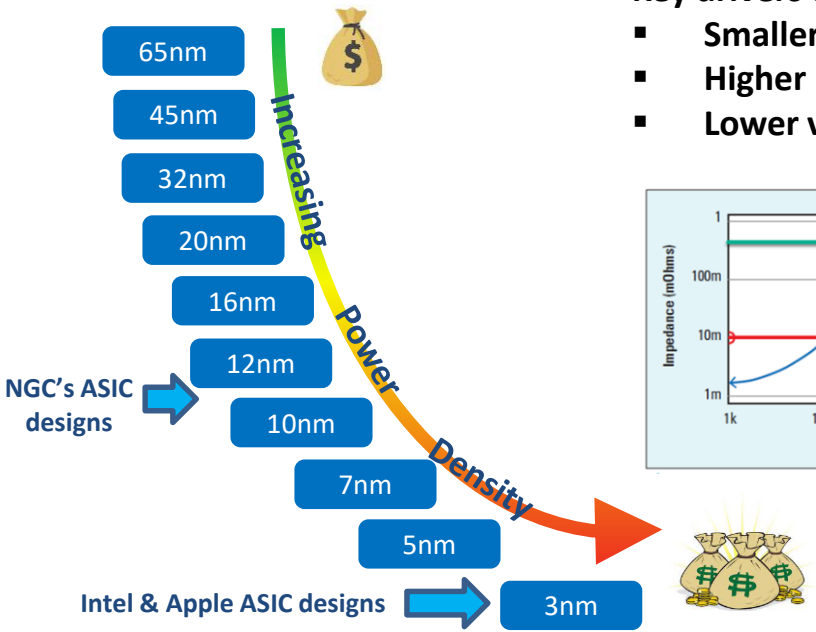
- **Know what your target PDN impedance needs to be for your VRM, board, substrate and die.**

- **A clear methodology on how to know if the voltage ripple at the die bumps on a substrate is within the defined specification of the ASIC**

Overview

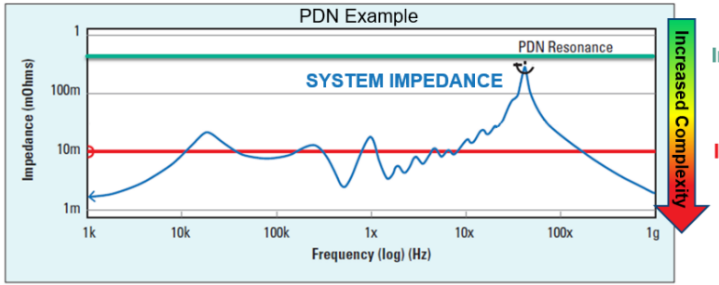
- Power integrity challenges and drivers with ASICs
- PI Methodology workflow with ASICs
- CPM model generation
- Calculating your target impedance
- Substrate model generation and optimization
- Full PDN analysis
- CPM modulation
- Time domain analysis with voltage ripple
- Next steps
- Summary
- Questions

Power Integrity Challenges and Drivers



Key drivers of PI Challenges

- Smaller silicon technology
- Higher power (& current) densities on ASIC chips
- Lower voltage margins on ASIC chips

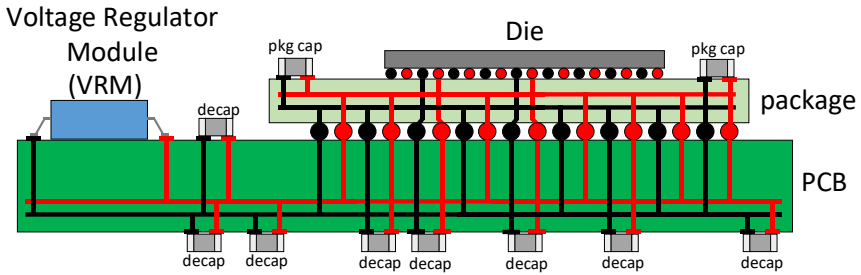


Impedance Target for ASICs ~10 years ago

Impedance Target for today's ASICs

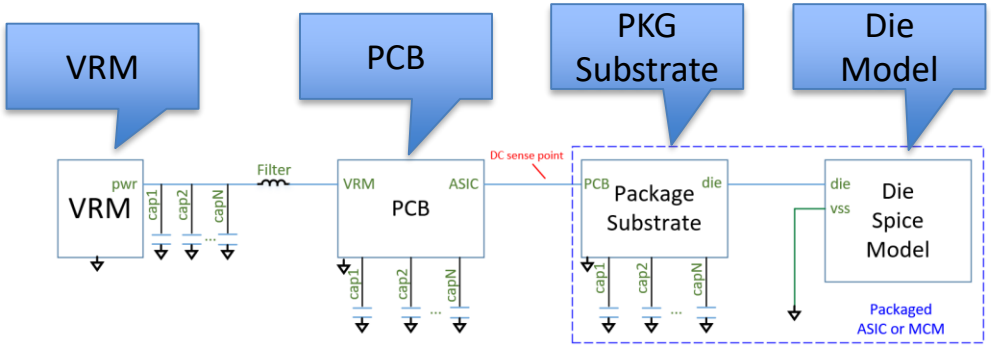
Impedance design targets for today's ASICs cost more money & time to develop

Definition of PI Workflow with ASICs



Power Integrity System Model

4 Main Blocks for PI System Analysis

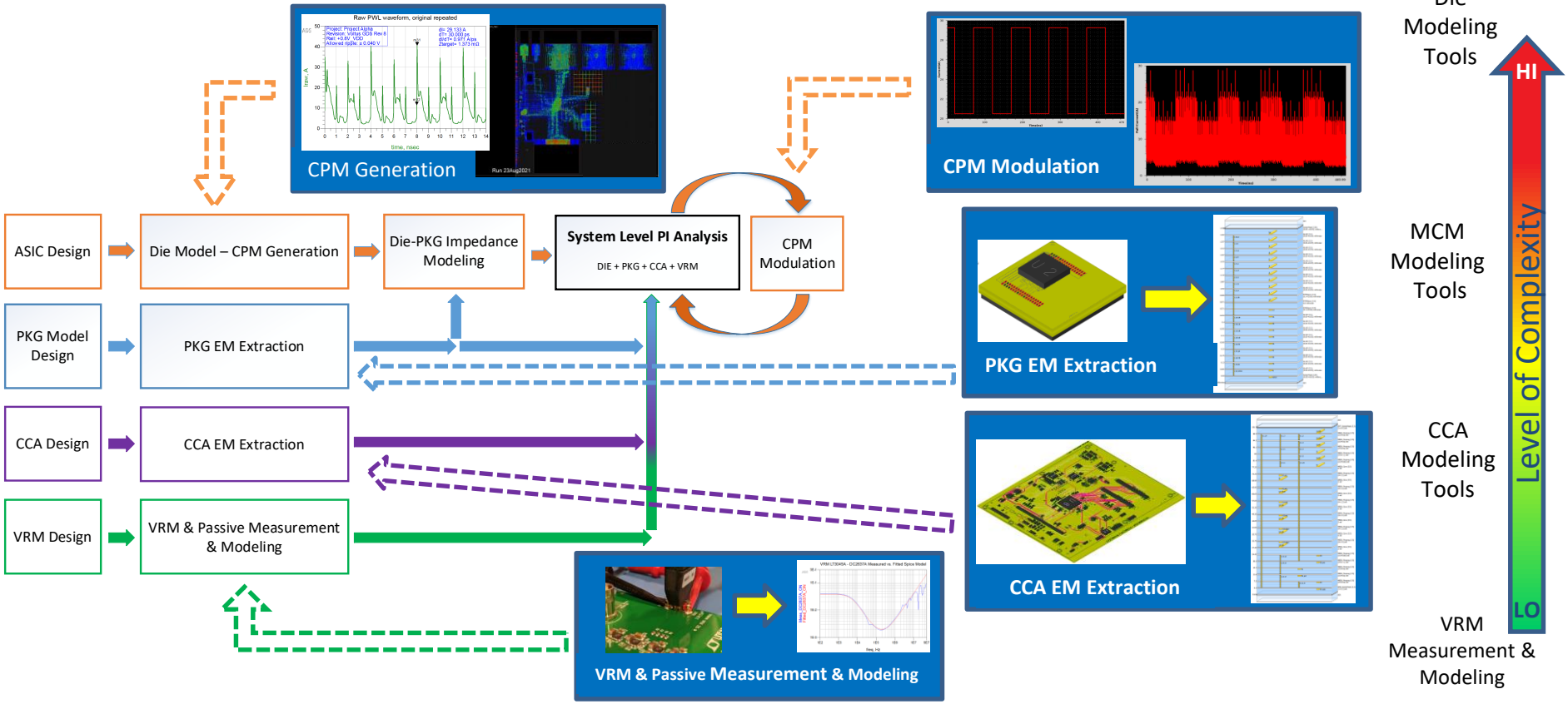


Power Integrity System Diagram Model

- **As node geometries decrease on ASICs, there are more transistors causing additional current draw and voltage ripple requirements are tighter.**

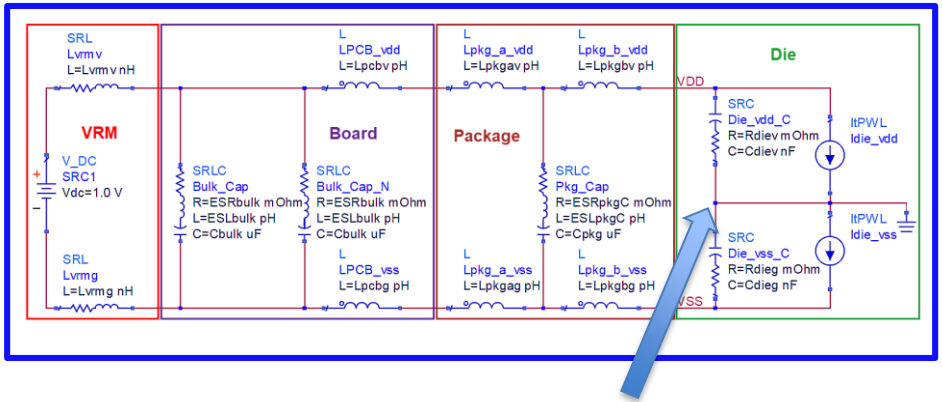
We cannot change the current draw, but we can manage the voltage ripple

Definition of PI Workflow with ASICs

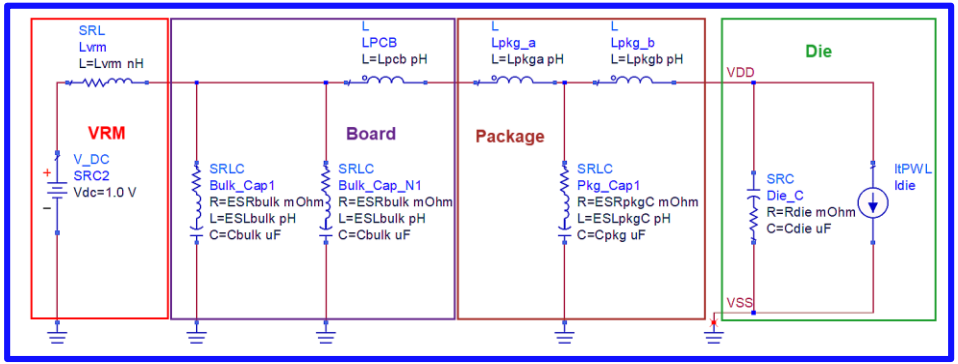


Die Model Extraction - Partial versus Looped Model

Partial die Model



Looped die Model



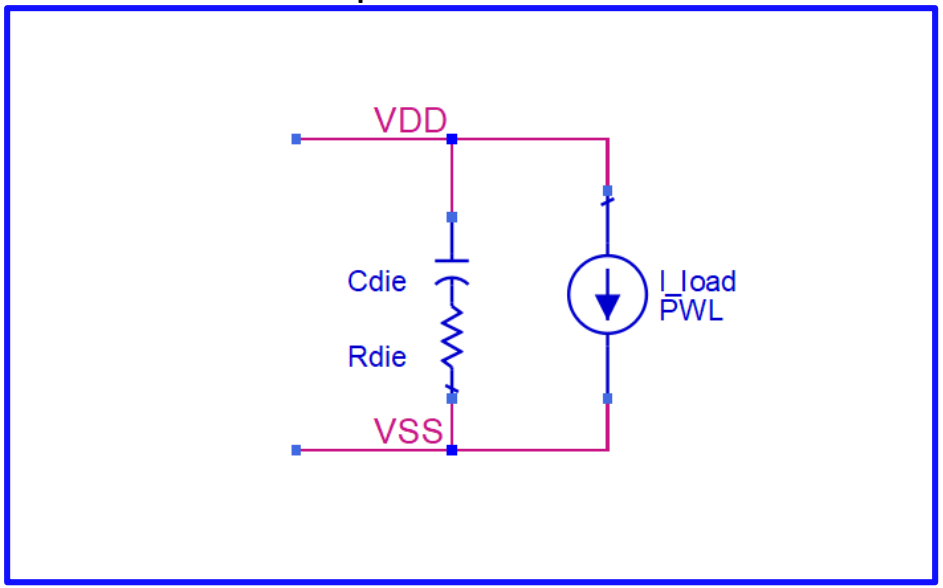
die Spice Node 0 enabled with die model

Spice Node 0 disabled

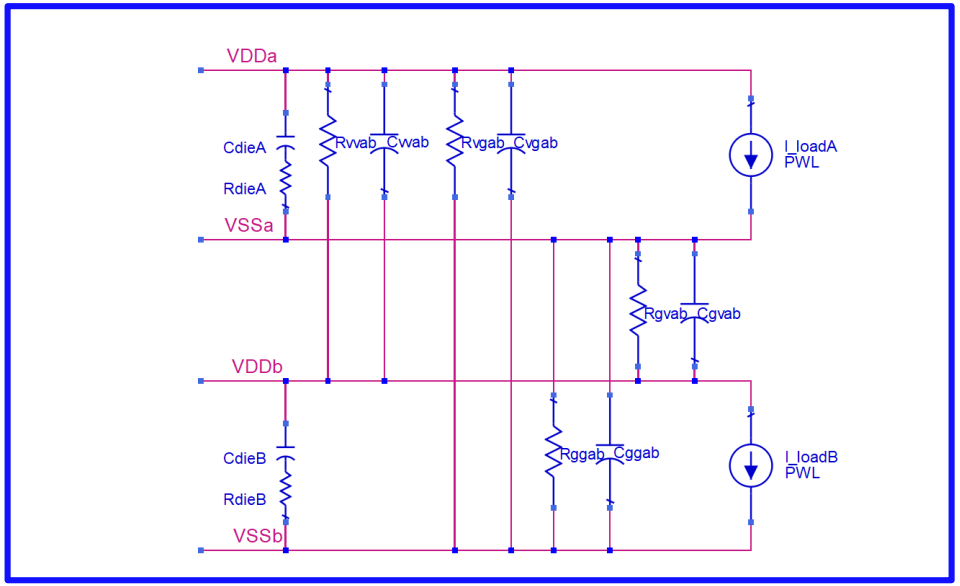
- **By disabling spice node 0, VDD and VSS are referenced to each other which is essential for the current loop when generating the CPM model**
- **For looped models, the passive elements on the VDD rail is the combination of passive elements of the actual VDD and actual VSS rails**

Die Model Extraction - Lumped versus Distributed Model

Lumped die Model

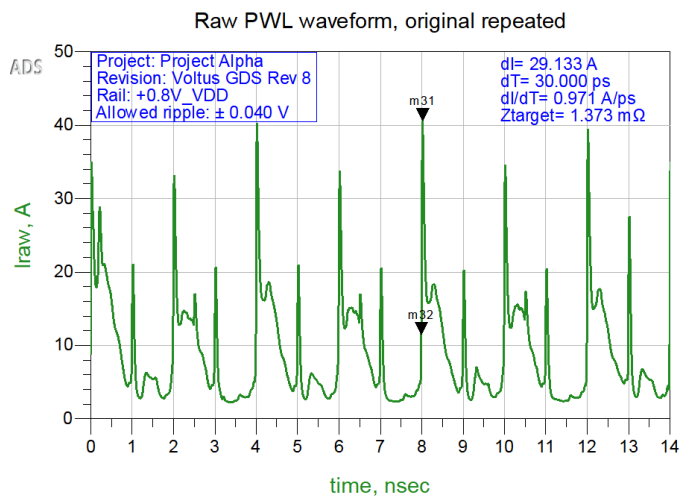


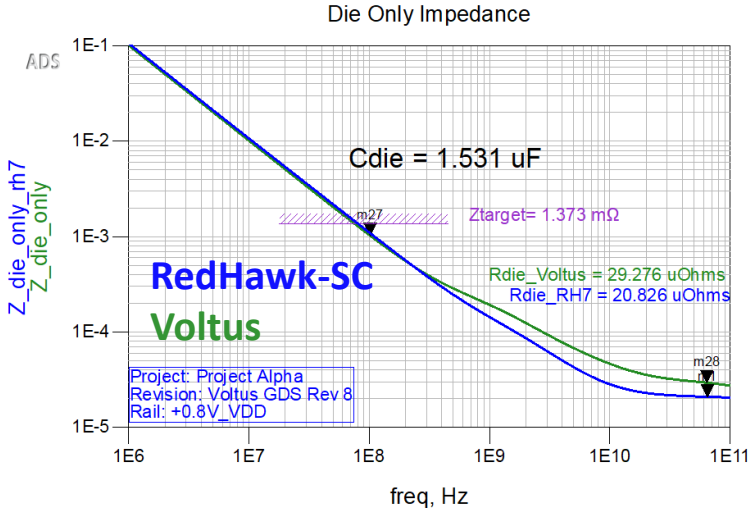
Distributed die Model



- **Lumped models have one load current, one $C_{DIE}R_{DIE}$ and two nodes**
- **Distributed models have multiple load currents, with multiple $C_{DIE}R_{DIE}$, one node per die bump, and passive interaction between all nodes**

Die Model Extraction Comparison Verification





- **The CPM Die model Extractions consists of 2 primary components:**

1. **Piece-wise linear (PWL) waveform representing current at the die bumps**
2. **Passive spice model which includes R_{DIE} and C_{DIE}**

***Recommendation is to generate CPMs as lumped and looped model**

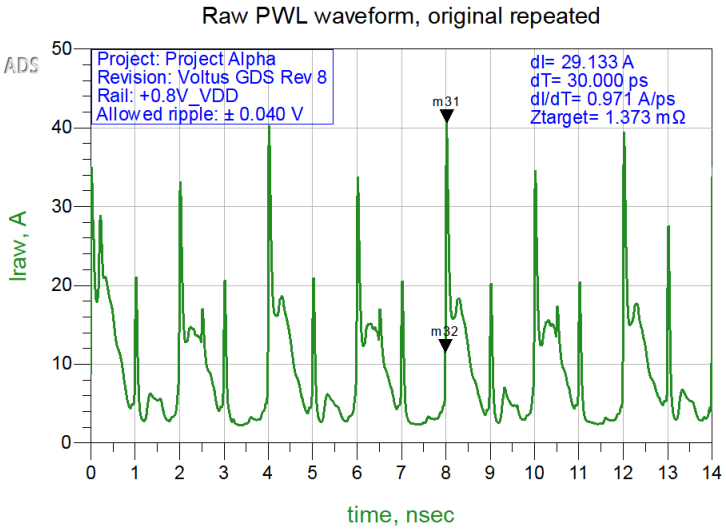
Extracted die model shows great correlation with 2 EDA tools, which also validates our passive die model!

Target Impedance – The Traditional Way

- Typically, the expectation is to calculate Z_{TARGET} based on the maximum transient current.
- Using the PWL waveform example shown

$$Z_{TARGET} = \frac{\Delta V}{\Delta I}$$

- ΔV is the allowed voltage variation
  ΔI is the current change where dI/dT is maximum
  ΔV = V_{RIPPLE} = 5% of 0.8V = 40mV, ΔI = 29.133A
- This makes Z_{TARGET} = *1.37 mΩ*
- Analysis shows that violation of this impedance target will still provide a V_{RIPPLE} in spec. Therefore, this Z_{TARGET} is too conservative!



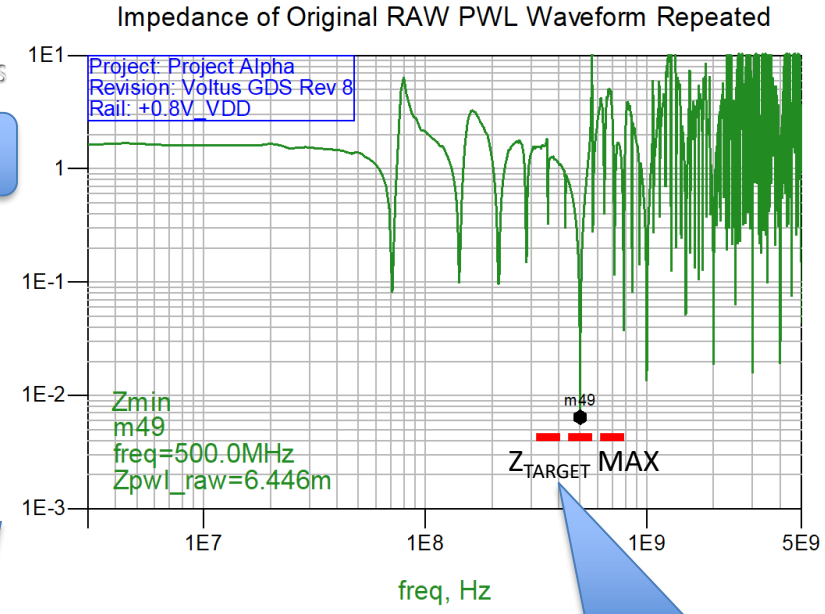
Target Impedance – The Right Way with a CPM

Source: screenrant.com

$$Z_{PWL\_raw} = \frac{V_{RIPPLE}}{mag(I_{PWL})} = \frac{40\ mV}{mag(I_{PWL})}$$

$$Z_{TARGET}(f_0)\frac{\Delta V}{\Delta I(f_0)}$$

$$Z_{TARGET\ MAX}(500\ MHz) = \frac{40\ mV}{6.2\ A} = \sim 6.5\ m\Omega$$

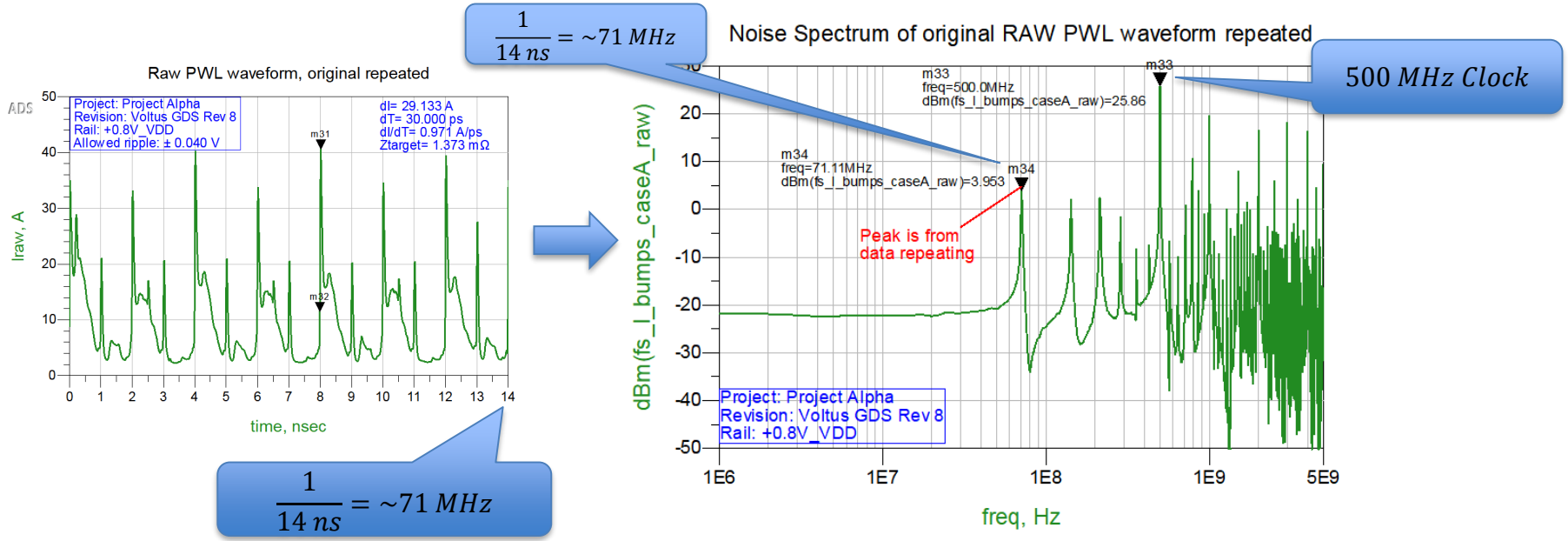


Or we can plot Z_{PWL_RAW} to determine $Z_{TARGET\ MAX}$

Z_{PWL_RAW} Lowest impedance point can be used to calculate Z_{TARGET} for entire PDN for this CPM's PWL waveform

Noise Spectrum of CPM

- CPM generation is very compute intensive
  - Modeled dynamic current only represents a short window of actual die activity (typically a few clock cycles)
  - When repeating the CPM data, artifacts are created in the noise spectrum.

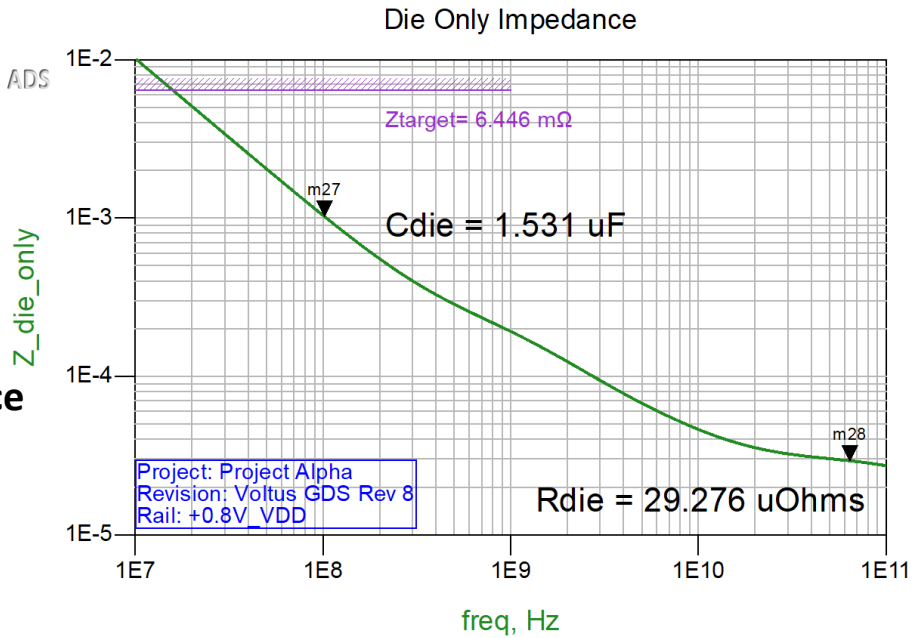


Die Model Analysis - Calculating C_{DIE} and R_{DIE}

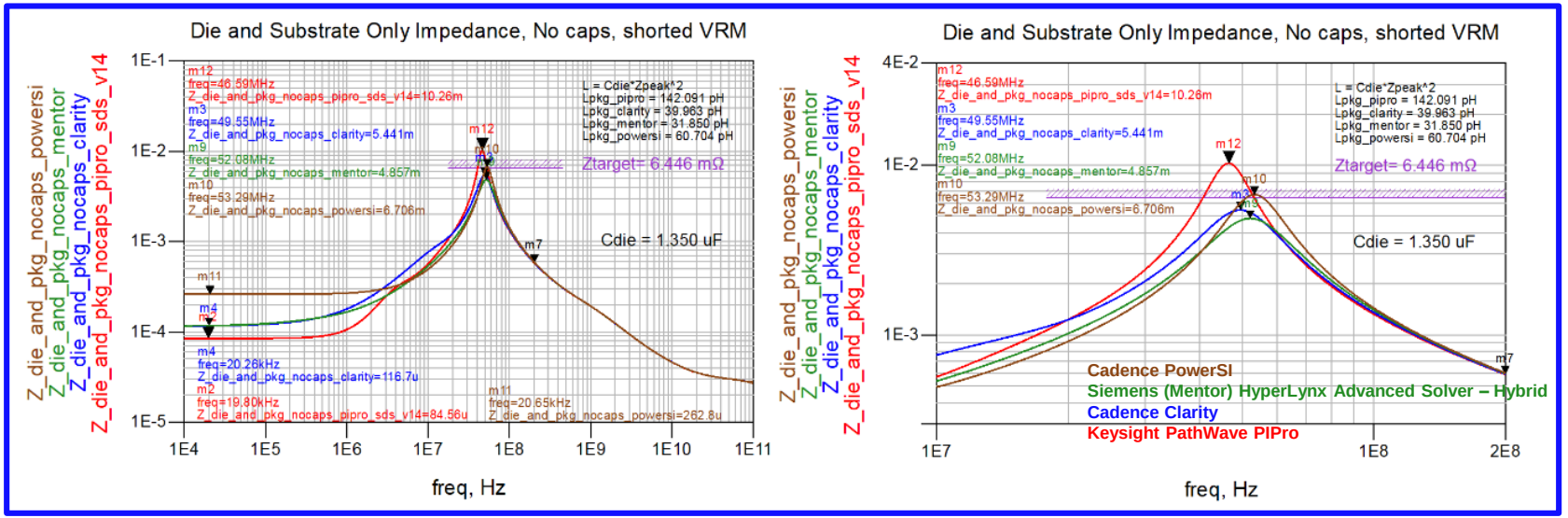
- **Impedance of R_{DIE} should never be above that of C_{DIE}**

$$C_{DIE\ MIN} = \frac{1}{2\pi f Z_{TARGET}} = \frac{1}{(2\pi)(100MHz)(6.446m\Omega)} \approx 247\ nF$$

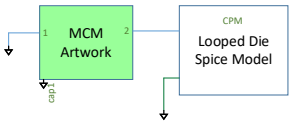
- **Ideally the ASIC should provide enough capacitance to meet Z_{TARGET} above 100 MHz**
- **Present substrate technology limits the effectiveness of the PCB PDN to around 100 MHz**



Substrate Artwork Extraction Verification



Setup for Model Shown



Correlation shown across multiple EM tools, this validates substrate artwork extraction

Substrate Design Goals

- Calculating max L_{PKG} ($L_{PKG\ IDEAL}$) to meet design goal of Z_{TARGET}

Z_{TARGET} = 6.446 mΩ

$$L_{PKG\ IDEAL} = \frac{Z_{TARGET}}{2\pi f} = \frac{6.446\ m\Omega}{(2\pi)(100MHz)} = 10.3\ pH$$

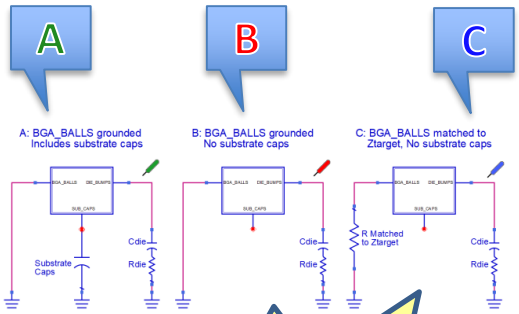
- However, ($L_{PKG\ IDEAL}$) represents a very low inductance that would require an excessively high number of substrate balls (both die bumps and BGA balls) to meet this inductance.

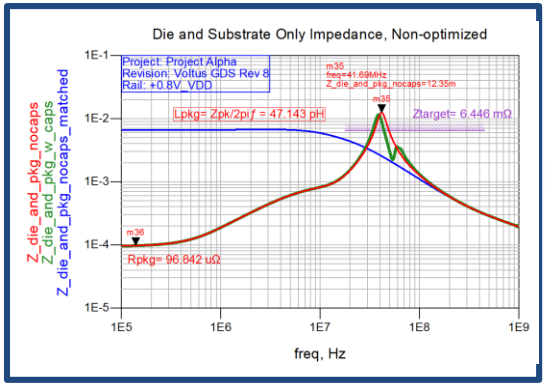
Next step is to consider adding mid-to-high frequency decoupling on-substrate

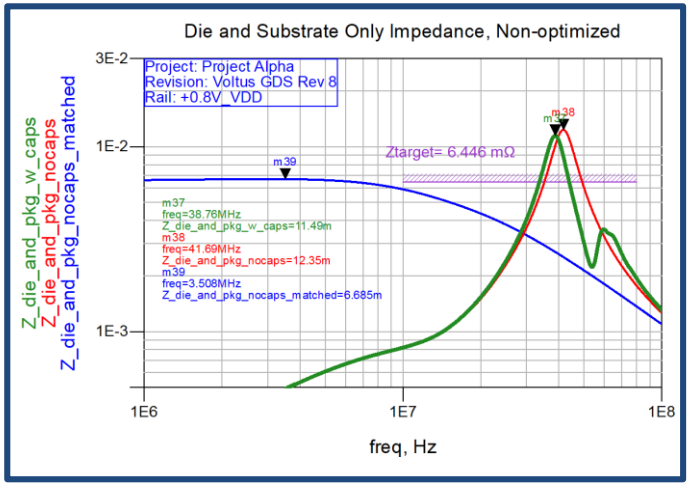
Substrate Artwork Analysis

- **After substrate artwork extraction**

Z_{TARGET} = 6.446 mΩ





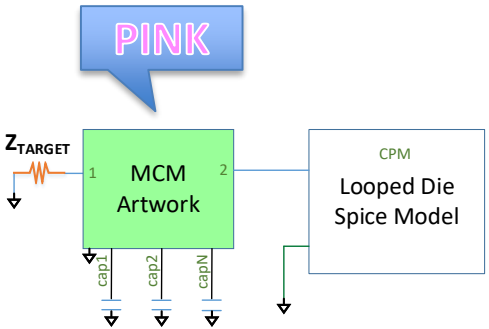


Substrate optimization needs to occur matched to a Z_{TARGET}

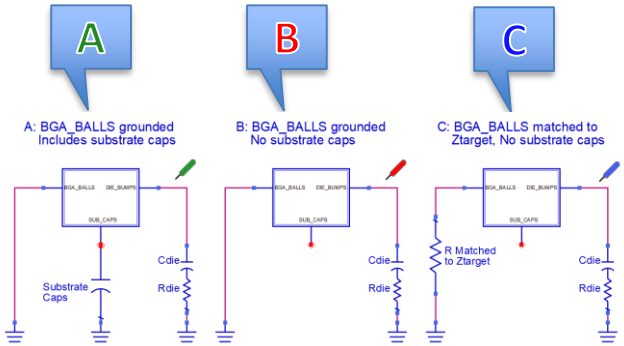
PDN Configuration	Impedance Peak (mΩ)	Percent Impedance Change from configuration B
B: BGA balls grounded, no caps included on the substrate	12.35	-
A: BGA balls grounded, 43 0.01uF caps included on the substrate	11.49	-6.9%
C: BGA balls connected to a resistor matching Z_{TARGET}, no caps included on the substrate	6.685	-46%

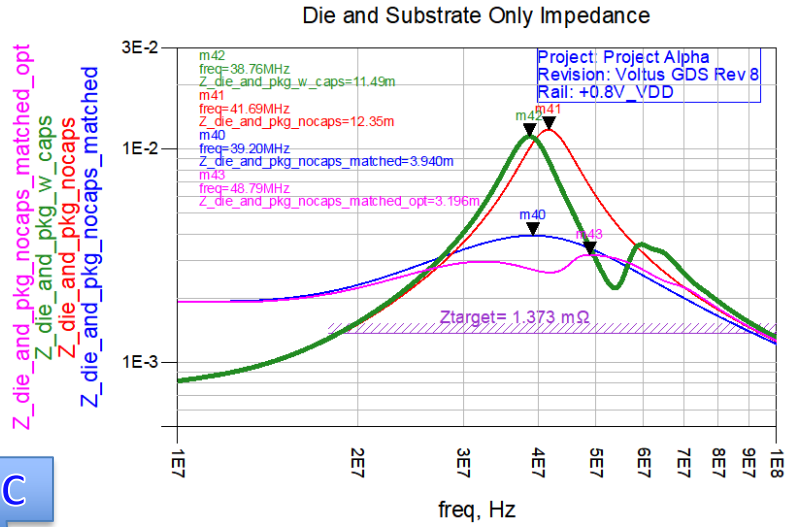
Package Design Optimization

- **Green is non-optimized, and pink is optimized (with a matched board impedance).**
- **QTYx14 of the 0.01uF (0201 pkg) capacitors were replaced with QTYx5 0.022uF (0201 pkg) capacitors**
- **Impedance peak drops from 3.94 mΩ (BLUE) to 3.19 mΩ (PINK) or 19%**



Z_{TARGET} = 1.37 mΩ



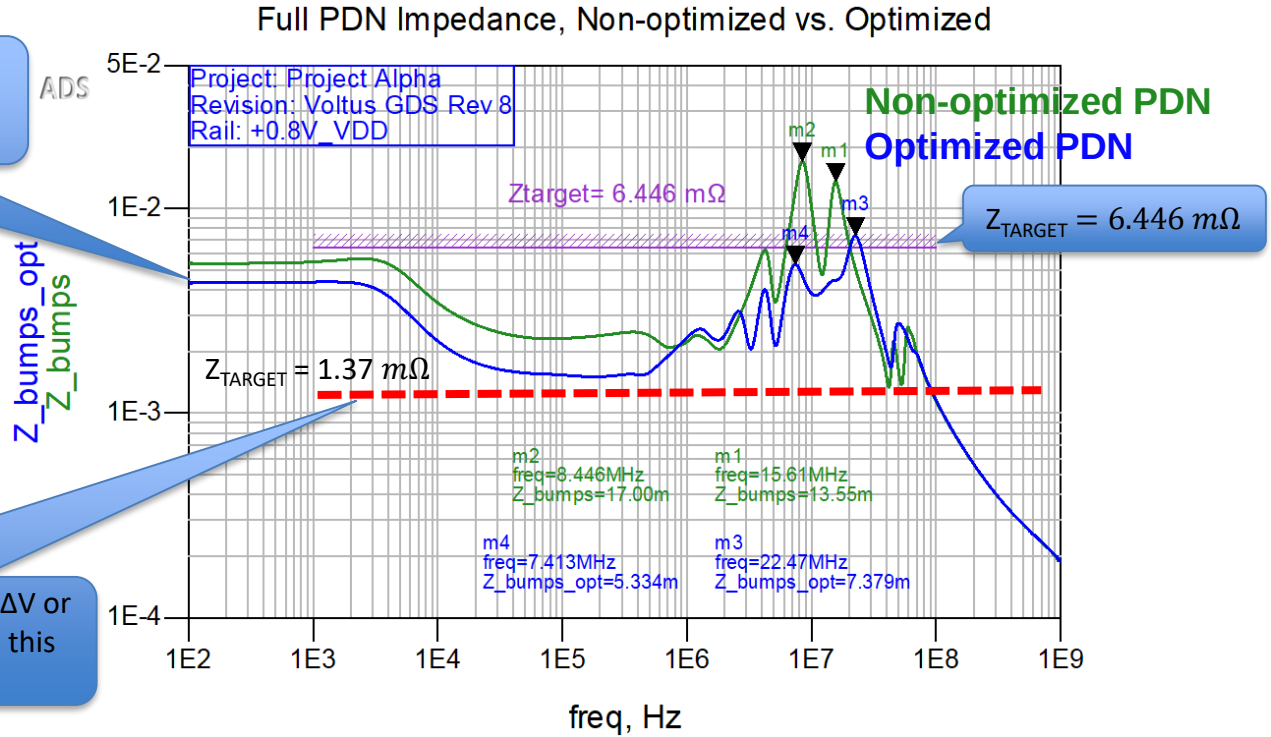


PKG w/No Caps matched to Z_{TARGET}

Optimized PKG w/caps matched to Z_{TARGET}

Full PDN Analysis – Impedance

BLUE = Optimized on-package and PCB capacitors, removal of filter inductor and resistor



$Z_{TARGET} = 6.446\ m\Omega$

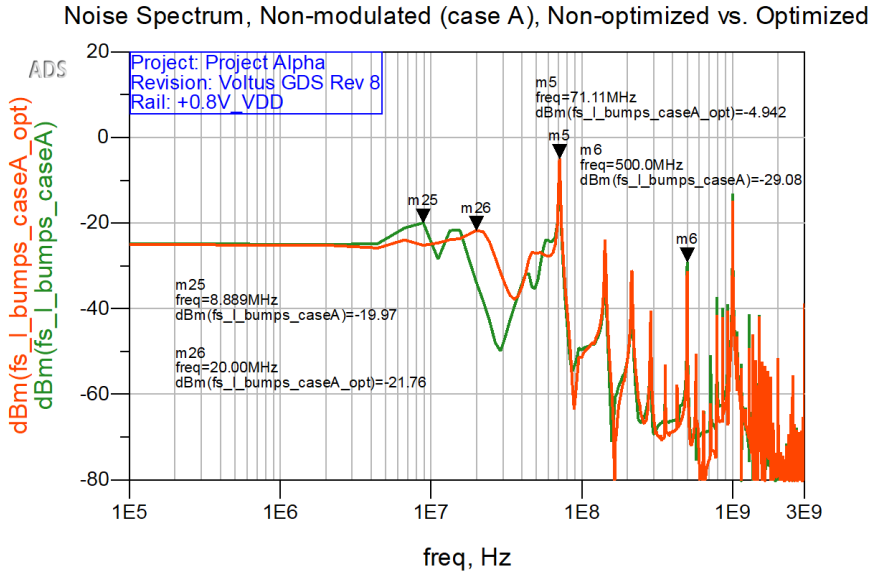
$Z_{TARGET} = 1.37\ m\Omega$

$Z_{TARGET} = 1.37\ m\Omega$ is too **conservative**, since ΔV or V_{RIPPLE} results shown are not be violated with this PDN design.

After Optimization only 1 impedance peak exceeds $Z_{TARGET} = 6.446\ m\Omega$

Full PDN Analysis – Noise Spectrum

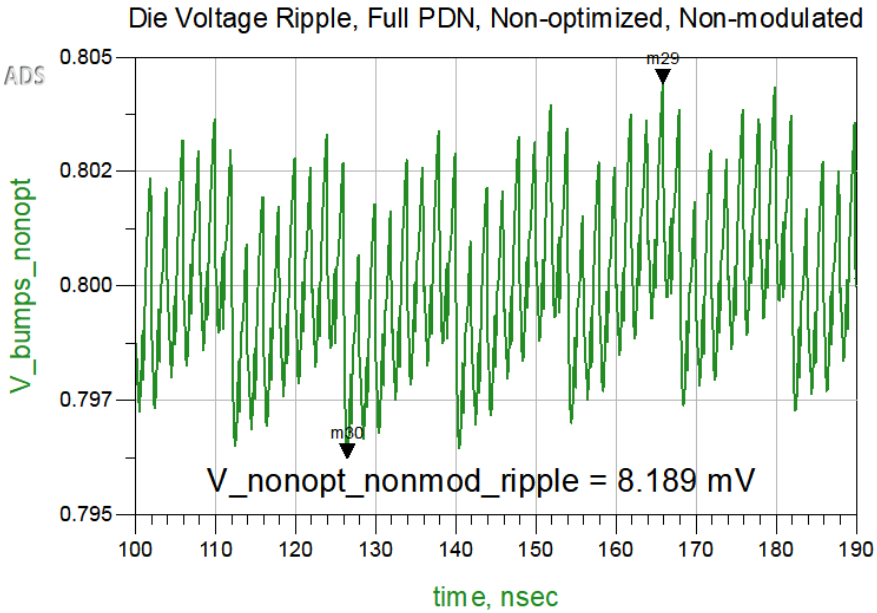
- **Capacitor changes had no effect above ~65 MHz**
- **At 9 MHz, noise was reduced by 2.5 dBm**
- **Noise is directly comparable to the impedance profile in the PDN.**

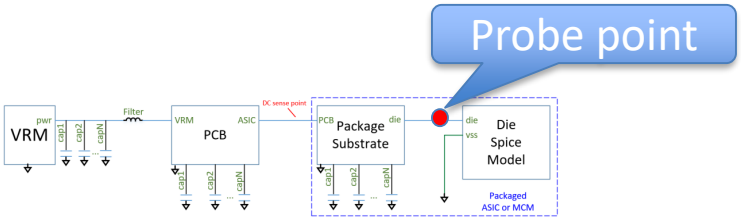


Non-optimized PDN – No Modulation
Optimized PDN – No Modulation

Time Domain Voltage Ripple without Modulation

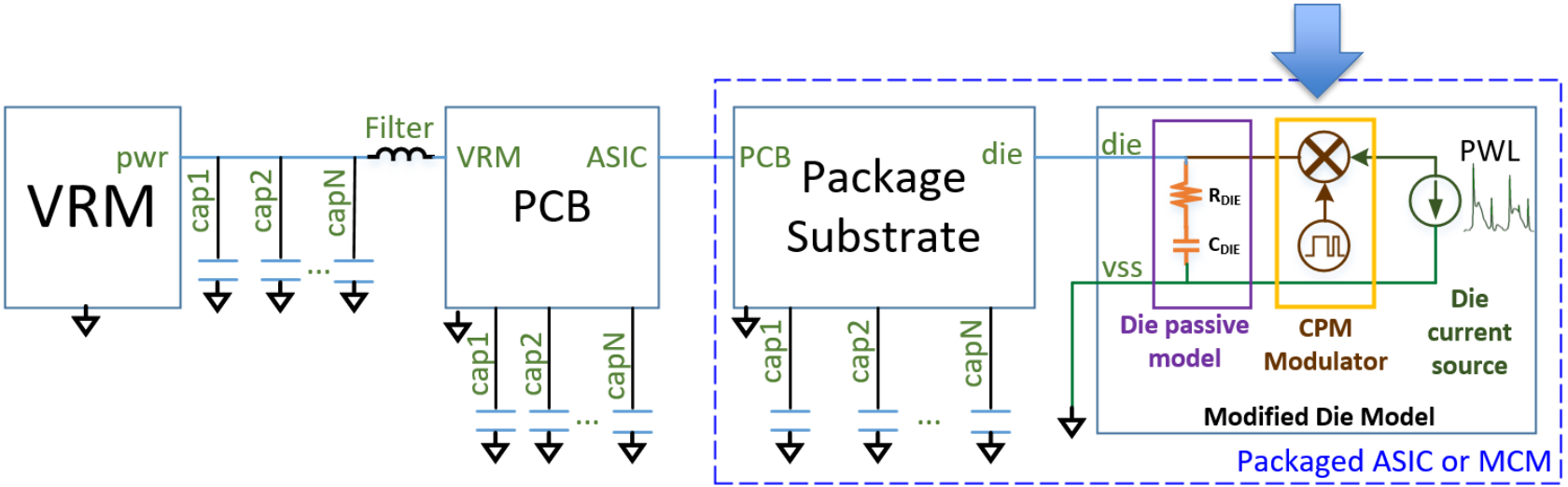
- **ASIC designs expect the IR drop from the bumps to the transistors not to exceed 7.5% of the on-chip voltage ripple threshold**
- **Time domain ripple without modulation on the Non-Optimized PDN shows**
  - **ΔV = 8.189 mV pk-pk**
- **Lower voltage ripple at ASIC die bumps provides more margin within the die design**





CPM Modulation

CPM Modulator added to PI System Model

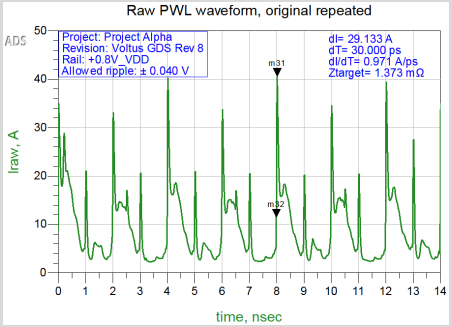


CPM Modulation provides a way to create the *Forced Response* on the System

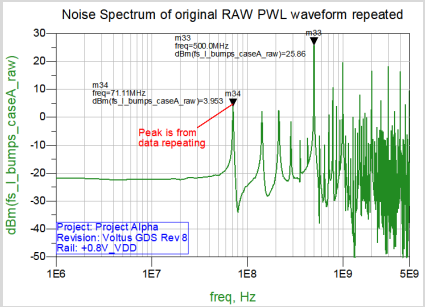
With modulation, it is possible to check for *Rouge Wave* conditions on the system PDN

CPM Modulation – Generating the Forced Response

Raw Project Alpha CPM current from Voltus



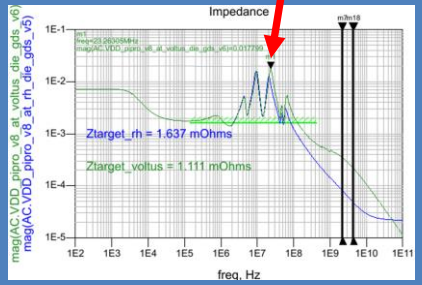
FFT of raw Project Alpha CPM Current from Voltus



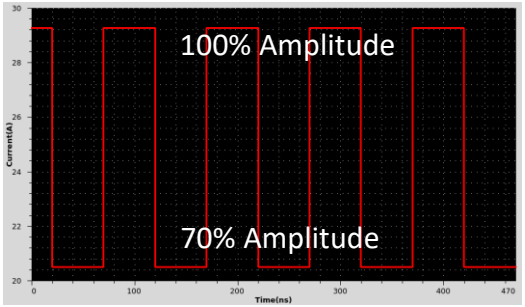
*CPM Current waveform has no low frequency content.

Entire frequency range of PDN is not covered by raw CPM current

System impedance model shows 20MHz impedance peaks

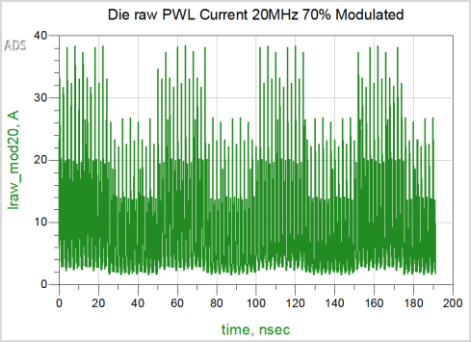


Modulation Current with 50ns period (20MHz)

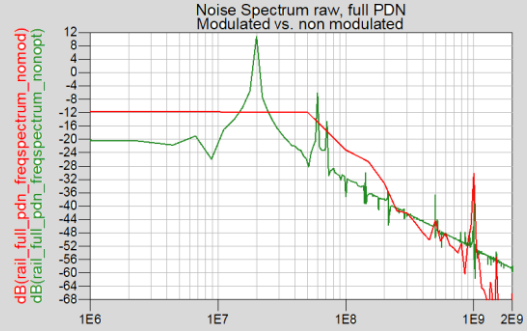


*Duty cycle =100% current for 25ns and 70% current for 25ns

Modulated CPM Current with 50ns period (20MHz)



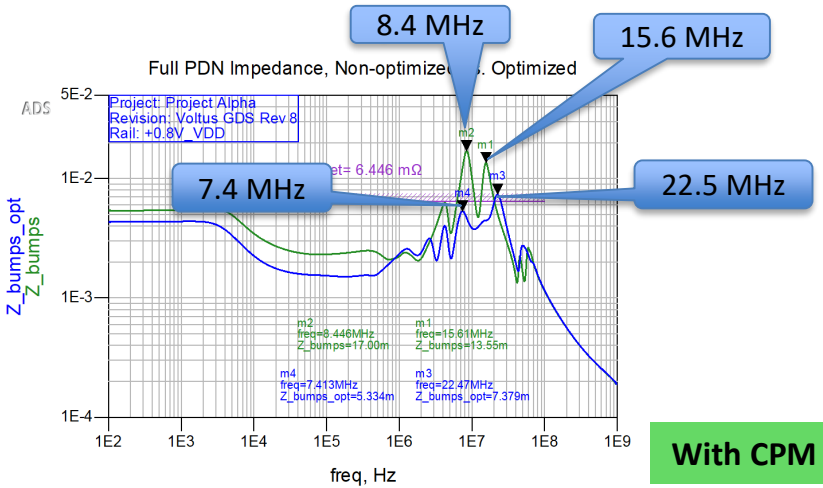
FFT of Modulated CPM Current with 50ns period (20MHz)

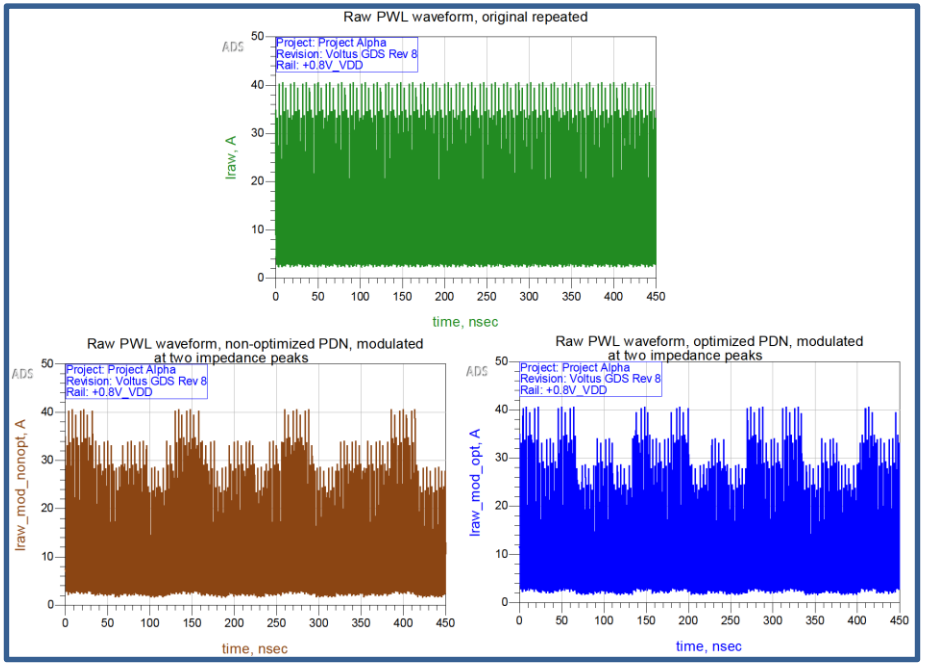


*New modulated CPM Current waveform now has low frequency content included

CPM Modulation Waveforms

- **Based on Non-optimized and optimized PDN, waveforms shown reflect simultaneous modulation at 2 impedance peaks.**
  - **Non-Optimized PDN modulation frequencies 15.6 MHz and 8.4 MHz**
  - **Optimized PDN modulation frequencies 22.5 MHz and 7.4 MHz**



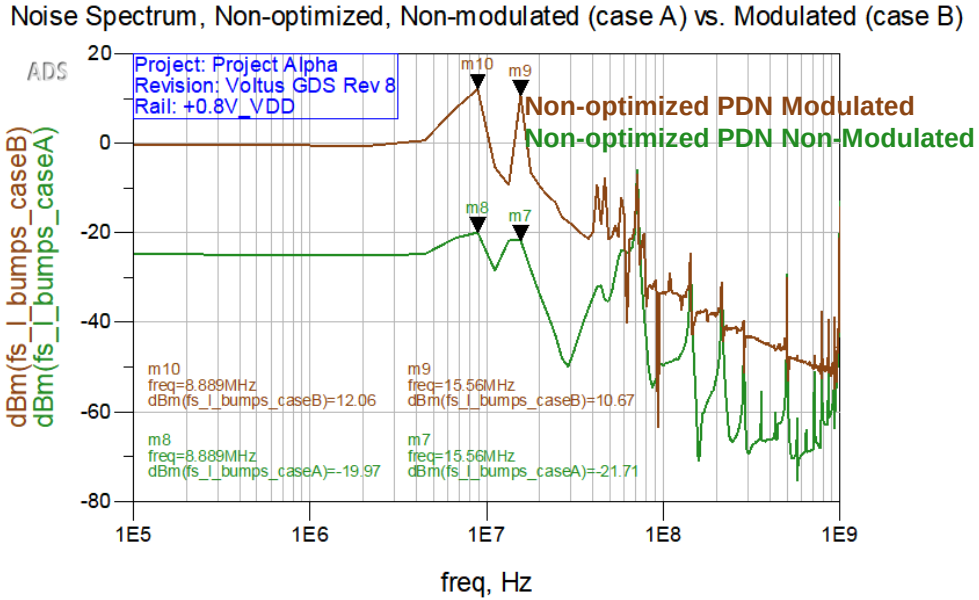


Non-optimized PDN Modulated PWL **Optimized PDN Modulated PWL**

With CPM modulation, it is possible to stimulate the PDN at more than 1 frequency

Noise Spectrum – Non-Optimized System PDN, Non-Modulated vs. Modulated

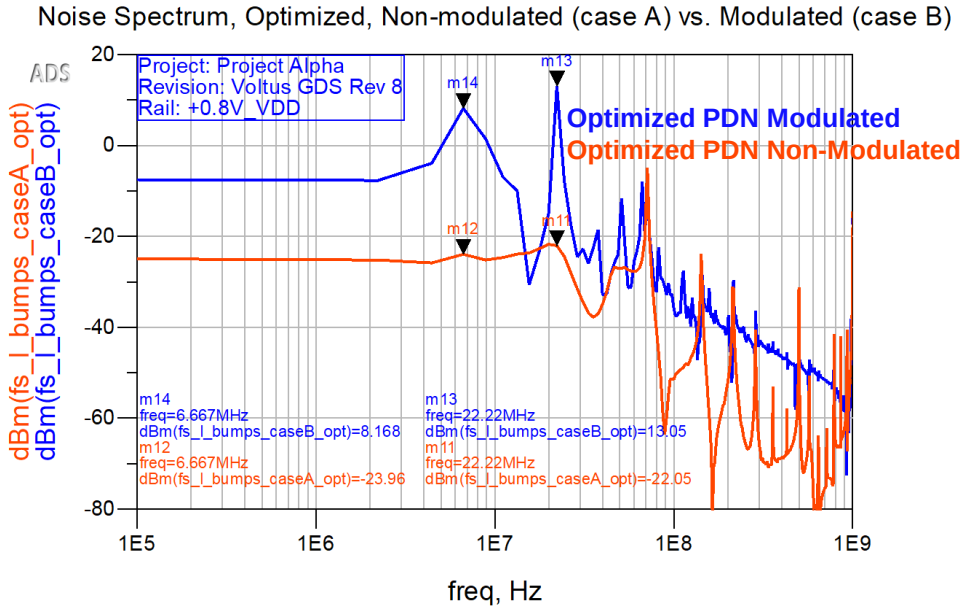
- **As shown on the Non-optimized PDN, with modulation a difference of**
  - *+32 dBm* @ 8.8 MHz vs. without modulation
  - *+31 dBm* @ 15.5 MHz vs. without modulation
- **Without modulation, it is not obvious if there is an impact on the PDN changes implemented**



Modulation of the Non-optimized PDN shows an increase of noise by 32 dBm

Noise Spectrum CPM Modulation vs. Non-Modulation

- **As shown on the optimized PDN, with modulation a difference of:**
  - *+32 dBm* @ 6.6 MHz vs. without modulation
  - *+35 dBm* @ 22.2 MHz vs. without modulation
- **Without modulation, it is not obvious if there is an impact on the PDN changes implemented**

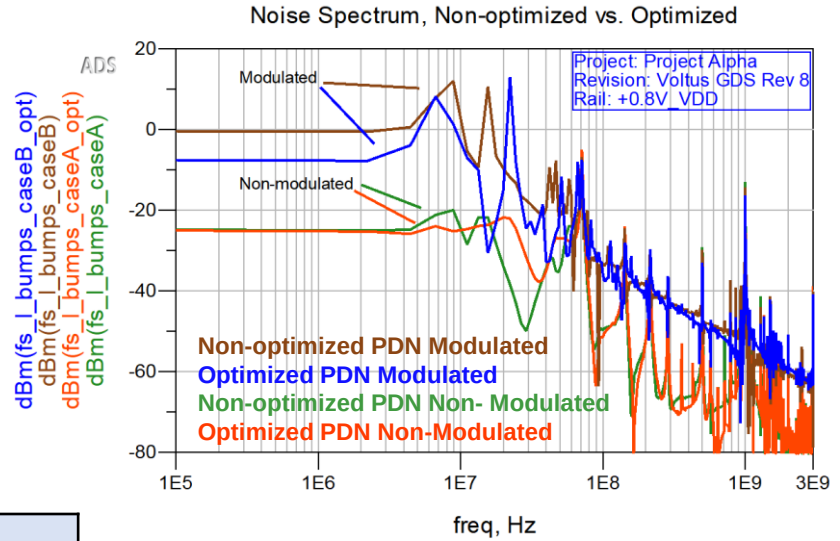


Modulation of the Optimized PDN shows an increase of noise by 35 dBm

Noise Spectrum – Optimized System PDN, Non-Modulated vs. Modulated

- **By creating the forced response in the system, this shows designers where modulating the CPM has a large impact on their design**

- **After optimizing the PDN and with modulation, it is easier to determine where the largest noise sources are to power integrity**



PDN Configuration	Peak Noise (dBm) Non-Optimized | Optimized	Noise Change
No Modulation	-20 | -24	-4 dB
84% Modulation at first impedance peak	+10.7 | +13	+2.3 dB
84% Modulation at second impedance peak	+12.1 | +8.1	-4 dB

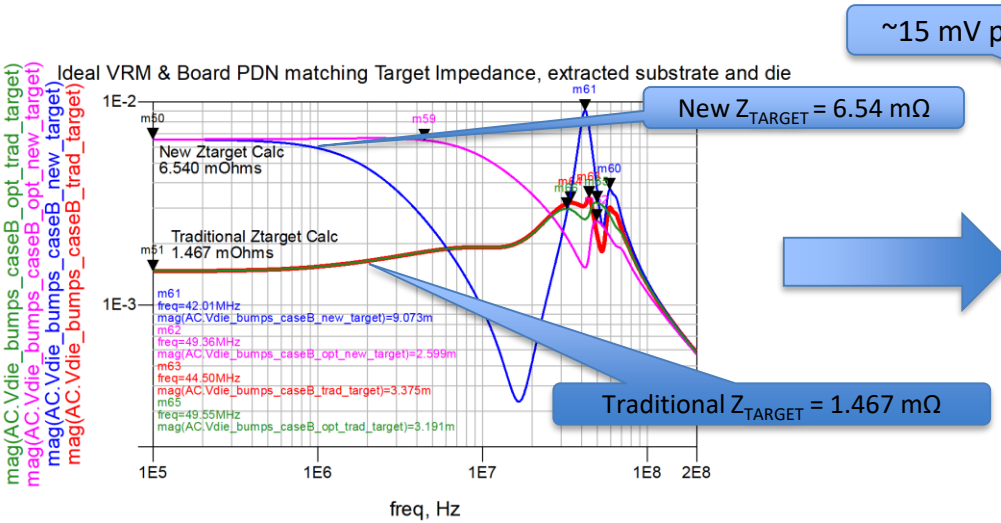
Without modulation, change was not as noticeable

Noise ***increased*** with modulation

Noise ***decreased*** with modulation

By optimizing the PDN, the noise *increased by 2.3 dB and reduced by 4 dB* at the modulation peaks in comparison to the non-optimized PDN, but overall noise is reduced

Matching Target Impedance and PDN Voltage Ripple

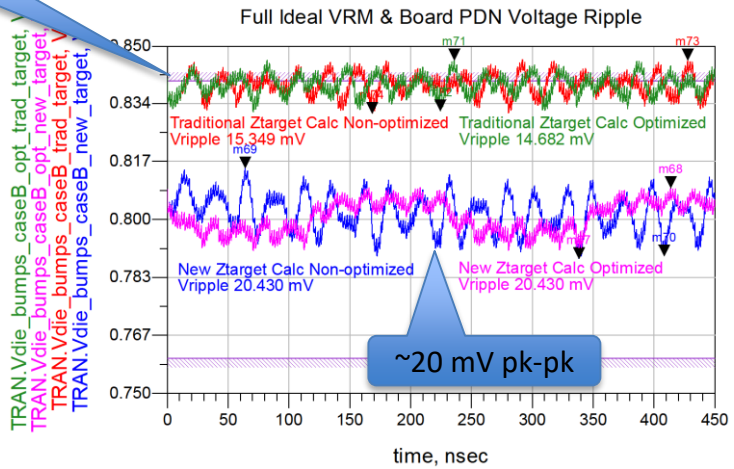


New Z_{TARGET} = 6.54 mΩ

Traditional Z_{TARGET} = 1.467 mΩ

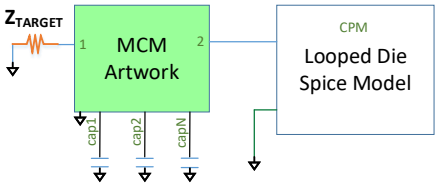
~15 mV pk-pk

Note: Voltage offset is intentional for better viewing



~20 mV pk-pk

Model Setup



Non-optimized PKG-DIE Modulated matched to 1.46 mOhm Z_{TARGET}
Optimized PKG-DIE Modulated matched to 1.46 mOhm Z_{TARGET}

Non-optimized PKG-DIE Modulated matched to 6.54 mOhm Z_{TARGET}
Optimized PKG-DIE Modulated matched to 6.54 mOhm Z_{TARGET}

The closer the PDN is to matching Z_{TARGET} , the lower overall voltage noise response

Determining Simulation Duration for Steady State Amplitude

- Each signal requires a minimum number of cycles to reach steady-state amplitudes [1]

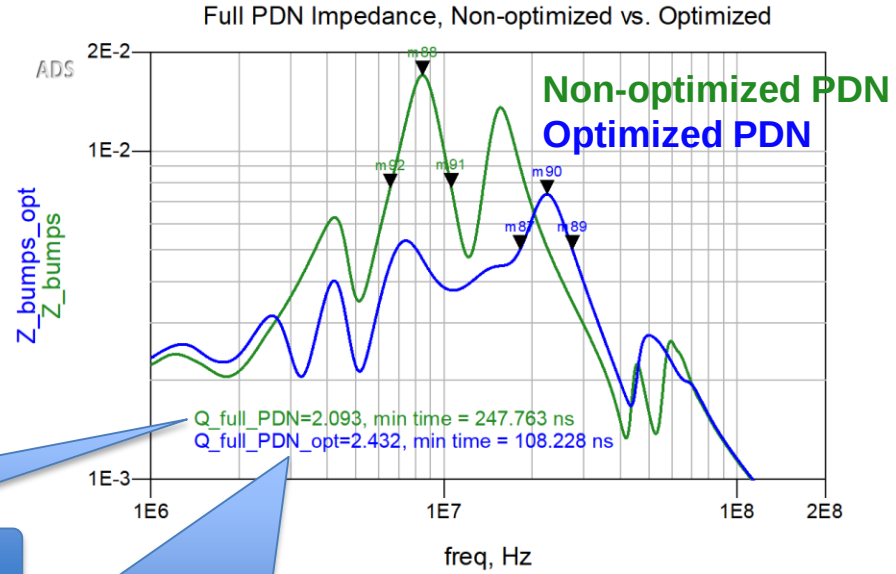
Q can be found in the PDN by:

$$Q = \frac{peak\ f_0}{Af_0 - Bf_0}$$

Where Af_0 and Bf_0 are the respective -3dB points

From Q the minimum cycles or simulation time required to achieve a steady state amplitude by:

$$minimum\ cycles = \frac{Q}{peak\ f_0}$$



Non-optimized PDN minimum simulation time for steady state ≈ **248 ns**

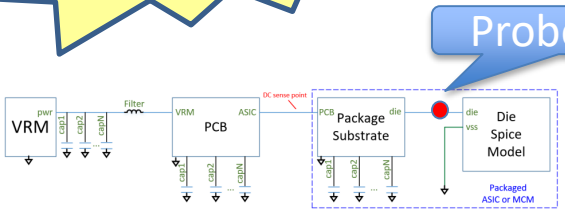
Optimized PDN minimum simulation time for steady state ≈ **108 ns**

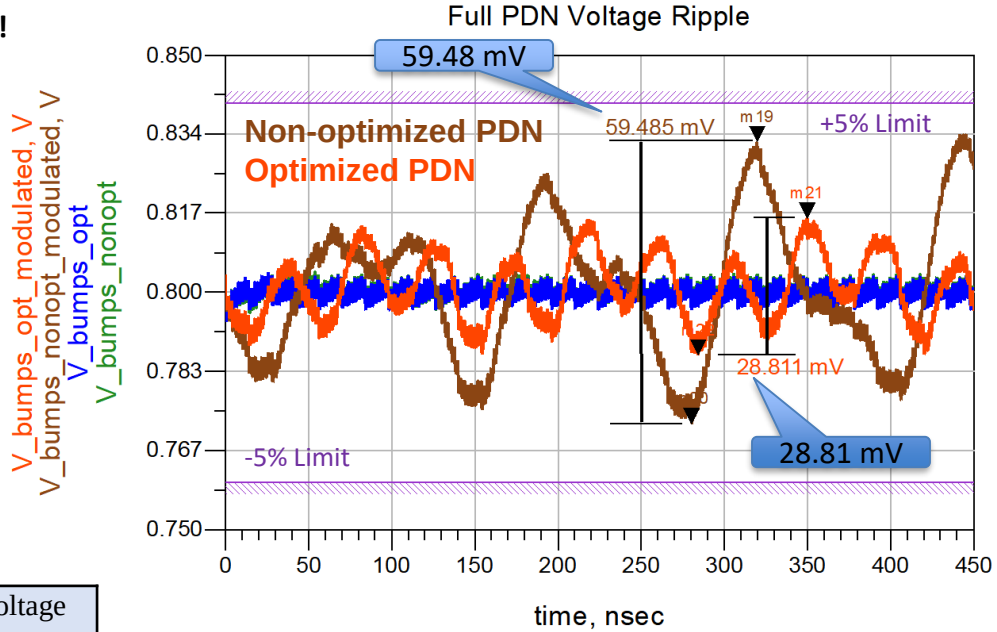
For the forced response to work, the simulation needs a minimum number of cycle to charge the PDN [1]

Full PDN Analysis – Time Domain Voltage Ripple

BOTH PDNs show the voltage ripple is less than the specification!

52% reduction in voltage ripple by optimization





CPM Load	Voltage Ripple Pk-Pk (mV) Non-Optimized PDN | Optimized PDN	Percent Voltage Change
No Modulation	5.4 | 5.4	-
Modulation	59.5 | 28.8	-52%

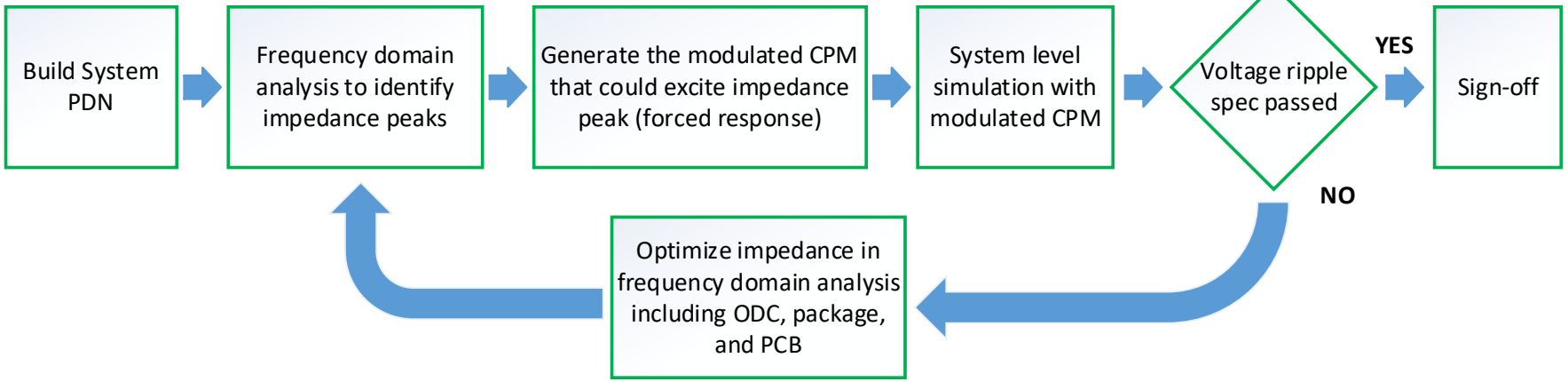
*Limits shown are based on (0.8V +/-40mV) +/-5% or 80mV pk-pk

*PDN Optimization only consists of changing capacitor values on PCB & on-substrate, removal of filter inductor and resistor

By optimizing the PDN, the ripple was ***reduced by 52%*** (from 59.5 mV to 28.8 mV)

Design Sign-Off with CPM Modulation

This methodology prevents both excessive over design and under design of the PDN

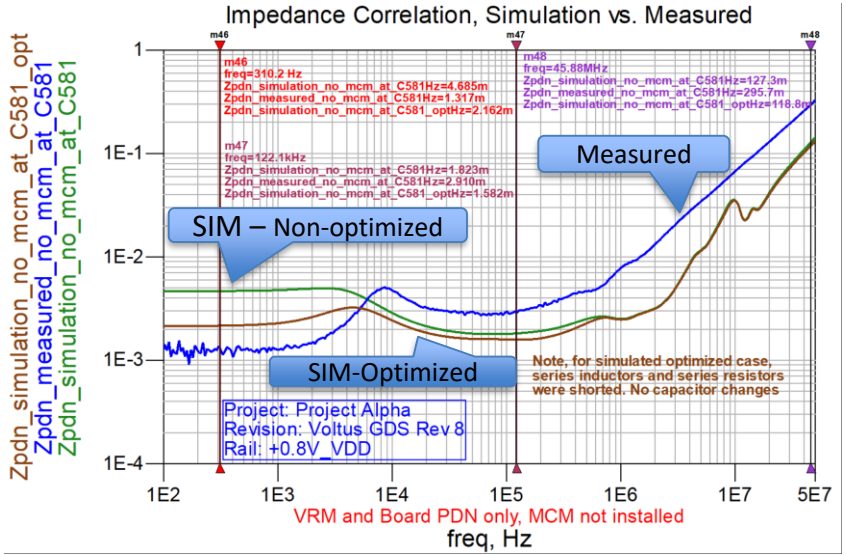


Initial analysis occurs in the frequency domain with PDN design → ***Design sign-off*** **occurs in the** ***time domain!***

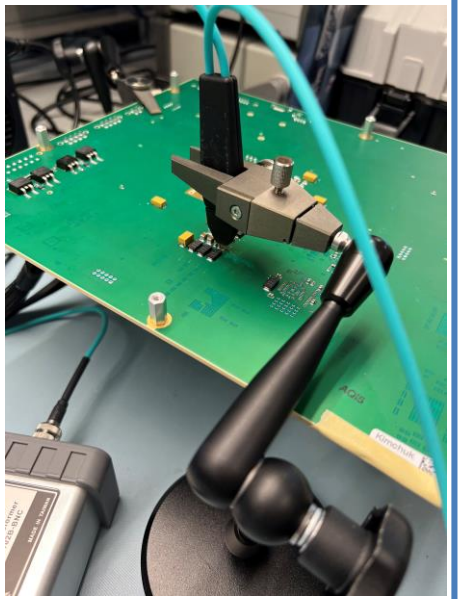
PDN Measurement of PCB

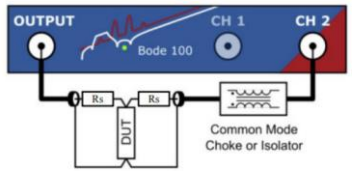
Room for improvement in measurement correlation could be addressed by:

- To more accurately depict the inductor DCR
- VRM model improvement
- Vendor capacitor model improvement
- PCB measurement indicates extractions are less resistive



PDN Configuration	Impedance @ 310.2 Hz	Impedance @ 122.1 kHz	Impedance @ 45.88 MHz	Peak Inductance @ 45.88 MHz
Measured PDN	1.31 mΩ	2.91 mΩ	295.7 mΩ	1.03 nH
Simulated PDN	4.68 mΩ	1.82 mΩ	127.3 mΩ	441.59 pH
Simulated PDN (shorted series inductors and resistor)	2.16 mΩ	1.58 mΩ	118.8 mΩ	412.11 pH





Source: Picotest.com

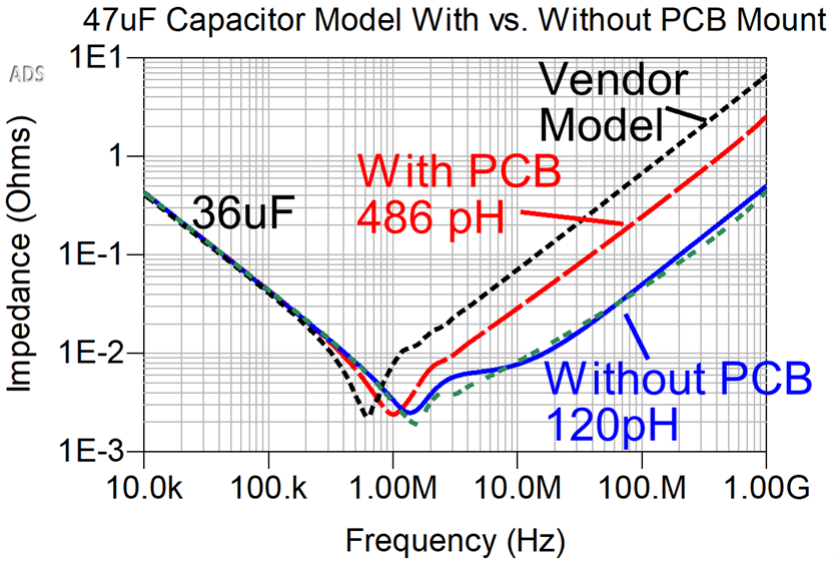
*Rs = 0Ω on P2102A-1X Probe

Measurement Setup

Next Steps

Next steps include:

- **Analysis of PDN with capacitor models that have mounting inductance removed to achieve better measurement correlation.**
- **Analysis using VRM state space average models**
- **Measurements in the time domain to validate the CPM models**



In this example, the measured capacitor has the same impedance as the vendor model at nearly 10x the frequency

Source: EDICon 2021 Partial Inductance – The secret to correlating simulation and measurement – S. Sandler, B. Dannan, & H. Barnes

Summary

- Demonstrated PI methodology with ASICs to achieve higher fidelity simulation using CPMs
- Discussed the importance of CPM modulation to generate a forced response as well as use to check for rogue wave conditions
- Showed how design sign-off can occur in time domain, after initial analysis in the frequency domain
- Discussed how target impedance analysis can be used with this method but does not correlate 100% to time domain simulation.

For Power Integrity Designs with ASICs….

Source: youtube.com

NORTHROP GRUMMAN

Thank you!

QUESTIONS?

Source: dilbert.com

References

1. Sandler, S., “Target Impedance Limitations and Rogue Wave Assessments on PDN” DesignCon 2015.
2. Sandler, S., Dannan, B., and Barnes, H., “Partial Inductance – The Secret to Correlating Simulation and Measurement”. EDICon 2021.