

Partial Inductance

the secret to correlating simulation and measurement

Session Presented By: Steve Sandler, Benjamin Dannan, and Heidi Barnes Date: August 25, 2021 Track: Technical Session

ED UNITARY STREET



Presenter Bios

Steve Sandler has been involved with power system engineering for more than 40 years. Steve is the founder and CEO of PICOTEST.com, a company specializing in instruments and accessories for high performance power system and distributed system testing. He frequently lectures and leads workshops internationally on the topics of Power Integrity and Distributed Power System Design. He is a Keysight Certified EDA expert.



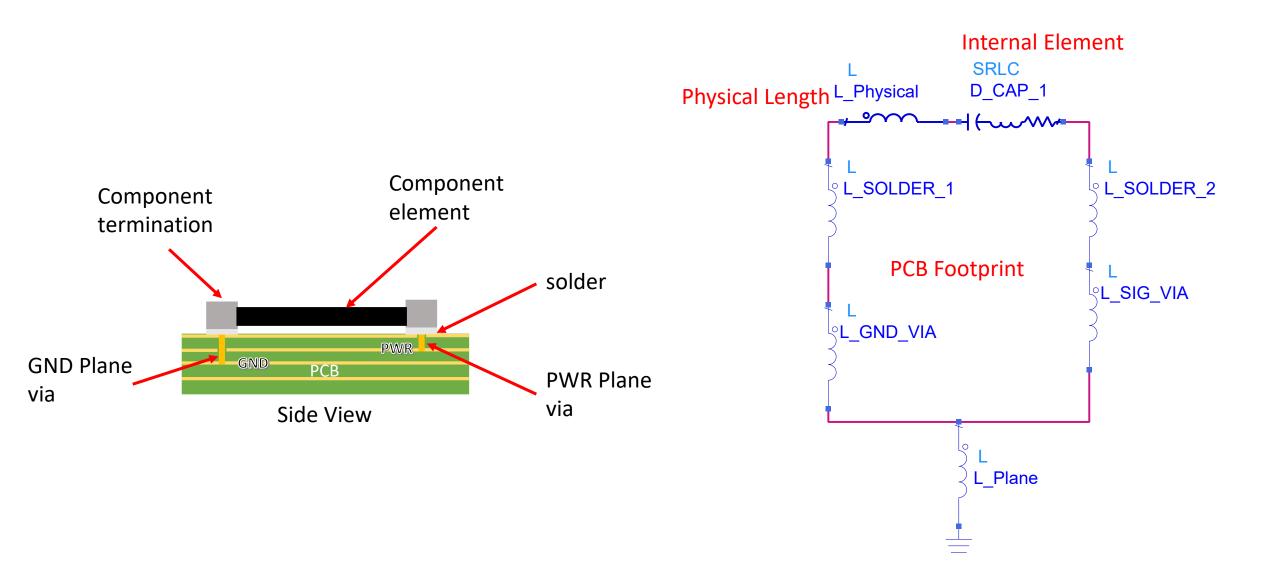
Benjamin Dannan is a Staff Digital Engineer at Northrop Grumman, with a multi-faceted background that includes a wide range of professional engineering and military experiences. He is a specialist in signal and power integrity design, and he received the prestigious DesignCon 2020 best paper award. Benjamin holds a certification in cybersecurity, has a BSEE from Purdue University, a Masters of Engineering in Electrical Engineering from The Pennsylvania State University. He is a Keysight Certified EDA expert.

Heidi Barnes is a Senior Application Engineer for High-Speed Digital applications in the EEsof EDA Group of Keysight Technologies. Her recent activities include the application of electromagnetic, transient, and channel simulators to solve signal and power integrity challenges. Author of over 20 papers on SI and PI and recipient of the DesignCon 2017 Engineer of the Year. Heidi graduated from the California Institute of Technology in 1986 with a bachelor's degree in electrical engineering. She has been with Keysight EEsof since 2012.



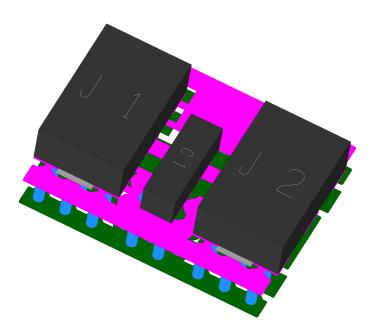
- Mounting Inductance Definition
- Simulating Mounting Inductance
- Measuring Mounting Inductance

Representation of Mounted Component

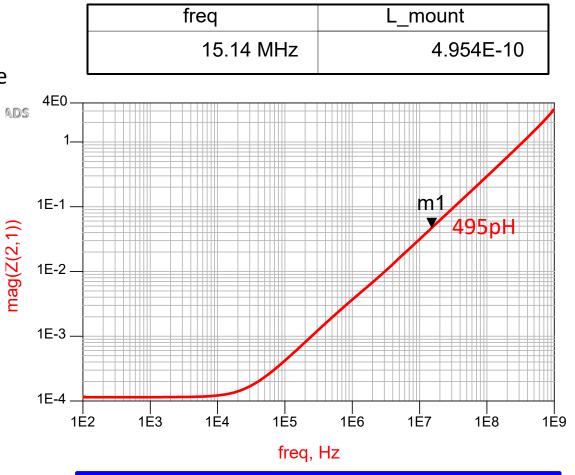




The ODB++ file from the PCB software is imported into Keysight Pathwave ADS and the PCB Pads are shorted together to measure the resistance and inductance of the PCB mount



Eqnnount=m1/(2*PI*indep(m1))



$$L_{flat} = 2 \times 10^{-4} \, \ell \big[\ln(\frac{2\ell}{w+t}) + 0.5 + 0.2235(\frac{w+t}{\ell}) \big]$$

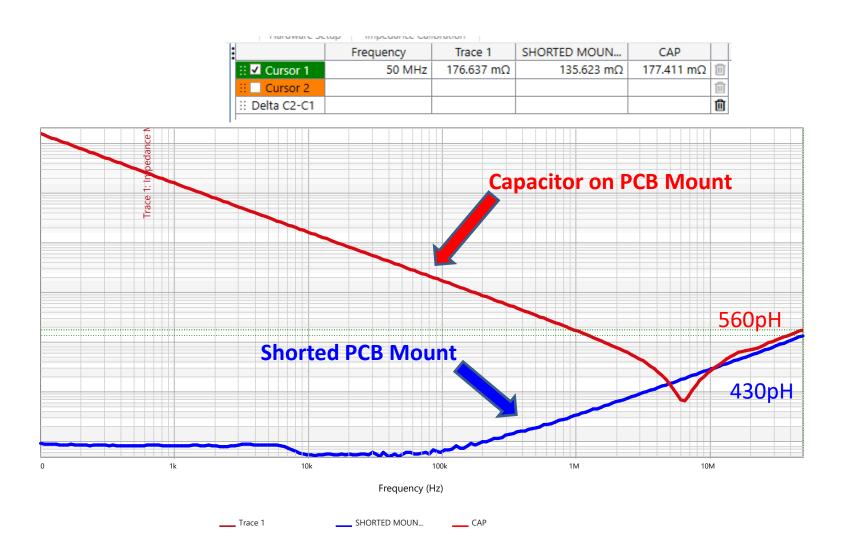
Constant Capacitor with and without mounting inductance

A measurement, performed without fixture removal results in a measurement very close to the simulated value of the PCB inductance.

Measuring the capacitor on the PCB results in 560pH. 130pH higher than the PCB mount.

So the capacitor, without the physical length of the mounting inductance is 130pH and the EM simulator includes the physical length inductance of the mount.

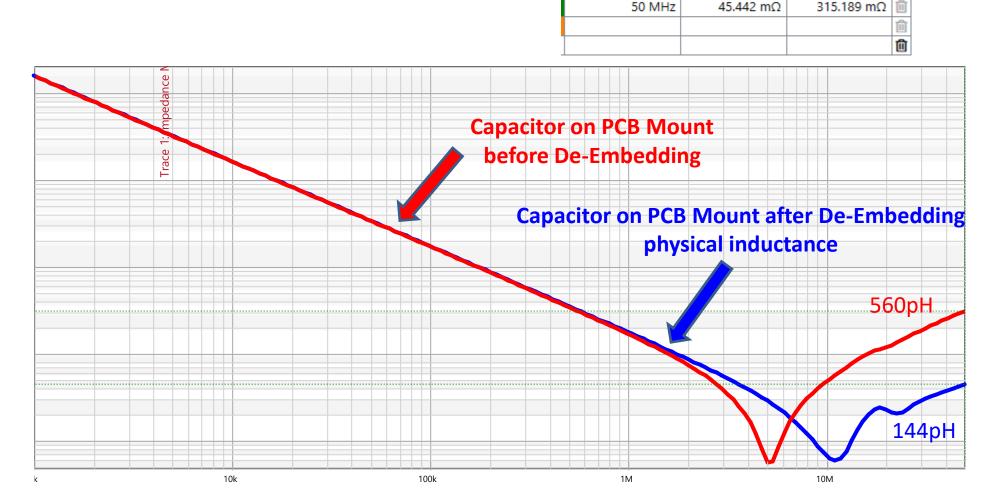
So the 130pH capacitor mounted on the PCB will simulate at 560pH.



EDN De-Embedding the Fixture

Performing the SHORT calibration on the PCB removes the physical inductance associated with the capacitor.

While the capacitor measures 560pH on the PCB, it measures only 144pH more than the shorted trace. The capacitive element is 144pH and the physical length of the capacitor with the mount is 416pH.



P2102A SOL C.,

Frequency

P2102A SOL C.,

Frequency (Hz)



GCJ21BR71E105MA12, L, DC0V, 25degC 1.45mm

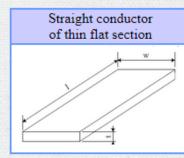
X In Production

Calculator of Straight Conductor

http://www.finetune.co.jp/~lyuka/technote/inductor/inductor-straight-flat.html

* X **Frequency Characteristic** 1nr ~400pH Inductance[H] ~340pH 100p 10p∟ 1M 10M 100M 1G 10G Frequency[Hz] 0.7mm × NRND GRM216R61E105KA12, L, DC0V, 25degC

Murata Vendor Data – 1uF, 25V capacitors



Conductor material:	Copper 🗸		
σ : conductance	58.5652	×10 ⁶ S/m	
k : thermal conductivity	398	W/m/K	
T : temperature	25	°C	
δ : skin depth	6.5766	μm	
f : frequency	100	MHz	
ℓ : wire length	2	mm	
w : wire width	1.2	mm	
t : wire thickness	1.5	mm	
<i>L_{flat}</i> : Inductance	0.4779	nH	
<i>R_{dc}</i> : DC resistance	0.0190	$m\Omega$	
heta : thermal resistance	2.7917	K/W	
C	alculate!		

 R_{dc} : valid for -50°C \leq temp \leq 150°C

Formulas used

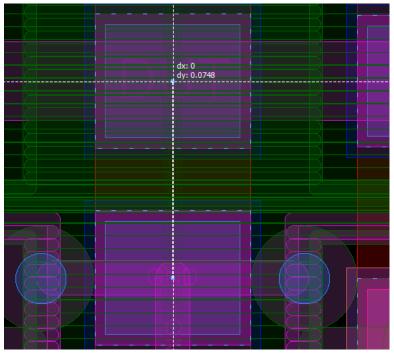
$$L_{flat} = 2 \times 10^{-4} \, \ell \left[\ln(\frac{2\ell}{w+t}) + 0.5 + 0.2235(\frac{w+t}{\ell}) \right] \, \left[\mu \mathrm{H} \right]$$

where

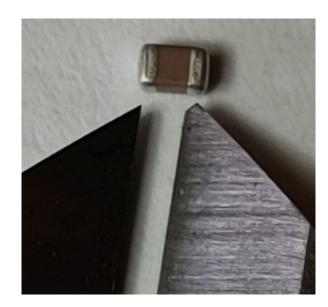
 L_{flat} : inductance of the conductor [µH] ℓ : length of the conductor [mm] w: width of the conductor [mm] t: thickness of the conductor [mm]



Our DUT is an AVX Cap P/N 08053C105JAT2A



PCB =0.749 in = 1.9 mm pad to pad



Cap = 1.6 mm pad to pad

Straight conductor of thin flat section

Conductor material:	Copper 🗸		
σ : conductance	58.5652	×10 ⁶ S/m	
k : thermal conductivity	398	W/m/K	
T : temperature	25	°C	
δ : skin depth	6.5766	μm	
f : frequency	100	MHz	
ℓ : wire length	1.6	mm	
w : wire width	1.27	mm	
t : wire thickness	1.3	mm	
<i>L_{flat}</i> : Inductance	0.3450	nH	
<i>R_{dc}</i> : DC resistance	0.0165	mΩ	
heta : thermal resistance	2.4349	K/W	
Са	Iculate!		

 R_{dc} : valid for -50°C \leq temp \leq 150°C

Formulas used

$$\begin{split} L_{flat} &= 2 \times 10^{-4} \, \ell \big[\ln(\frac{2\ell}{w+t}) + 0.5 + 0.2235(\frac{w+t}{\ell}) \big] \, [\mu \text{H}] \end{split}$$
 where
$$\begin{split} & L_{flat} : \text{inductance of the conductor } [\mu \text{H}] \\ & \ell : \text{length of the conductor } [mm] \\ & w : \text{width of the conductor } [mm] \\ & t : \text{thickness of the conductor } [mm] \end{split}$$

ED Vendor Capacitor ESL Data



Using the AVX proprietary simulation tool, the capacitor we are measuring is shown as 709pH at 50.39 MHz.

Clearly, AVX did not remove the fixture from their measurements. If this 709pH ESL was entered into the EM simulator, the simulator would add an additional 495pH for the PCB fixture would result in 1.2nH, more than double the correct answer.

Neither Murata or AVX include any description of how they measured their capacitor for inclusion in their simulator.

This is the reason we recommend you measure these capacitors yourself.

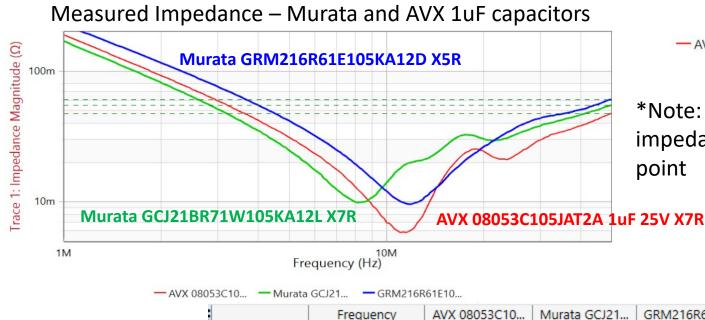
The ESL We Measured....

(H)

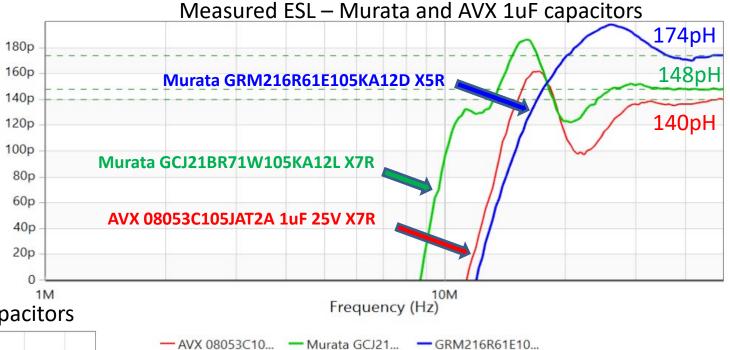
Frace 2: Impedance Ls

Comparing the measured data to the vendor data for the two Murata capacitors and the AVX capacitor we see a difference of:

- 252pH for the GCJ21BR71W105KA12L
- 166pH for the **GRM216R61E105KA12D**
- 569pH 08053C105JAT2A



Cursor 1



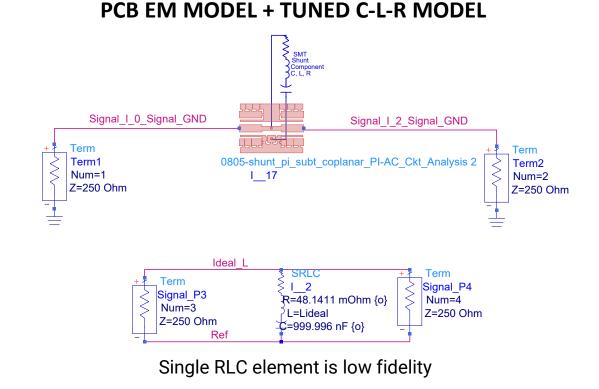
*Note: All of the Murata and AVX capacitors are 1uF, but impedance shows they do not have the same resonance point

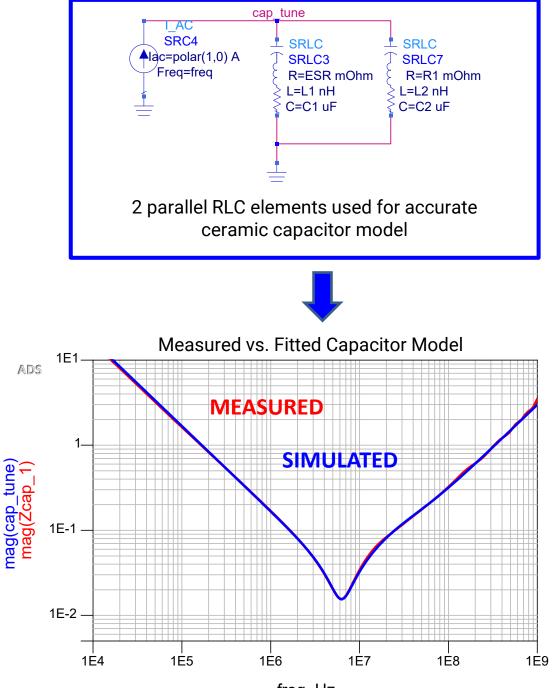
lency	AVX 08053C10	Murata GCJ21	GRM216R61E10	AVX 08053C10	Murata GCJ21	GRM216R61E10
50 MHz	47.166 mΩ	54.592 mΩ	60.597 mΩ	140.119 pH	148.087 pH	174.123 pH

ED Accounting for the Mount

How to Design for Power Integrity: Measuring, Modeling, Simulating Capacitors and Inductors

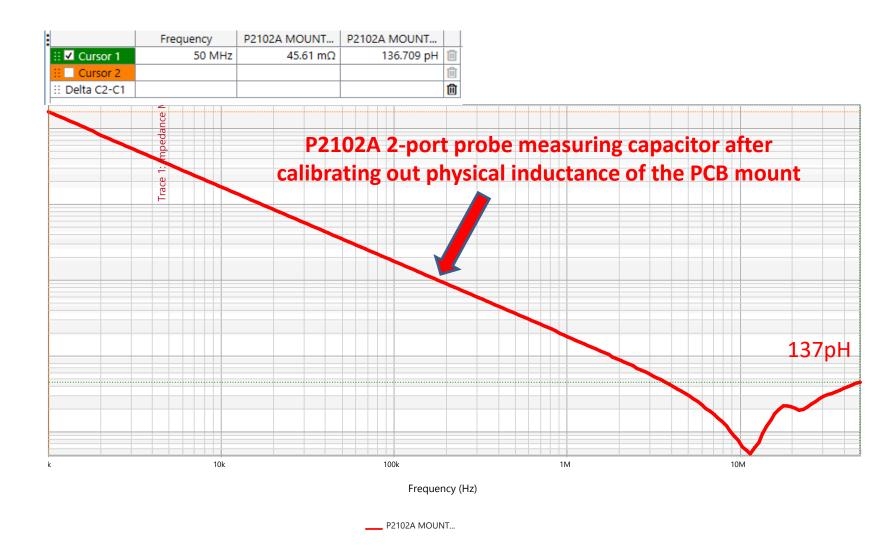
https://youtu.be/N4K3y4I4sKA





freq, Hz

CON Or Use a Probe for the Measurement

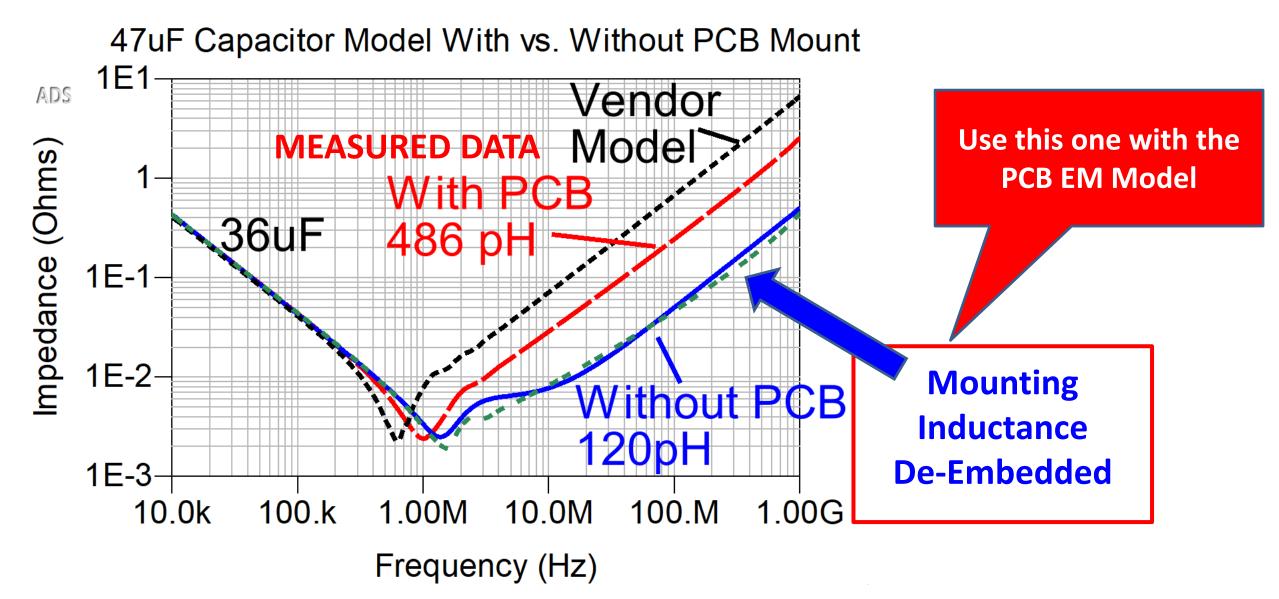


A 2-port probe provides 4 contacts on the capacitor termination pads. Using the 2port shunt through impedance and performing a fixture removal (SOL) calibration for the probe simplifies the process.

Use a shorted PCB mount, the same size as the capacitor for the calibration.

The P2102A 2-port probe provides a direct reading display of 137pH, very close to the 144pH we measured using the PCB de-embedding

47uF Vendor Data vs. Measured Model





Key Takeaways

- Accurate capacitor data can minimize the number of capacitors required, saving cost and valuable PCB area
- Measurement of the component is made up of 3 parts:
 - 1. Physical internal element
 - 2. External distance between the pads
 - 3. PCB Footprint- includes the pads and vias -
- The PCB mount must be removed for PCB simulation with EM models, otherwise it will be counted twice.
- Vendor is not always accurate; recommendation is to make your own measurements.

2 & 3 together are the PCB mount



Thank You for Attending

- S. Sandler, "How to Design for Power Integrity" Keysight sponsored YouTube Video Series: <u>http://www.keysight.com/find/how-to-videos-for-pi</u>
- Visit Picotest's Measurement Solutions page for more information -<u>https://www.picotest.com/measurements/index.html</u>
- Visit <u>www.picotest.com/blog</u> to see recent publications
- Join the Power Integrity for Distributed Systems LinkedIn Group
- Feel free to connect with us on LinkedIn