DesignCon 2022

DDR4-3200 FPGA Based System with Interposer Power-Aware SI Simulation to Measurement Correlation

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Abstract

DDR4-3200 Simultaneous Switching Output (SSO) channel modeling is further challenged to ensure data (DQ) compliance specification for an eye-opening at an ultra-low 1E-16 BER. With DDR4-3200 edge rates approaching <100 ps, power-aware SI simulation is necessary to achieve higher fidelity modeling. This paper intends to present methods for creating accurate power-aware signal integrity simulation through measurement correlation on the first DDR4-3200 FPGA memory controller, the Xilinx Versal, interfaced to a UDIMM with an interposer present during measurement.

This effort will combine simulation and measurement, which shows how to improve design margins during DDR4-3200 development cycles. Additionally, considerations and recommendations are provided for higher-speed DDR5 designs with more complex power distribution, channel topologies, and receiver architectures.

Author Biography

Benjamin Dannan is a Technical Fellow and an experienced Staff level Signal and Power Integrity (SI/PI) Design Engineer advancing high-performance ASIC and FPGA designs at Northrop Grumman. He is a Keysight ADS Certified Expert with expert level proficiency in high-speed simulation solutions, 3D EM solutions, and test and measurement solutions. He is a senior member of IEEE and an engineering professional. He has multiple years of experience designing, developing, and launching production products ranging from ASICs, radars, ground combat vehicles, pan-tilt-zoom (PTZ) camera video systems, fully autonomous robotic platforms, high-speed digital electronics, and other microelectronics solutions. Benjamin is a trained Electronic Warfare Officer in the USAF with deployments on the EC-130J Commando Solo in Afghanistan and Iraq, totaling 47 combat missions. In addition, Benjamin holds three patents in his name. Benjamin also has a certification in cybersecurity. He graduated from Purdue University with a BSEE and from The Pennsylvania State University with a Masters of Engineering in Electrical Engineering. In addition, he has co-authored multiple peer-reviewed journal publications. He has received the prestigious DesignCon 2020 best paper award, given to authors leading as practitioners in semiconductor and electronic design.

Randy White is the Memory Solutions Program Manager for Keysight Technologies. He is focused on test methodologies for emerging memory technologies in server, mobile, and embedded applications. Randy has spent the last 20 years investigating signal integrity measurement techniques, including de-embedding algorithms, measurement/model correlation, and high-speed measurements for real-time & sampling oscilloscopes as well as BERTs & AWGs. He has participated on many standards committees, including PCI-SIG, USB-IF, SATA-IO, JEDEC to help define new test methodologies. He is currently the chair of the JEDEC JC40.5 Logic Validation subcommittee. He graduated with a BSEE from Oregon State University.

Hermann Ruckerbauer, Owner of 'EKH - EyeKnowHow' has over twenty years of experience in high-speed measurement and simulation, especially on DRAM-related interfaces. EyeKnowHow is

serving the industry with consulting, simulation, measurements, and training for all kinds of high-speed serial interfaces. After receiving his Bachelor's Degree in Micro System Technology from the University of Applied Science in Regensburg he was doing design analysis and application testing for several memory generations at Siemens/Infineon. His latest activity before founding his own company was the definition of the DDR4 signaling standard within JEDEC for Qimonda. With the background of DRAM internal functionally, system application requirements, and high-speed signaling he is supporting any kind of high-speed interface implementations (e. g. for 10G Ethernet, PCIe, SATA, USB, ..) with a focus on memory standards. Holding many patents he was awarded in 2005 from Infineon in the category 'Outstanding Single Patent' for the patent on the “Temperature-dependent Self Refresh” in DDR Memory devices.

HeeSoo Lee is the DDR/SerDes product owner and an App Dev master scientist in the PathWave Software Solutions (PSS) group at Keysight Technologies. He has held several different positions since 1989 in Keysight/Agilent/Hewlett-Packard, including consulting business manager, technical marketing lead, and field applications engineer. Previously, he worked for Daeryung Ind. Inc. as an RF/MW circuit design engineer. He has over 30 years of design and simulation experience in RF, microwave, and high-speed digital designs. He graduated with a BSEE degree from the Hankuk Aviation University, South Korea.

I. INTRODUCTION AND BACKGROUND

The world is encountering the processing evolution as we have entered the era of Big Data. Yet this term "Big Data" is still an enigma to so many people. Big data in the cloud is one example that is a driving catalyst for this evolution which has fundamentally changed the way we do things. The U.S. military, for example, uses data in the cloud today to reduce injuries, and the National Basketball Association (NBA) monitors every player's movement on the floor during a game [1].

As a society, the amount of data we have consumed globally has consistently risen beyond expectations. Big data stats show that the creation, capturing, copying, and consumption of data went up by 5000% between 2010 and 2020. To be more precise, data usage increased from 1.2 trillion gigabytes to almost 60 trillion gigabytes [2]. By 2025, experts indicate that over 463 exabytes of data (463,000 petabytes) will be created each day, which is the equivalent of around 212,765,957 DVDs [3].

Figure 1 - Big Data Evolution [1]

Indeed, memory latency and bandwidth are limiting system performance. This is driven by the fact that machine and deep learning algorithms feed on data, and require sustained (streaming) memory bandwidth. The amount of unstructured data is growing such that memory access (latency) is becoming an issue as well. These challenges are commonly referred to as the "memory wall problem." This issue involves both the limited capacity and the bandwidth of memory transfer and entails different levels of memory data transfer. For example, data transfer between compute logic and on-chip memory, between computing logic and DRAM memory, or across different processors on different sockets. For all these cases, the capacity and the speed of data transfer have been significantly lagging behind hardware (HW) compute capabilities [4].

The computational cost of training recent state-of-the-art Transformer models in New Language Processing (NLP) has been scaling at a rate of 750x/2yrs, and the model parameter size has been scaling at 240x/2yrs. In contrast, the peak hardware floating-point operations per second (FLOPS) is scaling at a rate of 3.1x/2yrs, while both the DRAM and interconnect bandwidth have been increasingly falling behind, with a scaling rate of 1.4x/2yrs. To put these numbers into perspective, peak hardware FLOPS have increased by 90,000x over the past 20 years, while DRAM/Interconnect bandwidth has only scaled by a factor of 30x over the same time period [4]. The fact that memory bandwidth is not able to keep pace with the raw computing capabilities of today is the reason why a memory wall exists.

With the release of the JEDEC DDR5 standard in 2020, speeds of DDR5-4800 are being achieved with platforms such as Intel's Alder Lake [5]. That is a 50% increase from the max speed grade of 3200 MT/s available in the DDR4 standard. The question that Signal Integrity (SI) engineers need to ask themselves is if they are ready to model these solutions from a complete system perspective. Considering the significant bottleneck due to memory that continues to grow every year, along with the enormous data usage of our society today, this puts immense pressure on SI engineers to ensure that high-speed memory designs will work.

DDR4-3200 and DDR5-4800 edge rates are faster than 100 ps.This makes modeling high-speed parallel bus memory interfaces challenging for Signal Integrity engineers and even more challenging across multiple boards when only looking at SI models with injected jitter. More so, to ensure higher fidelity, modeling the power distribution network (PDN), as well as voltage regulator module (VRM), is critical to see the effects of SSO, as well as Simultaneous Switching Noise (SSN) contributing noise in a DDR4 system. By including these other components in the system model, a power-aware SI simulation is possible.

The many questions to consider are: How accurate are power-aware SI simulation models to the measurement for DDR4-3200 on one of the first DDR4-3200 FPGA memory controllers? How do we account for the measurement probe loading model in simulation, and how does crosstalk impact DDR4-3200? How do we model this effectively and correlate a power-aware SI model to measurement?

This effort intends to use one of the first DDR4-3200 FPGA memory controllers, the Xilinx Versal, interfaced to a UDIMM, to show a method to correlate signal integrity simulations to measurement accurately. Using correlated models is critical to ensure voltage and timing specifications are met for design sign-off with DDR4 designs today and DDR5 designs in the near future.

In addition to end-to-end system-level analysis, all design parameters will be validated through direct measurements. With these measurements, a model correlation process will be shared to highlight best practices.

Extending these findings to DDR5 will help with better understanding the complex nature of a memory channel and corresponding PDN. DDR4 and DDR5 standards define input and output signal performance at the device level but do not include channel-specific requirements. Thus, it is critical to fully assess system performance across a range of worst-case operating conditions. These conditions include single vs. multi-rank, varying ODT values, package parasitics, and crosstalk. This research effort will combine power-aware SI simulation, using Keysight ADS and measurement from Rohde & Schwarz test equipment, with DDR4 interposers from EyeKnowHow, to show how to improve design margins during DDR4-3200 development cycles.

II. STATEMENT OF THE PROBLEM

For traditional DDR memory designs, SI engineers had to consider reflections, crosstalk, ISI, SSO noise, system configuration, timing requirements, and topology in their workflows. Power integrity and signal

integrity workflows were typically separate design flows. The challenge with that paradigm is the power supply noise and SSN are not included in the majority of SI simulations unless designers injected random jitter into their simulation model. However, due to the speed necessary in today's design cycles, the amount of random jitter to inject into a simulation model is not always based on a measurement. Typically it is based on a previous design rule of thumb, which means it's likely not accurate. As memory systems continually move to higher speeds, this makes signal integrity signoff for parallel bus interfaces more challenging than ever. So, how does an SI engineer today know where the target is for "good enough" modeling? In other words, how do designers know where the boundary is between overdesign and missing critical design parameters?

Effectively, SSN has the effect of changing the potential between the DDR 1.2V power and the ground plane. It may also manifest itself as droop on the power rail, caused by multiple sinks switching at the same time and drawing more power than the PDN can instantaneously deliver. Simultaneous switching output noise in single-ended signaling is one of the major performance limiters as data rate scales higher [6]. Accurately modeling the effects of SSN is not inherently simple. The challenge is the power supply noise and SSN are not included in the majority of SI simulations. Today's SI engineers need to be able to do both SI and PI when it comes to modeling DDR interfaces. As a result, designing with DDR interfaces becomes more challenging than ever before, and the standard signal integrity analysis workflow is no longer good enough [7].

To accurately model the latest generation DDR4 and next-generation DDR5 solutions, simulations need to include SSN, and therefore power-aware SI simulation modeling is necessary. Otherwise, measurement of high-speed DDR4/DDR5 memory interfaces needs to include simulations to help mitigate uncertainty, as well as improve design margins during DDR4/DDR5 development cycles.

III. BACKGROUND ON INTERPOSERS

To correlate a DDR4 simulation model to measurement, interposers need to be included on the memory module. Interposers are used to allow probe measurement as close as possible to the memory component BGA ball. A depiction of how the EyeKnowHow (EKH) interposer is used in a DDR measurement application to allow an oscilloscope to measure close to the DRAM BGA ball accurately is provided in Figure 2.

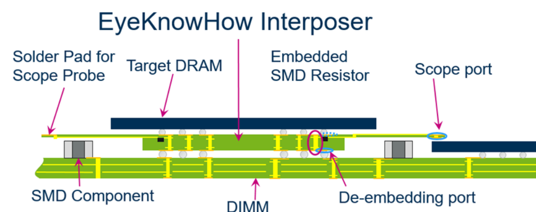


Figure 2 - Depiction of DIMM with Interposer Probe Locations [7]

To validate the device performance only, the interposer should be de-embedded from the measurement result. De-embedding is difficult if one looks into the details. Vector network analyzer (VNA) measurements require a setup where the interposer pads can be contacted. For complete interposer

de-embedding, 3-port and 6-port models are required for single-ended and differential signals respectively. It is important to note that each oscilloscope vendor has its own ways to implement the de-embedding process.

A 2-port model is used in a simulation where the test equipment response is included. This could include both interposer and probe loading or just the interposer. There are different ways to set up simulations for 2-port models of the interposer. In the simulation, the model can de-embed just the stub and leave the full via. This means part of the interposer via is still part of the measurement. If a 2-port de-embedded model is set up from the bottom pad (UDIMM PCB side) to the test pad, the reflection from the DRAM will not be correctly considered at the bottom pad since the via is only partly de-embedded. This means that 2-port models can never be correct, independent of their setup. For higher fidelity, it is best to use a 3-port model (or 6 for differential) to de-embed the interposer. However, there will always be some reflections that are part of the measurements even after de-embedding the interposer [8].

The next source of error is the embedded resistor on the interposer. Depending on probe type, as well as the defined input impedance, probe head resistors may need to be replaced with a different resistor value to maintain the required probe input impedance. Sounds simple, but then the designer also needs a modified probe model for de-embedding. The interposer with its resistor could be seen as an extension of the probe head. So ideally, the probe/interposer de-embedding should be done in one process, and the interposer resistor would be part of the probe heads resistor.

Therefore, with an interposer, designers can make measurements as close as possible to the DRAM ball. This method requires special attention to probe modeling which, if not accounted for, may cause errors in the final results.

Lastly, one should consider the DRAM specifications and where the actual test point is defined at the device ball. At the ball, reflections from the package may be seen. However, the DRAM receiver detects and latches the signal at the die. This implies that signal integrity measurements (verification) can be different from where specification conformance is defined (compliance).

IV. DDR4-3200 SIMULATION MODEL SETUP

Below, Figure 3 provides a depiction of the Xilinx VCK190 platform with a UDIMM attached to the DIMM slot.

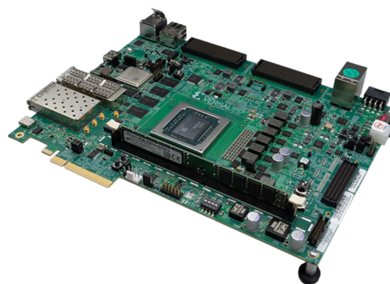


Figure 3 - Test Platform Xilinx VCK190 [9]

In addition, Figure 4 provides a depiction of the system simulation model, built using Keysight PathWave ADS Memory Designer, that represents a complete power-aware SI model across 8 DDR4-3200 byte-lanes on the VCK190 with an R/C A2 UDIMM from Micron. The PDN of this model includes the VRM, VCK190 PDN, Versal Package model, and UDIMM PDN. This is contained in the pre-layout block on the far right side of Figure 4, which contains all of the PDN for the VCK190 and the R/C A2 UDIMM.

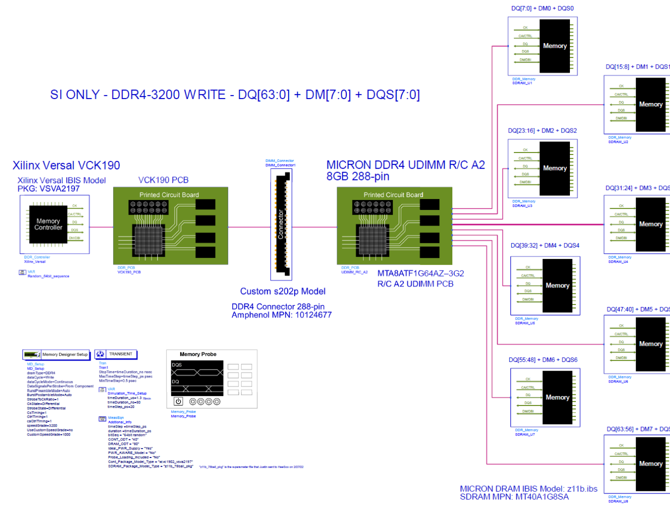


Figure 4 - DDR4-3200 SI Only Model with VCK190 and R/C A2 UDIMM

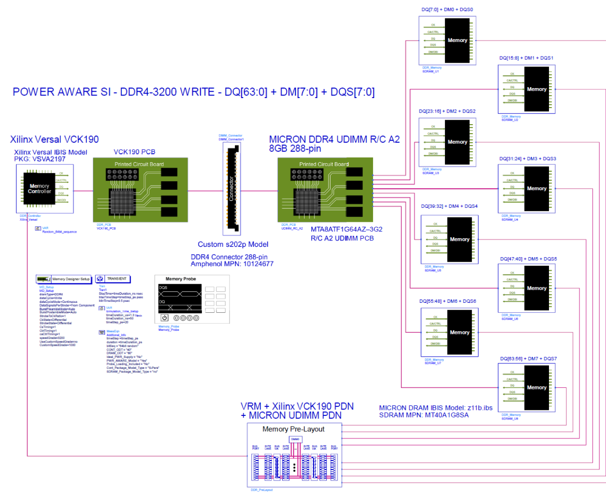


Figure 5 - DDR4-3200 Power-Aware SI Model with VCK190 and R/C A2 UDIMM

A. VCK190 VRM MODEL

To build an accurate representation of the PDN, it is vital to start with a proper model of the VRM. An ideal voltage source should never be attached to a port of an extracted PCB S-parameter model because it shorts out a significant portion of the PDN with zero impedance [10]. Therefore, to accurately model the VRM on the VCK190 for the DDR4 1.2V bus, an Infineon PS5401 evaluation board was measured under load using a 2-port probe. The resulting fitted spice model was compared to the measured model, which is

represented in Figure 7. The VRM measurement was captured under load, which is not shown in the setup (Figure 6).

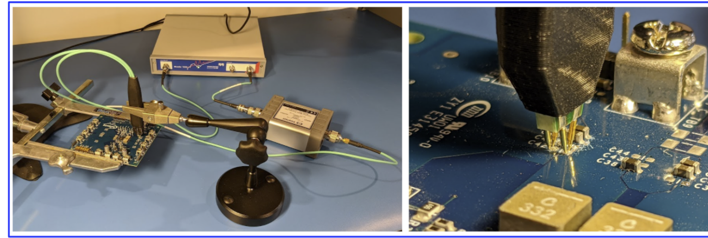


Figure 6 - VRM Measurement Setup with Bode 100 and Picotest P2102A

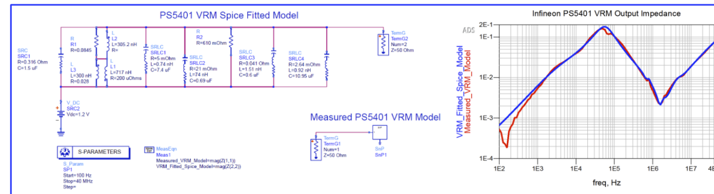


Figure 7 - ADS Schematic and Results for Infineon PS5401 VRM Measured vs. Fitted Spice Model

B. VCK190 AND UDIMM PDN MODEL EXTRACTIONS

The VCK190 PDN and the R/C A2 UDIMM PDN were both extracted using Keysight PIPro. Spice models for each capacitor model were used from Murata. There are a total of 26 VDD pins on the UDIMM connector. Therefore, to ensure the accuracy of spreading inductance in the system simulation model, 26 pins were used on the Amphenol connector S-parameter models. However, the ground return path of the UDIMM connector is not yet considered in this current model.

For Power-Aware SI simulations, all VDD pins on SDRAM are grouped or lumped into a single node. Whereas on the Versal VSVA2197 package, there are three VCCO IO banks used where each bank has 3 VDD pins, for a total of 12 pins. Xilinx provides, as part of their PDN kit, a package-die model for each bank. In this case, the 3 VDD pins for each bank (700, 701, and 702) are lumped into a single node. The Versal has only 3 Vdd pins connecting to each of the three respective VCCO XPIO banks. In addition, all of the SDRAMs and Versal IBIS models use an ideal ground. The VDD pins are only connected to the respective Versal VCCO bank in the IBIS model. This is depicted by the pins shown in Figure 9 below. In the future, an additional analysis could be done to explore the effects of including the resistive losses when not using an ideal ground return in the PDN.

The Versal IBIS model includes lumped RLC package models for the supported packages for SI simulations. Xilinx provides distributed IO package models for the Versal to allow greater simulation fidelity. The VCK190 uses a Versal with the VSVA2197 package, where the impedance for that VCCO bank package-die die model can be referenced by Figure 8. As shown by Figure 8, each Versal VCCO bank has an on-die capacitance of 17.6 nF. When looking at the byte lane distribution across these three

VCCO banks, it was observed that there are a maximum of four-byte lanes on bank 700. From this, a capacitance of 440 pF per DQ available can be calculated. When referencing the Micron IBIS Model Quality Report for the Z11B, it is reported that there is 304.4 pF per DQ available. This provides a good comparison to determine a reasonable amount of on-die decoupling capacitance is available per DQ on the Xilinx Versal.

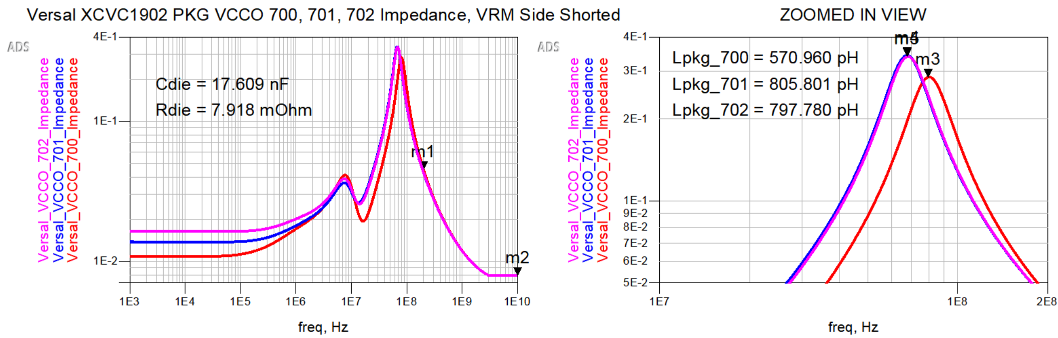


Figure 8 - Versal XCVC1902 VCCO XPIO Package and Die Impedance

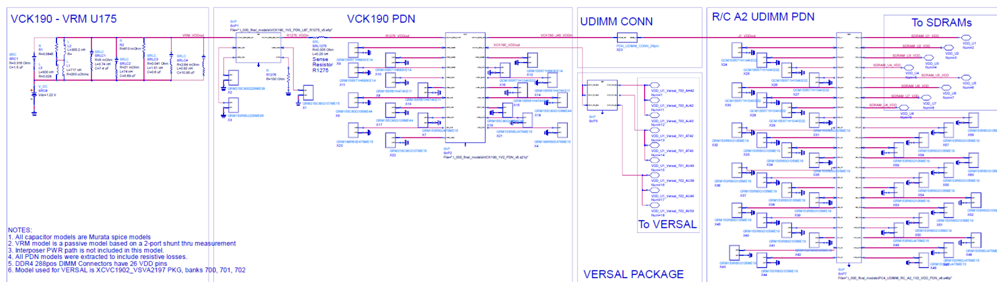


Figure 9 - System PDN Model for VCK190 and UDIMM

For reference, Figure 10 depicts the system PDN looking from the Versal die side of the package, as shown in Figure 9. In the PDN, there are three impedance peaks below 100mΩ inside 100MHz, that are observed. The maximum impedance peak occurs at 85 mΩ at 11 kHz. With reference to Figure 7, this 85 mΩ impedance peak in the PDN can be traced to the VRM as the root cause.

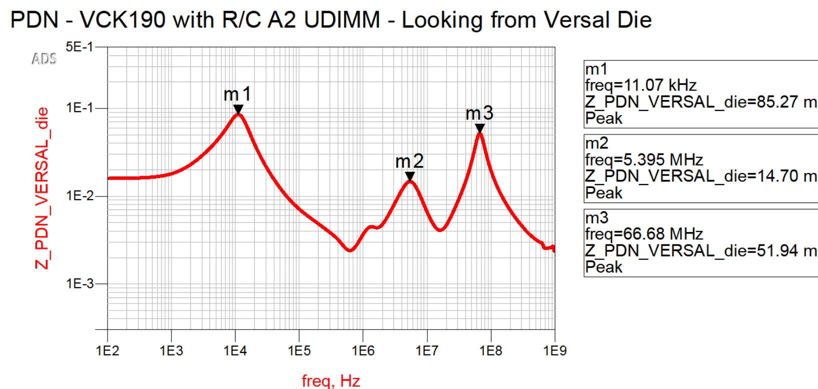


Figure 10 - System PDN Impedance from VERSAL - includes VRM, VCK190 PDN, UDIMM R/C A2 UDIMM PDN

V. VCK190 AND UDIMM PCB EM EXTRACTIONS

To build a power-aware SI model, electromagnetic (EM) extraction models are necessary for both the SI and PI components. SIPro was used to create the models for the SI components, which included EM extractions of all 8-byte lanes on the VCK190 PCB and the R/C A2 UDIMM PCB. Keysight PathWave SIPro is a hybrid solution with a method of moments (MOM) and finite element method (FEM) solutions. PIPro was used to create the models for the PI components, which included EM extractions of the PDN for the VCK190 PCB and the R/C A2 UDIMM. Keysight PathWave PIPro is a full 3D FEM solution. The PCB stack-ups used can be referenced in Figure 11. All EM extractions from the VCK190 PCB and the R/C A2 UDIMM were checked for causality and passivity violations. All models used were fully passive, and only some models had minor causality violations.

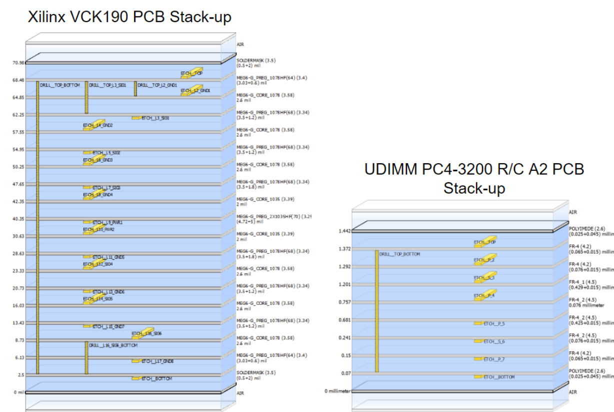


Figure 11 - Depiction of VCK190 PCB and R/C A2 UDIMM PCB Stack-ups

A. VCK190 UDIMM CONNECTOR SETUP

Since Amphenol only provides 12-port Signal-Ground and 24-port Signal-Signal touchstone models, a custom model needs to be compiled for all signals in the eight bytes lanes. This model is shown below in Figure 12. The limitation with this vendor model is that the crosstalk is limited due to the 12-port model. In other words, DQ5 will not see crosstalk at the UDIMM connector from DQ6. The alternative would be to request the vendor extract all signal nets together in a full 3D FEM solution, which leads to a 176-port model for eight-byte lanes or a 202-port model for 9-byte lanes with the clock included. Another option would be to mirror the model to allow crosstalk from both sides to the victim DQ signals. However, the crosstalk of the furthest signal pins is already marginally negligible. So the best solution is to use an S-parameter model that allows simulation of the crosstalk from the furthest pin.

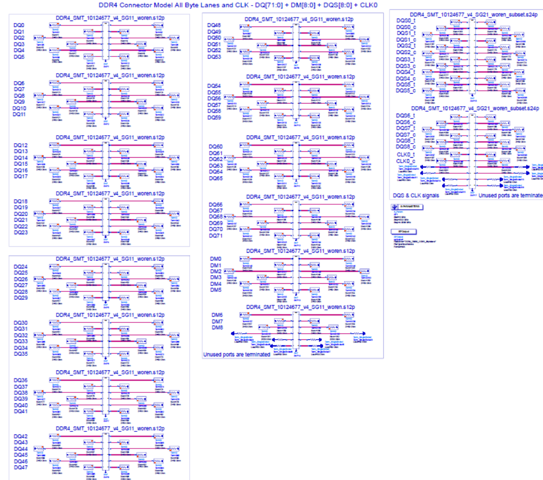


Figure 12 - ADS S-Parameter Model for 9-Byte Lane DDR4 UDIMM Connector

VI. DDR4-3200 MEASUREMENT SETUP WITH INTERPOSER

To make proper measurements with the R&S RTP164 oscilloscope, the RT-ZMA14 probe tips will be mounted onto the interposer. The RT-ZMA14 probe tips use resistors with a default value of 332Ω. As depicted by Figure 13, to ensure a proper impedance match, the ZMA14 will need to be modified with a 232Ω resistor, which in series with the 100Ω embedded resistor on the interposer, provides a 332Ω to match the scope. The RT-ZM160 probe was designed with an input resistance of 332Ω total for matching purposes (e.g., gain control), so the combination of the 100Ω embedded (series tap) resistor on the interposer and the modified probe tip 232Ω series resistor sums to the expected 332Ω value.

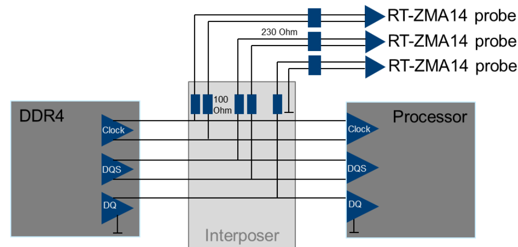


Figure 13 - Principal Test Setup with RT-ZMA14 and Interposer [11]

A depiction of these resistors that need to be modified is shown in Figure 14.

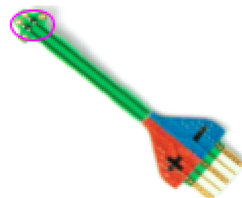


Figure 14 - R&S RT-ZMA14 Probe Tip Resistors [12]

A modified probe tip also requires a customized de-embedding file provided by Rohde & Schwarz R&D, which is named “RT-ZMA14_232R_interposer.s4p”. The method to correctly set up the de-embedding with this file for both differential and single-ended signals is shown in Figures 15 and 16.

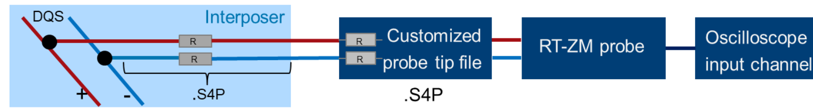


Figure 15 - De-embedding Differential Signals with RTP Oscilloscopes [11]

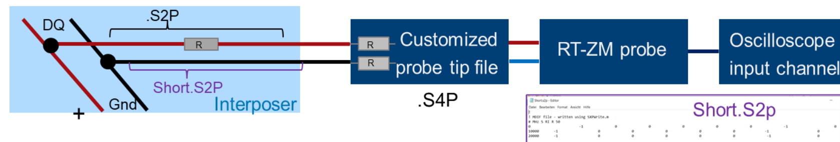


Figure 16 - De-embedding Single-Ended (SE) Signals with RTP Oscilloscopes [11]

The DQ49 data signal was measured on a UDIMM that was modified with an EKH interposer, which is inserted into the DIMM slot on the VCK190 platform. These measurements were captured by de-embedding the 2-port interposer model and the custom RT-ZMA14 probe model.

Figure 17 provides a depiction of the DQ49 (DQ1 on the interposer) probe location that will be used on the interposer to attach the RT-ZMA14 probe tip. It is important to note the RT-ZMA14 is a solder-in solution. Any solder-in solution is preferred over the handheld browser, especially for tests over a long period where different test patterns could be run. When using the RT-ZMA14, the single-ended DQ nets are connected such that single return connects to the blue minus marked

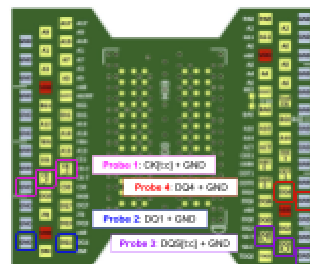


Figure 17 - Depiction of Probe Measurement Locations on EKH DDR4 x8 Interposer: Ballout for Single Die and Stacked Package [7]

Figure 18 provides a depiction of the UDIMM that has been modified with the EKH interposer and the RT-ZMA14 probes which are also modified with 232Ω resistors, as shown earlier by Figure 14. Figure 19 is a zoomed-in view of Figure 18.

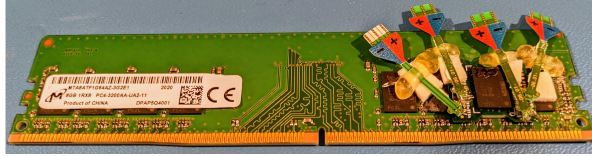


Figure 18 - Depiction of Micron DDR4-3200 (R/C A2) UDIMM [13] with EKH Interposer and R&S RT-ZMA14 Probes

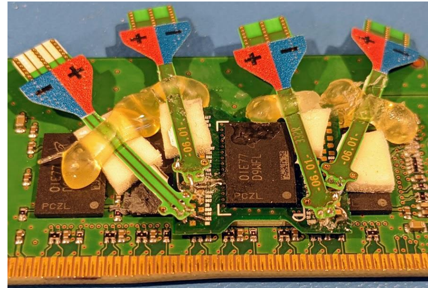


Figure 19 - Zoomed In Depiction of UDIMM with EKH Interposer and R&S RT-ZMA14 Probes

Figure 20 provides a depiction of the final measurement setup with the measurement probes affixed to an interposer that has been modified on a UDIMM.

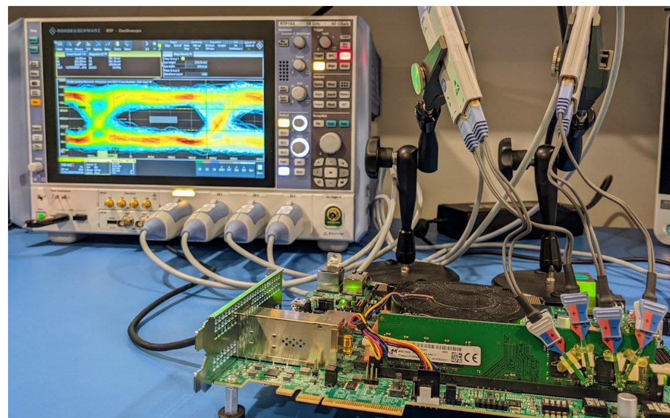


Figure 20 - Measurement Setup With R&S RTP164, RT-ZM160, RT-ZMA-14, Xilinx VCK190, Micron UDIMM (R/C-A2) Modified with Interposer

Vertical measurements are computed from the properties of the eye histogram in the region that is defined by the Eye Level Boundaries parameters, as shown in Figure 21.

On the R&S RTP164 oscilloscope and in ADS Memory Designer, Eye Height is calculated according to EQ(1).

$$Eye\ Height = (Level1 - 3 \cdot \sigma_{LEVEL1}) - (Level0 + 3 \cdot \sigma_{LEVEL0}) \quad (1)$$

As shown, Level1 is the mean of the vertical eye histogram in the upper half of the eye-level boundary, and Level0 is the mean of the vertical eye histogram in the lower half of the eye-level boundary.

Horizontal measurements are computed from the statistics of the crossing histogram at certain amplitude thresholds, as shown in Figure 21.

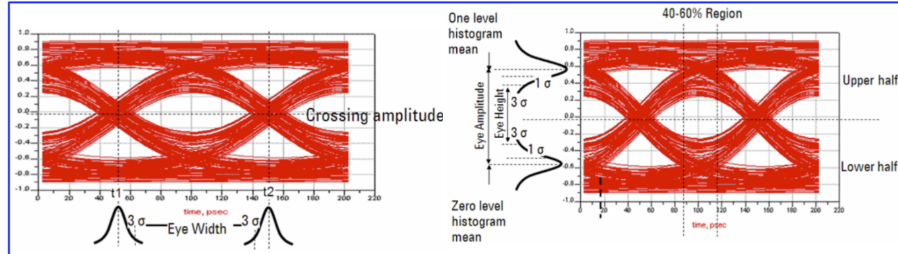


Figure 21 - Eye Diagram Eye Width and Eye Height Measurement Methods [14]

On the R&S RTP164 oscilloscope and in ADS Memory Designer, Eye Width is calculated according to the EQ(2).

$$Eye\,Width = (t_2 - 3 \cdot \sigma_2) - (t_1 + 3 \cdot \sigma_1) \quad (2)$$

Where t_2 and t_1 are the mean values of the crossing time histograms.

However, even the JEDEC DRAM specification does not define eye diagram measurements this way. This method is a good way to correlate simulations to measurements since these eye width and eye height calculations are available both on the R&S RTP164 scope and in Keysight PathWave ADS. Lastly, per Micron, their typical approach to correlation is by eye shape, not eye width and eye height, due to the extensive lot variation across DRAMs.

VII. DDR4-3200 MEASUREMENT RESULTS AND ANALYSIS

The measurement results for DQ49 (DQ1 on the interposer) are shown in Figures 22 and 23, which also both include the DDR4-3200 eye mask. It is important to note that Figures 22 and 23 are the same measurement, except Figure 22 does not include the probe loading, whereas Figure 23 does include the probe loading from the RT-ZMA14 probe. On the RTP164, a simple button press allows users to include or remove the probe loading from the measurement. To accurately correlate our simulation model to measurement, probe loading must be considered. When probes are applied to a circuit, there is a small amount of capacitance from the probe that can interact with the circuit. Further, when a high-frequency signal is applied to a capacitor, a frequency-dependent impedance is seen by the oscilloscope. If the impedance is high enough, this can weaken the signal or render it potentially unusable.

As depicted by Table 1, a 13% (50 mV) signal level improvement in eye height is observed when probe loading is removed from the measurement. This level difference is due to the capacitive loading from the

RT-ZMA14 probe. Further, this signal loss will vary from one RT-ZMA14 probe to another. Therefore, understanding the effects of probe loading is an essential part of making good measurements [8].

Lastly, the results summarized in Table 1 reflect measurement captures for at least 4096 bits across the channel. With 4096 bits and a DDR4-3200 unit interval of 312.5 ps, it equates to a total DDR4-3200 write simulation time of approximately 1.3 μs needed for correlation to measurement.

Table 1 - DDR4-3200 Measurement Results with and without Probe Loading

Parameter	**Measurement with Probe Loading Included**	**Measurement with Probe Loading Removed**	**Measurement Difference**	**Signal Loss due to Probe Loading**
DQ1_EYE HEIGHT - 3σ	326 mV	376 mV	50 mV	-13%
DQ1_EYE WIDTH - 3σ	223 ps	222 ps	1 ps	+0.5%

Multiple measurements were made of DQ49. From these measurements, the three measurements selected were the lowest, medium, and highest eye height results, which are shown in Figure 24. These results were averaged, and the summary of these results is shown in Table 2. As shown by Table 2, an average eye height was found to be 348 mV, and an average eye width was found to be 228 ps.

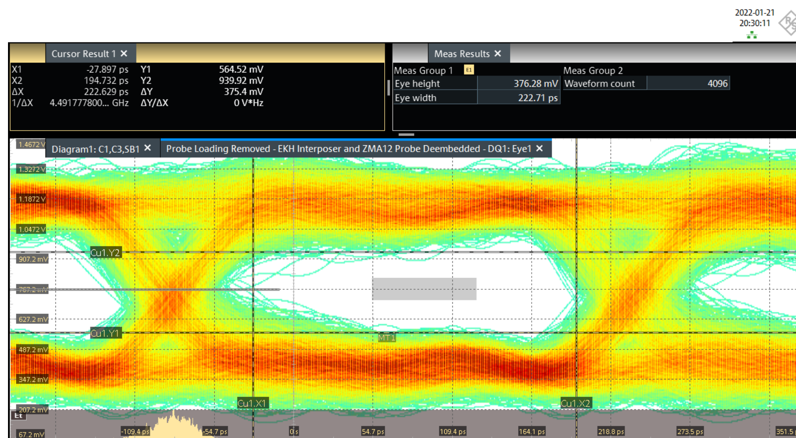


Figure 22 - DQ1 Write Eye Measurement, No EQ, DRV STR = 40Ω, ODT = 40Ω, SLEW RATE = FAST, Interposer and RT-ZMA14 Probe De-embedded, Probe Loading Removed

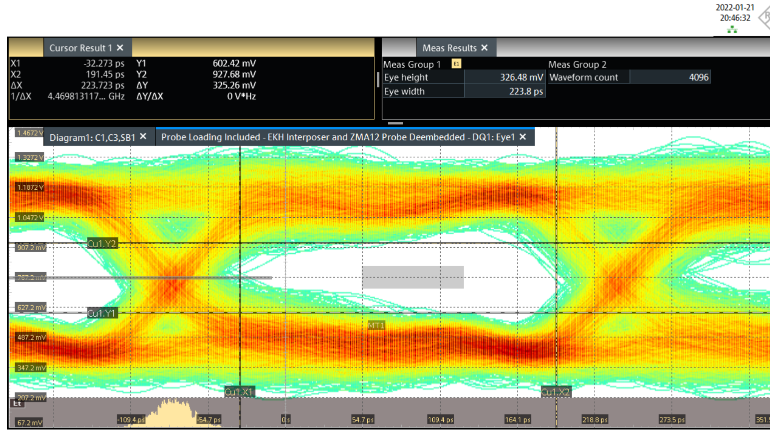


Figure 23 - DQ1 Write Eye Measurement, No EQ, DRV STR = 40Ω, ODT = 40Ω, SLEW RATE = FAST, Interposer and RT-ZMA14 Probe De-embedded, Probe Loading Included

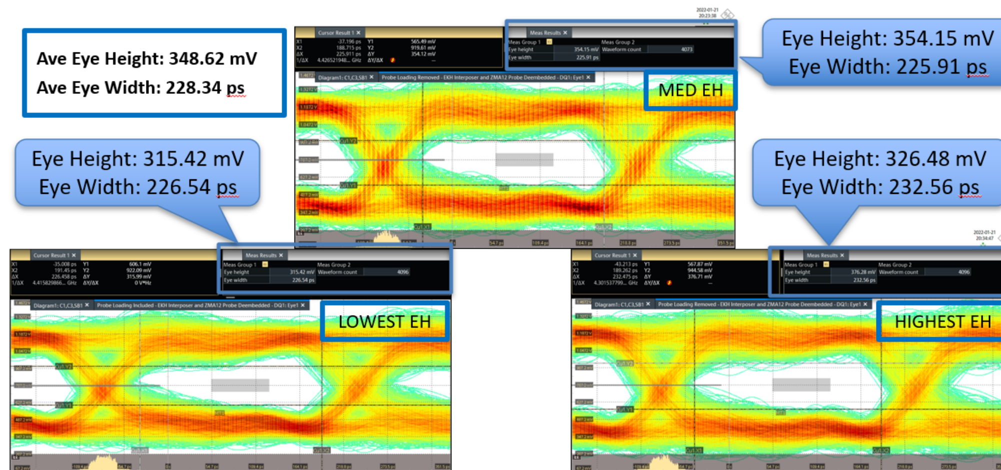


Figure 24 - DQ1 Write Eye Measurement Results, No EQ, DRV STR = 40Ω, ODT = 40Ω, SLEW RATE = FAST, Interposer and RT-ZMA14 Probe De-embedded, Probe Loading Removed

Table 2 - Summary of DDR4-3200 Measurement Results

Parameter	Lowest Eye Height	Medium Eye Height	Highest Eye Height	**Average**
DQ1_EYE HEIGHT - 3σ	315.42 mV	354.15 mV	376.28 mV	**348.62 mV**
DQ1_EYE WIDTH - 3σ	226.54 ps	225.91 ps	232.56 ps	**228.34 ps**

Lastly, it was found that the ODT setting of 40Ω reported by Xilinx was incorrect as depicted on the measurement shown in Figures 22 and 23. This thought was explored after a discussion was had with Xilinx to confirm if the ODT setting of 40 Ω was correct. By looking at the measurement results, it is determined that this ODT setting of 40Ω is not possible. An ODT setting of 80Ω is more reasonable. Regarding Figure 25, for a memory controller using a pseudo open drain (POD) configuration, with a drive strength of 40Ω and an ODT setting of 40Ω, the lowest voltage level that is achievable is 0.6V for

LEVEL0. Whereas with a drive strength of 40Ω and ODT setting of 80Ω, the lowest voltage level possible is 400 mV for LEVEL0, which is more in line with the actual measurement captured.

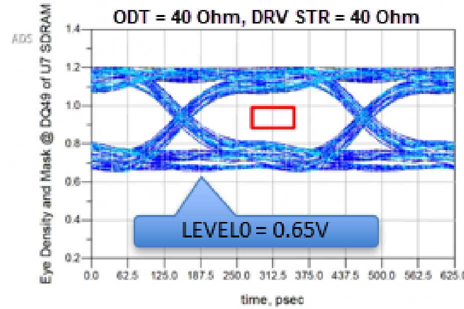
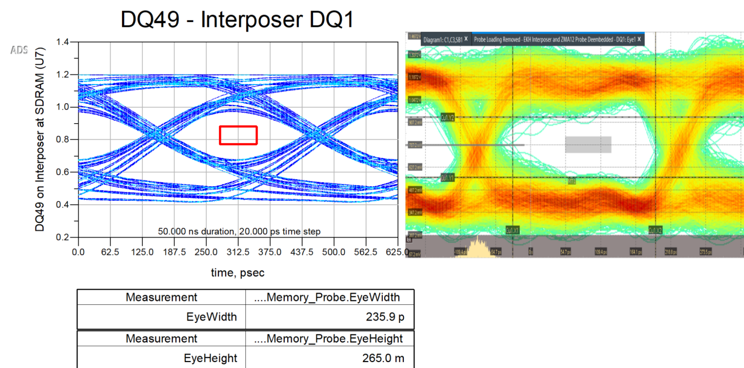


Figure 25 - SI Only Simulation with Versal IBIS Model using ODT setting of 40Ω, with 40Ω drive strength

VIII. DDR4-3200 SIMULATION TO MEASUREMENT CORRELATION RESULTS AND ANALYSIS

The initial simulation results for DQ49 or DQ1 on the interposer are shown in Figure 26. These results were found after optimizing the eye-opening by using an ODT value of 80Ω. This ODT setting is different from the measurement that reportedly used an ODT setting of 40Ω and was previously shown to be incorrect by analysis. The following result shown in Figure 26 is an SI-only simulation using the Versal IBIS RLC package model. Although the eye is open, the rising and falling edges show that they are very slow even compared to the measured data. The eye height is relatively small compared to measurement. The average eye height measurement showed an 82 mV larger eye height or 31% larger eye height. Further comparison between the initial SI Only simulation results shows that the eye height, width, and overall shape are very different from measurement. These differences will also be investigated and discussed in the following paragraphs.



Measurement	....Memory_Probe.EyeWidth
EyeWidth	235.9 p
Measurement	....Memory_Probe.EyeHeight
EyeHeight	265.0 m

Figure 26 - SI Only Simulation with Versal IBIS Model RLC package, 50 ns Duration vs. Measurement

If the IBIS model RLC package is turned off (or disabled), the simulation result is shown below in Figure 27. A slightly better opening (4 mV) is observed. However, this concludes that the Versal IBIS RLC package model is still too slow and not an accurate model to use for DDR4-3200 simulation.

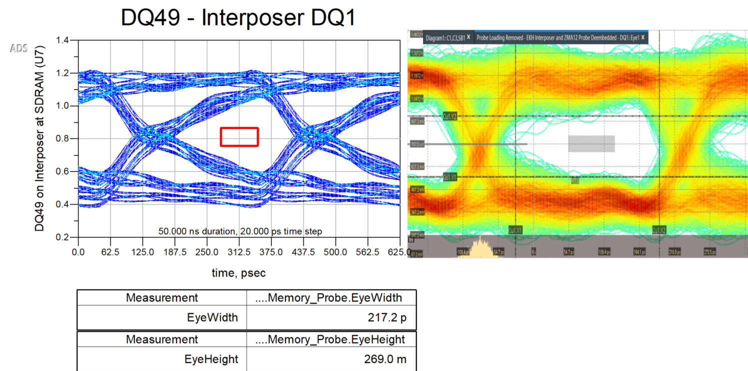


*Figure 27 - SI Only Simulation with Versal IBIS RLC package Off (**Disabled**), 50 ns Duration vs. Measurement*

As a next step, the Versal distributed s-parameter package model was used instead of the RLC package. This result is shown in Figure 28. The eye height is still smaller by over 50 mV compared to average eye height measurement results. The results look more promising since the eye shape correlates better to the eye shape seen during measurement.

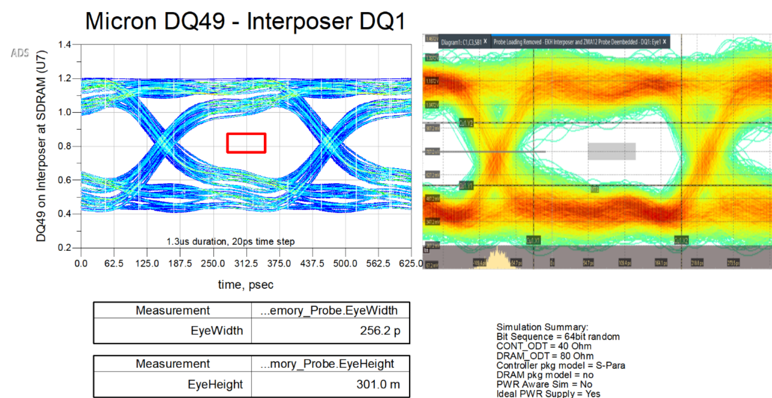


Figure 28 - SI Only Simulation with Versal s-parameter distributed package, ODT 80Ω, No DRAM PKG, DRAM ibis v2.4, DRAM corner = TYP, 1.3 μs Duration vs. Measurement

Regarding Figures 28 and 29, a 13% (or 38 mV) increase in eye height and a 4% (or 10 ps) increase in eye width is observed by moving from the Versal distributed s-parameter package model to the Versal IBIS sparse matrix package model.

Additionally, accuracy issues were identified with the Micron z11b.ibs package models, so both simulations are shown without including the DRAM package as part of the model.

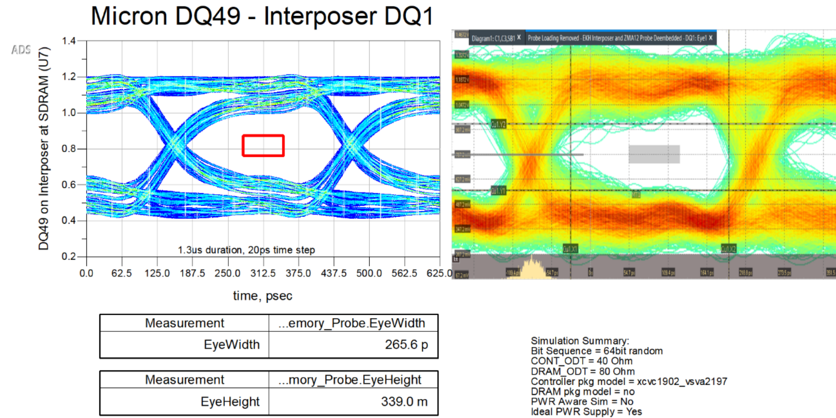


Figure 29 - SI Only Simulation with Versal sparse matrix package, ODT 80Ω, No DRAM PKG, DRAM ibis v2.4, DRAM corner = TYP, 1.3 µs Duration vs. Measurement

Figure 29 is the same simulation as Figure 30, except Figure 29 uses version 2.4 of the Micron z11b.ibs model and Figure 30 uses the recently released version of 2.8.2. As shown just by using a newer version of the same ibis model, a 0.6% (2 mV) increase in eye height is observed.

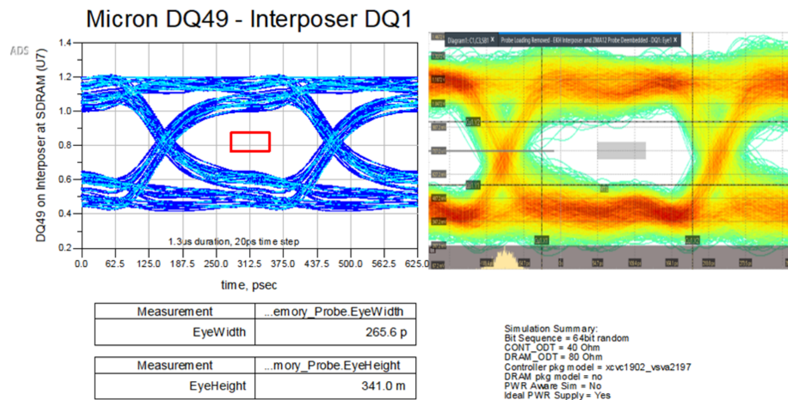


Figure 30 - SI Only Simulation with Versal sparse matrix package, ODT 80Ω, No DRAM PKG, DRAM ibis v2.8.2, DRAM corner = TYP, 1.3 µs Duration vs. Measurement

Further comparison between the measurement and simulation in Figure 30 shows that eye LEVEL0 value is around 20 mV lower in the measurement. This implies that the ODT value in the Micron DRAM ibis model is set to a lower impedance than what was measured. In other words, the measured model had an ODT value that is weaker or higher impedance than 80 Ω. After engaging with Micron on this topic, it was found that the DRAM ibis model corner cases (Typ/Slow/Fast) in the 80 Ω submodel respectively correlate 82.3Ω/92.8Ω/71.3Ω. Therefore by setting the Slow corner on the Micron DRAM ibis model, a 1.8% (6 mV) increase in eye height is observed, which can be seen in Figure 31. The simulation shows an eye height of 0.3% (1 mV) different and an eye width of 15.7% (36 ps) different from the average measurement results. Lastly, jitter was injected into the simulation at the memory controller (Versal). More specifically, 0.36 ps of random jitter (RJ) and 23.4 ps of periodic jitter (PJ) at 200 MHz were used. These results are shown in Figure 32. The eye width is 2.65% (6 ps) larger than the average measurement

result, and eye height is 9.4% (33 mV) lower than the average measurement result. Figure 32 is the best SI-only simulation result achieved. In addition, the shape of the simulated eye is now also identical to measurement. These results are summarized in Table 3. Lastly, as shown by the results in Figure 32, eye width now correlates to measurement with injected jitter. However, from the results shown in Figure 32, it can be concluded that the ODT model in the DRAM ibis model prevented the result from matching the eye height measurement.

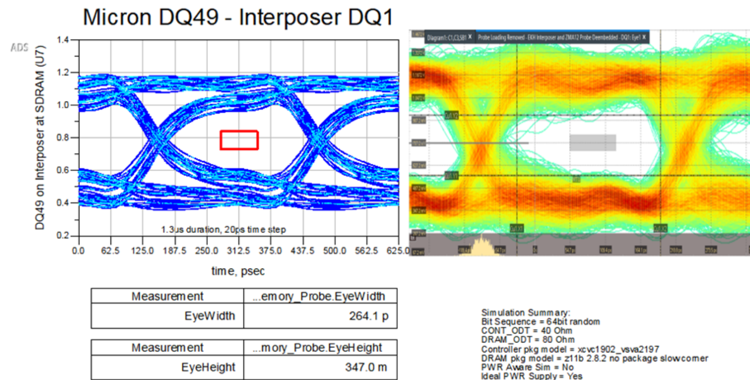


Figure 31 - SI Only Simulation with Versal sparse matrix package, ODT 80Ω, No DRAM PKG, DRAM ibis v2.8.2, DRAM corner = Slow, 1.3 µs Duration vs. Measurement

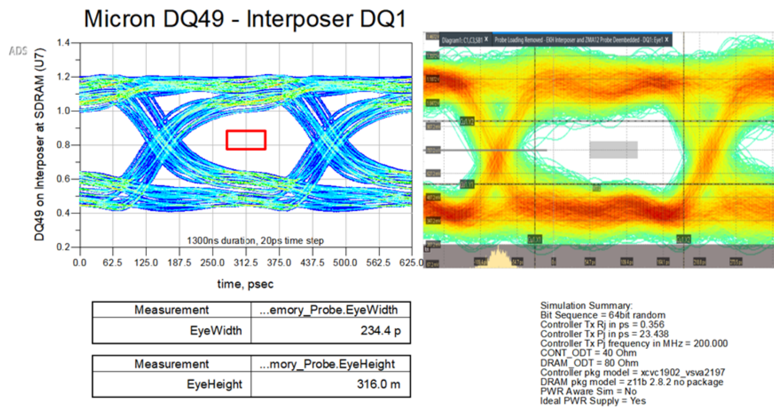


Figure 32 - SI Only Simulation with Injected Jitter - with Versal sparse matrix package, ODT 80Ω, No DRAM PKG, DRAM ibis v2.8.2, DRAM corner = Slow, 1.3 µs Duration vs. Measurement

When adding in the full system PDN to run a power-aware SI simulation, this result is captured by Figure 33. As shown by Figure 33, a 15% (52 mv) decrease in eye height from the average measurement result and a 12% (28 ps) increase in eye width from the average measurement results is observed. This is likely because the IBIS model does not contain the correct Versal IBIS PI models representing pull-down [ISSO PD] transistors, pull-up [ISSO PU] transistors, and composite current curves. This is essential to showing the dynamic impedance of the buffer as well as the switching behavior which correctly allows the composite current from VDD and VSS to be induced into the IO signals, which manifests as SSN.

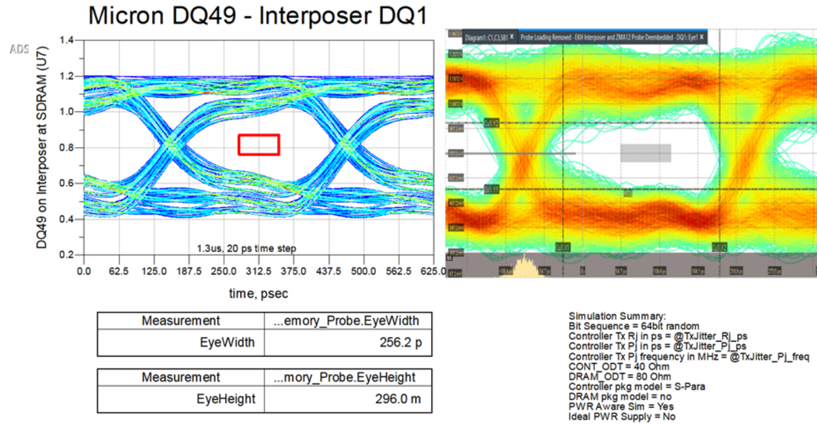


Figure 33 - Power-Aware SI Simulation with Versal s-parameter distributed package, ODT 80Ω, No DRAM PKG, DRAM ibis v2.8.2, DRAM corner = TYP, 1.3 μs Duration vs. Measurement

As shown by this analysis and the summary contained in Table 3, the best result is SI only with injected jitter. Therefore, the conclusion is that the data shown in Figure 32 is as close to measurement correlation as possible for the paper. Xilinx and Micron are both still investigating the issues that were identified with their IBIS model, which will not be completed in time for the publication of this paper.

For all of the results shown in Table 3, the simulation duration used was 1.3 μs (4160 bits), which increases the number of bits across the channel to more closely match the measurement. In addition, for all of the simulations shown, a 64-bit PRBS pattern was used.

Table 3 - Summary of DDR4-3200 Simulation and Measurement Results

Parameter	SI Only Simulation Versal Sparse Matrix Model, DRAM PKG Off, DRAM SLOW Corner	SI Only Simulation with Injected Jitter Versal Sparse Matrix Model, DRAM PKG Off, DRAM SLOW Corner (MEM CTL RJ = 0.36 ps / PJ = 23.4 ps)	Power Aware Simulation Versal SP Model, DRAM PKG Off, DRAM TYP Corner	Average Measurement without Probe loading
DQ1_EYE HEIGHT - 3σ / % Delta from AVG Meas.	347 mV / -0.3% Delta	**316 mV / -9.4% Delta**	296 mV / -15% Delta	348 mV
DQ1_EYE WIDTH - 3σ / % Delta from AVG Meas.	264 ps / +15.7% Delta	**234 ps / +2.65% Delta**	256 ps / +12% Delta	228 ps

IX. FURTHER DDR4-3200 SIMULATION RESULTS AND ANALYSIS

The JEDEC JESD79-4D DDR4 SDRAM standard and Micron R/C A2 UDIMM datasheet specify an operating voltage of 1.2 +/-60 mV. This voltage ripple specification also applies to the Micron MT40A1G8SA SDRAM part used on the UDIMM.

To verify that a significant amount of SSN was captured, a 64-bit PRBS pattern was run across all 64 bits, where each bit pattern was randomly generated. The voltage ripple results are shown in Figure 34. A peak-to-peak voltage maximum of 13.5 mV is shown. However, this is due to the initial PDN in-rush current to charge the capacitors. The ripple voltage steady-state is closer to 7.5 mV, as shown. When

running a power-aware SI simulation, the expectation for a 1.2V DDR4 bus would be for the voltage ripple to be around at least 60mV peak-to-peak or more due to all of the parallel DDR4 signal nets switching. Further inspection of the 1.2V VDD noise spectrum shows that the noise peak for the DDR4-3200 is almost -81 dB, which is likely too low to be realistic.

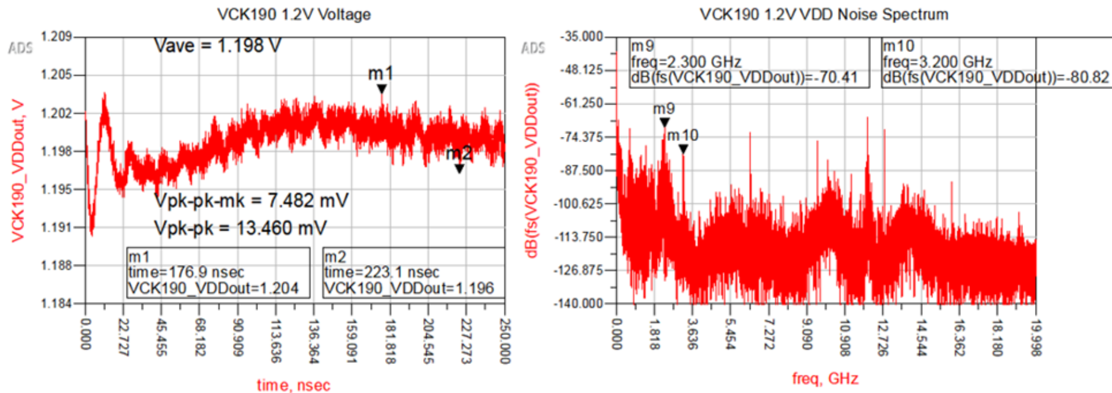


Figure 34 - VDD Ripple and Noise Spectrum Result - 1.2V Rail on VCK190

As shown by Figure 35, DQ49 exhibits a minimal noticeable amount of noise superimposed onto the waveform due to the VDD noise. This is likely because the Xilinx Versal IBIS mode does not include accurate [Composite Current], [ISSO PU], [ISSO PD] curves, which can be correlated by the noise spectrum results shown in Figure 34. This again indicates that the Versal IBIS PI models are likely incorrect. If this model were correct, the composite currents from VDD would be seen as SSN superimposed onto the DQ waveform shown in Figure 35 while exhibiting a much higher ripple voltage.

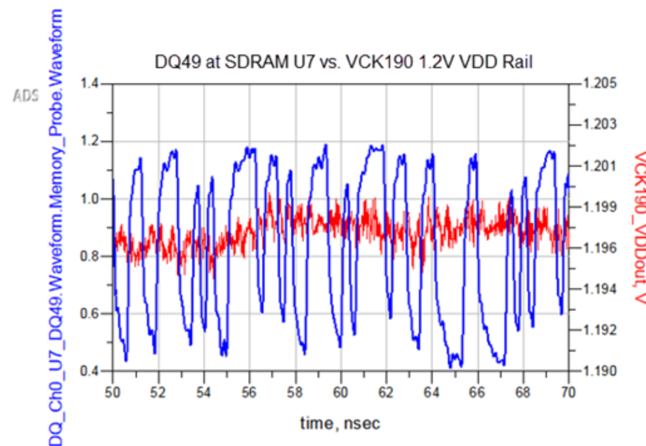


Figure 35 - SSO Result - VCK190 VDD Rail vs. DQ49 at SDRAM U7

X. DDR5 MEMORY INTERFACES AND BEYOND

Looking forward, beyond DDR4, DRAM has evolved to better suit growing system-level needs. Memory standards often follow the general scalability rule of ‘2x’ when considering new performance metrics such as data rate, capacity, and burst length, all while maintaining similar or acceptable power envelope

and latency targets. The VDD/VDDQ of 1.1V (vs. 1.2 for DDR4) helps with power reduction but requires tight voltage regulation of +/-3% to meet SI/PI requirements. With increasing frequency and downward voltage scaling, one would expect more relief with improved signaling techniques. Unlike serial interfaces like PCI Express or Ethernet, DDR still uses single-ended signaling. As shown previously, care must be taken to fully comprehend both SI and PI effects, which are present in high-speed, wide parallel buses like DDR.

Designers looking to adopt DDR5 must now account for effects from PDN, loading or reflections, and channel equalization. As an example, a typical system configuration is a two DIMM-per-channel, dual-rank (two loads per DIMM) system. Multi-rank DIMMs have the advantage of higher capacity but include an additional load for every additional rank. Each DQ is connected to two DRAMs, and with a two DIMM-per-channel system, this presents four loads (2 DpC x 2 loads per DIMM) to the memory controller. Because of the multi-drop architecture, when one rank is active the other rank loads the bus with additional reflections.

With DDR5, the channel response for memory interfaces with 4 DIMM slots can become a challenge. Regarding the model shown in Figure 36, consider an RDIMM with a series resistor: the stubs that occur from the three empty DIMM slots are too long to compensate with a 4-tap DFE. This is shown by looking at the insertion loss plot depicted in Figure 37. In summary, this provides insight that traditional multi-DIMM DDR architectures might not be possible on DDR5 speeds.

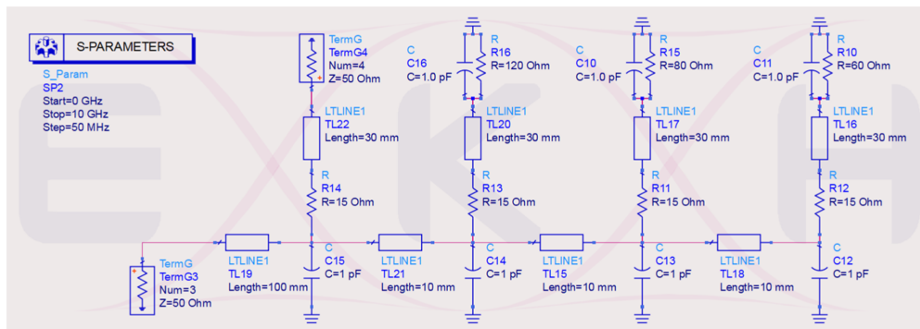


Figure 36 - 4 DIMM Slots Model - 10mm DIMM-to-DIMM + 30mm DIMM stub [15]

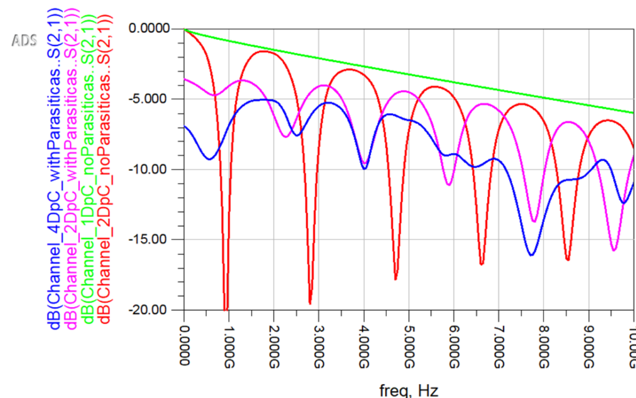


Figure 37 - 4 DIMM slots Channel Insertion Loss Response [15]

Now, let’s consider a standard 2 DIMM per channel (2DpC) configuration for a DDR5-6400 application, where the DDR5 data rate for this channel is equal to 6400 Mbps.

In Figure 38, shown below, a 2DpC configuration is shown with arrows depicting the reflection of the wave in this channel.

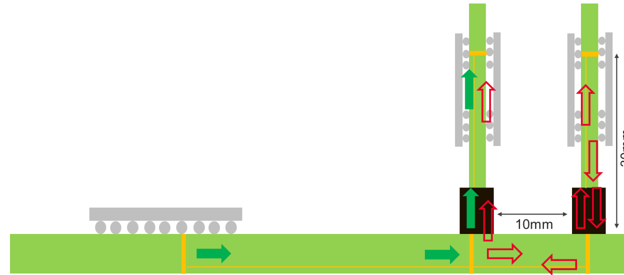


Figure 38 - Reflections Analysis in a 2 DIMM per Channel (DpC) Configuration [15]

Further analysis shows that the total length for the reflected wave is found by equation (3).

$$Reflected\ Wave\ Total\ Length = 10\ mm + 30\ mm + 30\ mm + 10\ mm = 80\ mm \quad (3)$$

For this we can determine the delay of the reflected wave by EQ(4).

$$Reflected\ wave\ delay = 80mm \times 7\ ps/mm = 560\ ps \quad (4)$$

Assuming a DDR5-6400 channel bandwidth, that equates to a data UI of 156.25ps. By equation (3) we can determine the minimum number of taps that are needed due to the reflected wave delay based on our defined UI.

$$Min\ DFE\ taps = \frac{560\ ps}{156.25\ ps} = 3.58\ bits \quad (5)$$

With a 4-tap DFE, the maximum delay that can be tolerated is found by multiplying the total taps by the data rate UI as shown by EQ(6).

$$Maximum\ DFE\ Delay = 4\ taps \times 156.25\ ps = 625\ ps \quad (6)$$

By EQ(8) we can calculate the remaining DFE delay available to the channel.

$$Remaining\ DFE\ Delay = 625\ ps - 560\ ps = 65\ ps \quad (7)$$

As shown, equalization is needed to compensate for the reflections in the DDR5 channel. Additionally, in DDR5 channels, these interfaces will equate to greater SSO and SSN noise, which will also require power-aware modeling to achieve simulation accurately needed for design sign-off. Multi-drop architectures could undoubtedly limit the higher performance of a memory design unless there is relief

from equalization. In addition to reflections, insertion loss, package effects, and other parasitics should be accounted for as a complete model. DDR5 end-to-end system modeling will require a golden channel, as shown in Figure 39. This is a typical system for design parameter exploration [16]. To facilitate the development of higher speeds, additional research is needed for crosstalk minimized routing, especially in pin field and breakout regions. In addition, research needs to be done on unmatched CK/DQS path compensation, multi-rank loading, and Tx/Rx equalization.

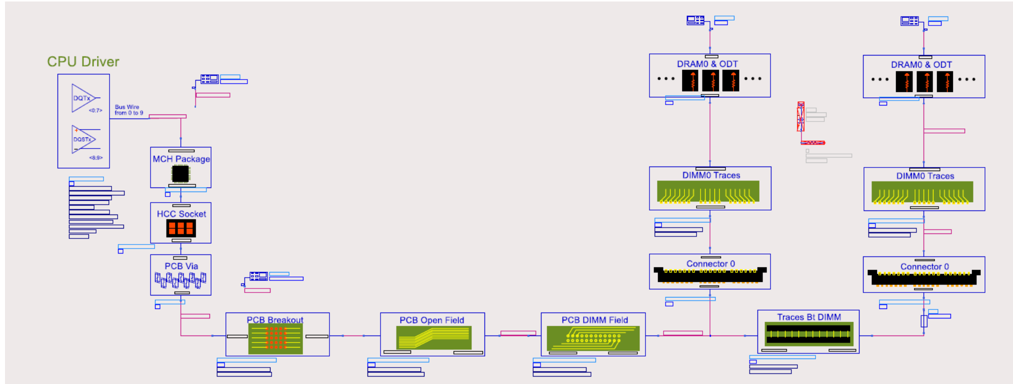


Figure 39 - DDR5 End to End System Model for 2 DIMM per Channel Topology [17]

XI. CONCLUSIONS AND SUMMARY

In this paper, a detailed DDR4-3200 measurement method with an interposer was analyzed and discussed. Additionally, DDR4-3200 power-aware SI, as well as SI-only simulations, were discussed and analyzed. Further, when vendor models were identified to be incorrect, a solution was presented to show how to work towards achieving a system model with PathWave ADS Memory Designer to achieve a more desired simulation solution that correlates to an actual measurement result. Lastly, since SSN or SSO noise is a function of inductively coupled noise, additional research is needed to explore the effects of this noise generated through the return path at the UDIMM connector, Versal package, VCK190 PCB, and UDIMM PCB.

As shown, with a multi-drop DDR5 system, the eye is closed due to reflections from the unused DIMM slot. However, as memory systems are continually adopting high-speed serial technologies, new memory devices may need to use more advanced equalization (e.g., DDR5) and multi-level modulations (e.g., DDR6 and GDDR7 with PAM4). These complex parallel memory interfaces will drive system-level performance to include power-aware SI modeling using IBIS models that allow modeling with pre-emphasis and AMI. Additionally, DDR5 has moved the power management from the motherboard to the DIMM. Putting the PMIC on the module allows tighter control over voltage regulation and power-up sequencing. Regardless, noise margins are shrinking at the same time.

DDR5 power-aware SI simulation using AMI modeling is not yet possible in any EDA simulation solution. This means designers will need to apply a two-step approach for DDR5 simulations to know where margin exists in their designs. To support full system-level performance, IC vendors and EDA

software tools will need to develop a suitable solution that allows power-aware SI and AMI modeling with equalization.

XII. ACKNOWLEDGEMENTS

We would like to express our sincere appreciation to Steven Sandler (Picotest), Stephen Slater (Keysight), Jason Ruffing (Rohde & Schwarz), Mike Schnecker (Rohde & Schwarz), Nacim Bravo (Keysight), Taylor Maddix (Xilinx), Ryan Arp (Xilinx), Fran Olveri (Xilinx), Jon Schimek (Xilinx), Sam Hendrix (Xilinx), John Rinck (Xilinx), Justin Butterfield (Micron) and Stephanie Dannan for their support to help make this paper possible. We would also like to thank Keysight and Rohde & Schwarz for the excellent technical support on the simulation and measurement efforts.

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IX. APPENDIX

A. DDR4 MEASUREMENT TEST EQUIPMENT LIST

Table 4 - Test Equipment List for DDR4-3200 Measurement

Description	Model	QTY	Notes:
16 GHz BW Oscilloscope	R&S RTP164 [18]	1	SW packages included: DDR Memory analysis, Jitter, De-embedding
16 GHz BW Modular Probe	R&S RT-ZM160 [19]	4	
Modular Probe Tip	R&S RT-ZMA14 [12]	4	Measuring 4 signals per DIMM
Flex Tips	1337.9781.02	20	This comes in a sheet of QTYx10 with each RT-ZMA-14. 10 Flex Tips 332 Ohm solder-in.
UDIMM modified with EKH Interposer		1	
Probe Holders	Keysight N2787A [24]	2	3D Probe Positioner. Alternative = R&S RT-ZAP
Kapton Tape	N/A	N/A	Used as needed
Glue/RTV	N/A	N/A	Used to secure probe tips to interposer

B. VCK190 VRM MEASUREMENT TEST EQUIPMENT LIST

Table 5 - Test Equipment List for VRM Measurement

Description	Model	QTY
Vector Network Analyzer	OMICRON Lab Bode 100 [20]	1
2-port PDN Transmission Line Probe Kit	Picotest P2102A-2X [21]	1
Common Mode Transformer	Picotest J2102B-N [22]	1
Picotest PDN Cable®, BNC-BNC, 0.25-meter	BNCJ/BNCJ-250 [23]	1
SMA Female to N Male Adapter	Pasternack PE9081	1
SMA Female to BNC Male Adapter	Pasternack PE9073	1
BNC Female to N Male Adapter	Pasternack PE9002	1
3D Probe Positioner	Keysight N2787A [24]	1
VRM - Infineon PS5401 Eval (DUT)	EVAL_PS5401-INT [25]	1