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**Conference**
January 30 – February 1, 2024

**Expo**
January 31 – February 1, 2024

*Santa Clara Convention Center*

# Design, Simulation, and Validation Challenges of a Scalable 2000 Amp Core Power Rail

Steve Sandler, Picotest.com
Benjamin Dannan, Signal Edge Solutions
Heidi Barnes, Keysight Technologies
Idan Ben Ezra, Broadcom Semiconductors
Yu Ni, Monolithic Power Systems

# Speakers

## Steve Sandler

*Managing Director, Picotest*

Steve@Picotest.com | Picotest.com

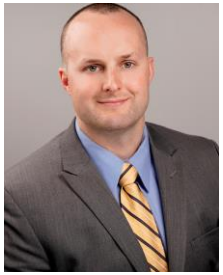
Steve Sandler has been involved with power system engineering for more than 40 years. The founder and CEO of Picotest.com, a company specializing in instruments and accessories for high-performance power system and distributed system testing DesignCon 2023 Engineer of the Year.

## Heidi Barnes

*Power Integrity Applications, Keysight Technologies*

Heidi_barnes@keysight.com | Keysight.com

Senior Application Engineer in the PSS EDA Group of Keysight Technologies. Her recent activities include the application of electromagnetic, transient, and channel simulators to solve signal and power integrity challenges. Author of over 20 papers on SI and PI and recipient of the DesignCon 2017 Engineer of the Year.



## Benjamin Dannan

*Chief Technologist, Signal Edge Solutions*

Ben@signaledgesolutions.com | Signal Edge Solutions

Benjamin Dannan is the Chief Technologist at Signal Edge Solutions, a senior member of IEEE, and an experienced signal and power integrity (SI/PI) design consultant, advancing high-performance ASICs and developing advanced packaging solutions for high-speed digital designs.

## Idan Ben Ezra

*HW and PI Engineer, Broadcom Ltd*

Idan.benezra@Broadcom.com | Broadcom.com

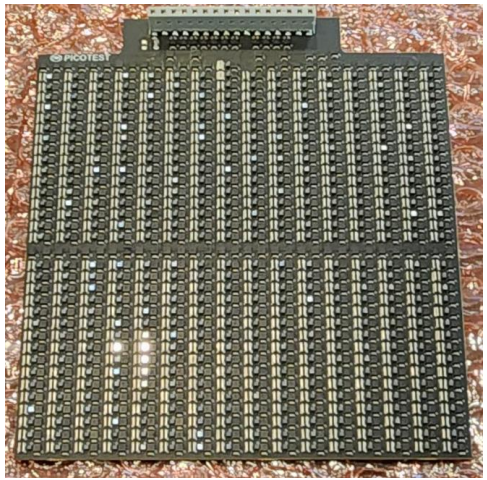
Hardware and PI engineer at Broadcom Semiconductors, DNX group of CSG-Switch Products, in Israel. In Broadcom Idan is a Focal point in full system Power Delivery Network analysis design stages. Idan has hands-on experience with lab power measurements including correlation to simulation.

# Outline

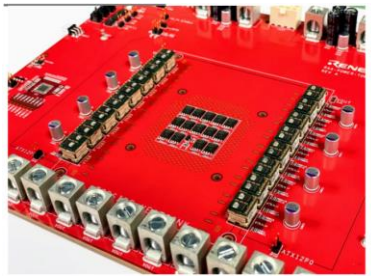
- Who and Why needs 2000 Amps?
- How do we build it?
- Validation with Step Loader – How Hard is This?
- Measure-Based Modeling of the Components and PCB EM Models – Why Measure?
- End-to-end Digital Twin Simulations – Why Simulate?
- Measurement Case Study – It Works!

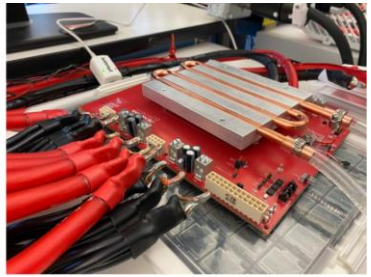
# Why 2000 Amps?

- Motivation:
  - The goal is to demonstrate how one can effectively validate a 2k Amp core power rail design using a substitute 2000 Amps step load device
- Why:
  - While 2000 Amps may seem excessive, the increasing processing power of AI, data centers, and supercomputing has already exceeded this current level (NVIDIA X100 ~1500A)
- Challenges:
  - VRM solutions including modeling (measured based)
  - Driftnet input stage (48V)
  - Thermal design
  - Simulations for Transient, Frequency, EM, DC, and Electro-Thermal
  - How to validate this kind of step
  - Projected dynamic current (ultra high speed testing)
  - Bandwidth of the current from the package
  - ASIC isn't available



# Today's 1000 Amp Stepper Solutions

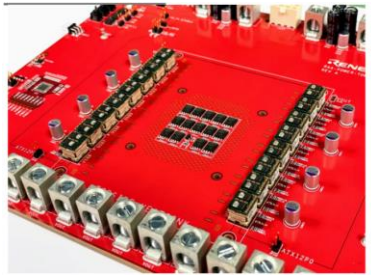


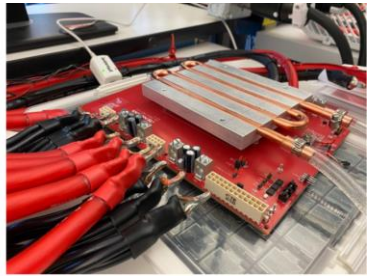


Renesas 16 power tower solution for 1000A


LoadSlammer for 1000A Peak

# Next-Generation 2000 Amp Stepper Solutions

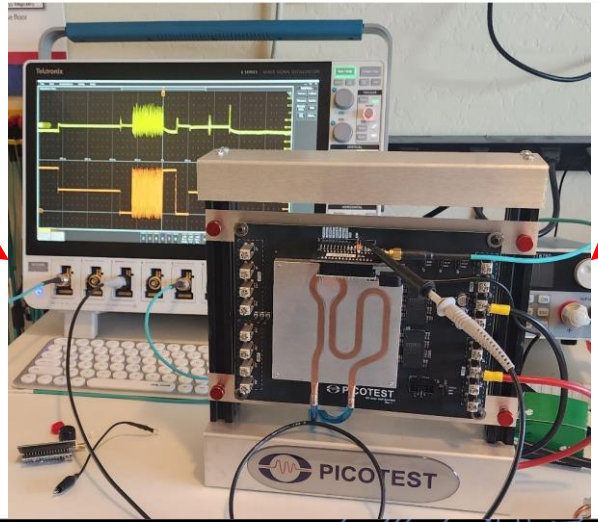


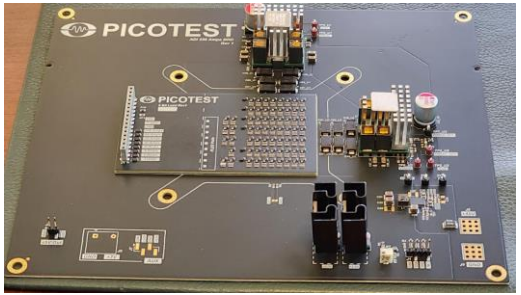


Renesas 16 power tower solution for 1000A


LoadSlammer for 1000A Peak

Picotest 2000A interposer



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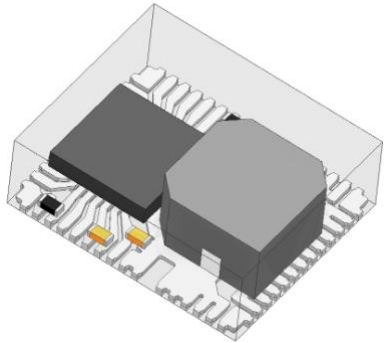
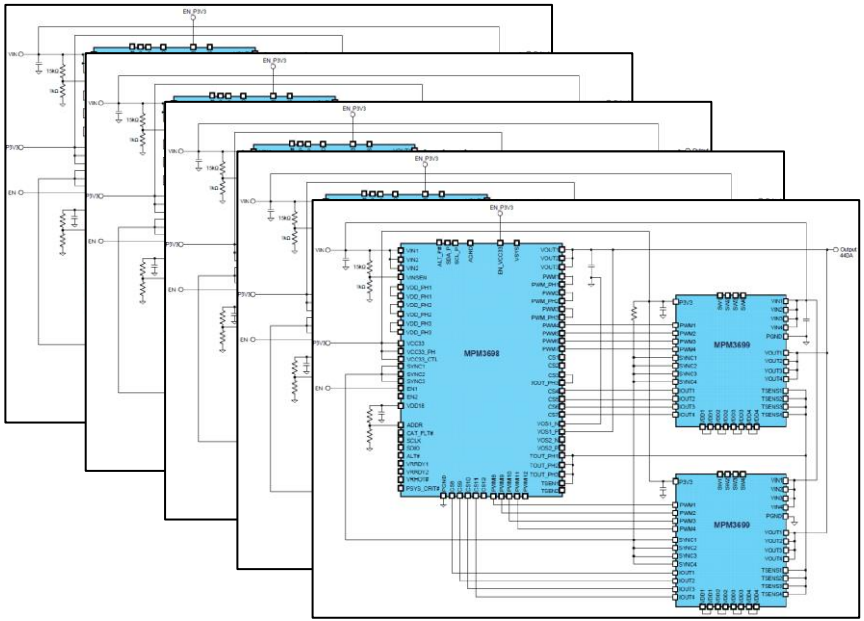
# How to Design a 2000 Amp Power Delivery Solution

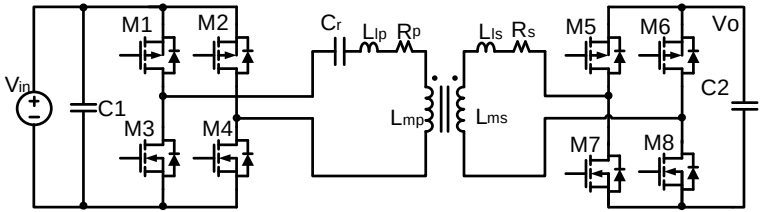
- VRM Vendor
  - MPS and ADI (Analog) only supported this scale
- How:
  - Two major architectural paths today (48V → core voltage) and (48→ 12V/5V → core voltage)
- The implantation:
  - 5 x [Controller + 2 Followers] monolithic models (55 phase total)
  - Up to 2200A peak and ~2000A SS

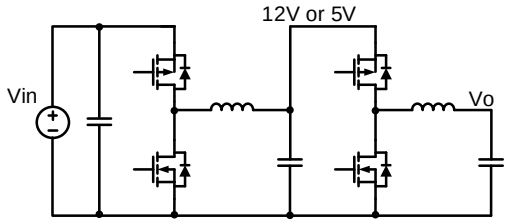




# Architecture Options to Achieve $V_{OUT}$ Core Voltage

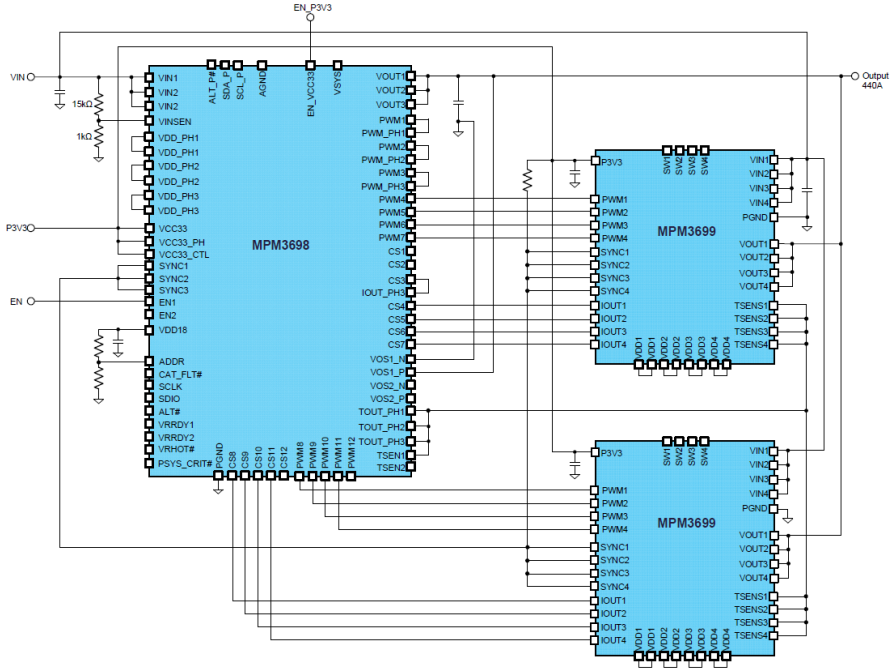
| | 48V → Core Voltage | 48V → 12V/5V → Core Voltage |
|---|---|---|
| Topology | Resonant Converter | Two Stage Buck Converter |
| Advantages | ▪ Good Efficiency<br>▪ Higher Energy Density | ▪ Flexible Combinations<br>▪ Multiple Vendors<br>▪ Optimized Cost<br>▪ Wider Operation Range |
| Disadvantages | ▪ Complex Control<br>▪ Higher Cost<br>▪ Narrow Operation Range | ▪ Lower Energy Density |



# Two Stage 2000A Design

- Fix 4:1 Ratio Step Down 48V -> 12V
- Use Fully Integrated Module 12V -> Core Voltage
- 1 x MPM3698 + 2 x MPM3699 for 400A
- 5 Sets to total 2000A
- Wide $V_{IN}$ for 36V to 54V system
- Wide $V_{OUT}$ for 0.4V to 3.3V core voltage

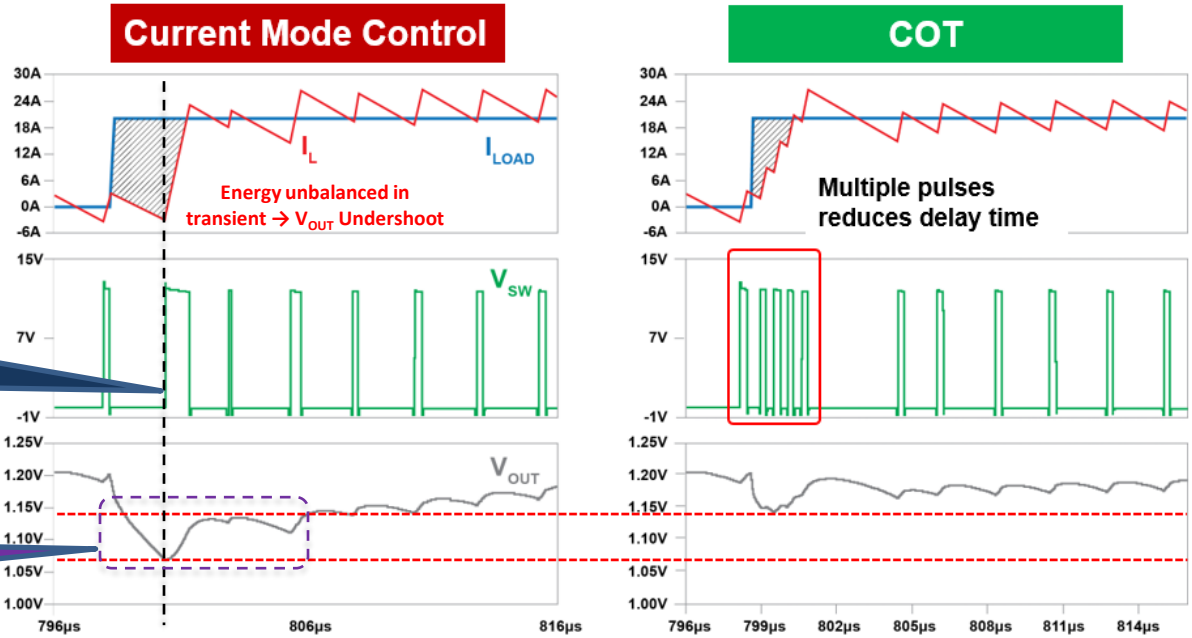



**Scalable Power Delivery Topology 100's of Amps to 1000's of Amps**

# Current Mode Control vs. Constant-On-Time (COT) VRMs

**COT Advantages vs. Current Mode**

- COT can switch faster
  - Faster load transient response
- Reduced PDN output capacitance
- Simpler control loop




$V_{COMP}$ has already responded, but the system needs to wait for internal CLK to turn on SW

$V_{OUT}$ undershoot due to CLK delay

Source: monolithicpower.com/en/advantages-of-constant-on-time-control-in-dc-dc-converters

**For same load current step, COT control can switch faster and further reduce $V_{OUT}$ undershoot**

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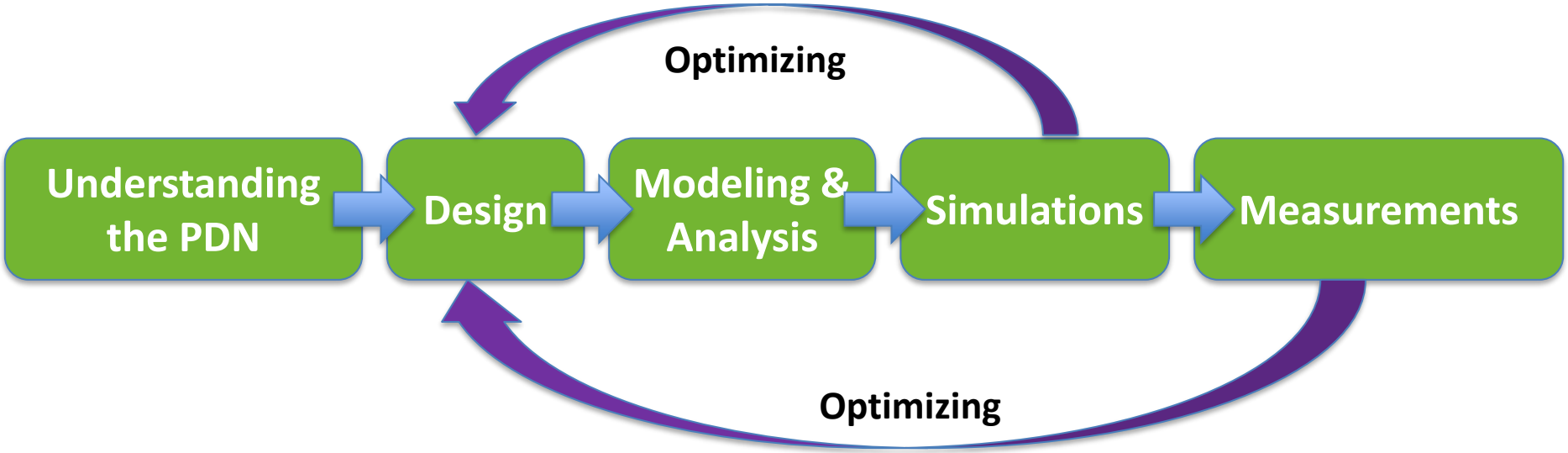
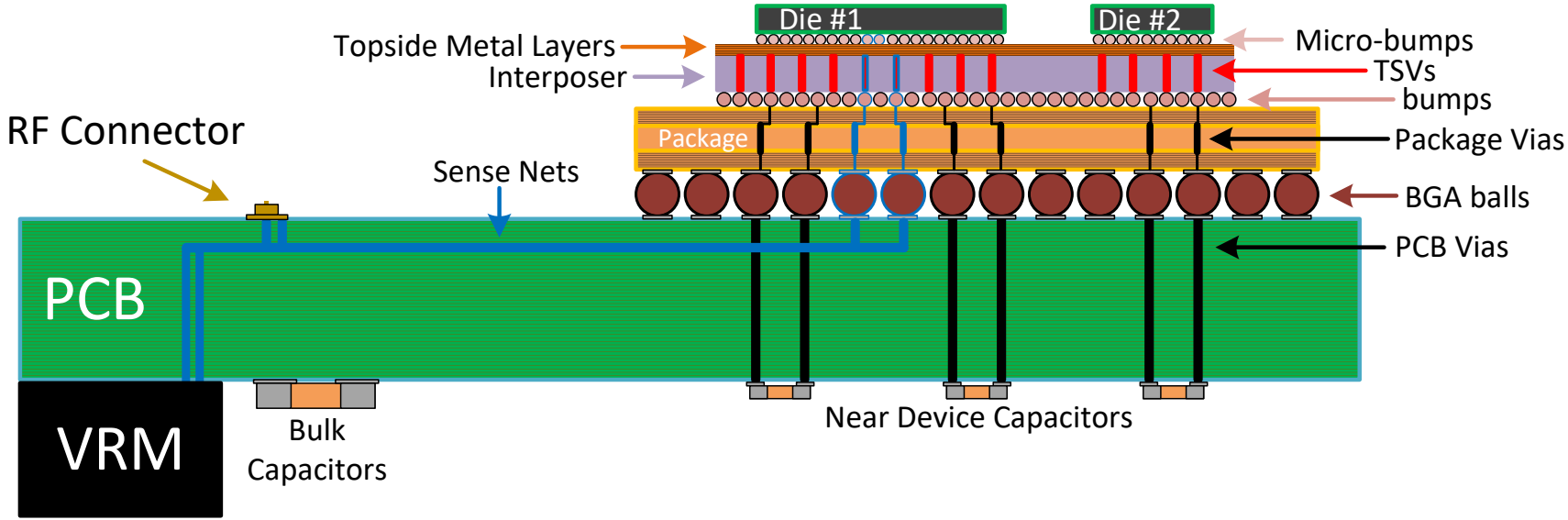
# How to Validate PDN with a step loader

- Validation task:
  - The validation task involves ensuring that the power delivery network (PDN) can **handle** such a **large load** (step and steady state) **without causing** voltage drops, noise, and other issues that could impact the operation of the system



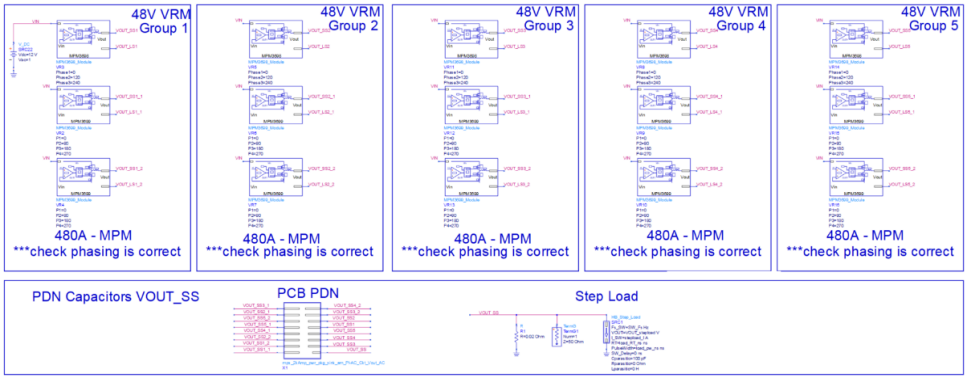
# PDN Design and Simulation Validating steps

- Understanding the Power Delivery System
  - VRM Vendors, Types, Scales, PDN (PCB, Package and Die)



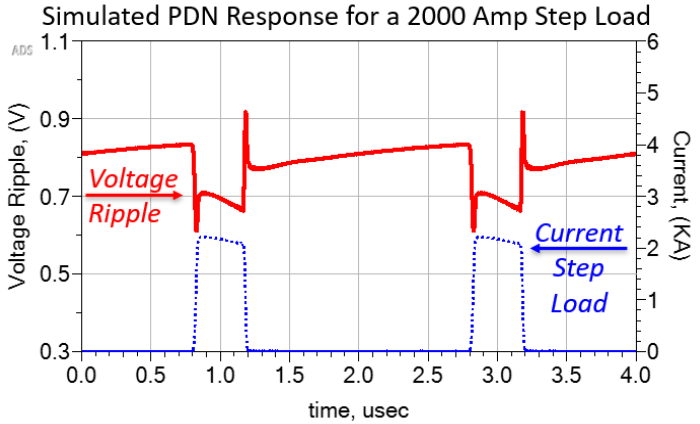
# PDN Design and Simulation Validating steps

- Voltage Regulation
  - Selecting the right multi-phase VRM solution is crucial to achieve a successful working design
  - Switching frequency, LBP, TLVR, Load Line, etc.
- Modeling and Analysis
  - Using modeling and simulation tools to predict how the load will affect the power delivery system (VRM, PCB, PKG, DIE CPM, Sensing points)
- Simulate the Load – The powerful EDA tool



# Validating PDN Simulation Transient Results

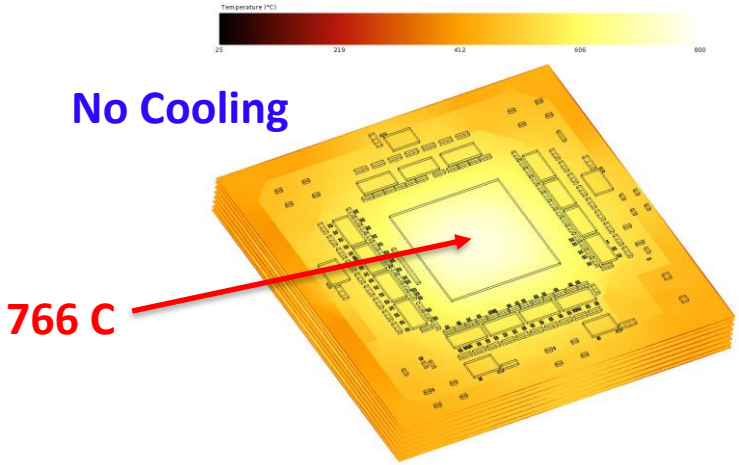
- Transient Analysis
  - This will help to identify the voltage noise ripple magnitude of the undershoot (droop), overshoot (kick), and any resonant ringing on the power rail

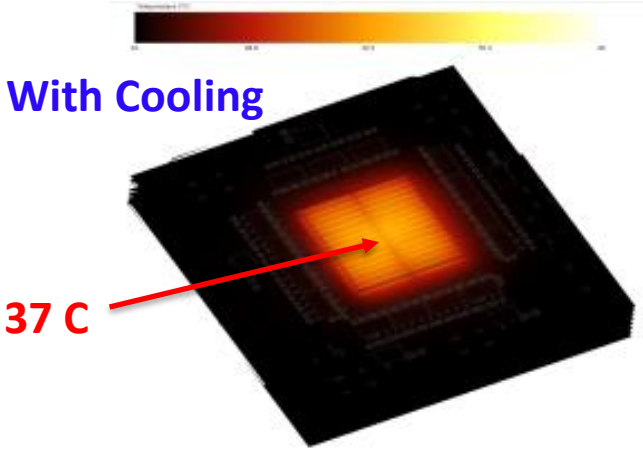



- Noise Analysis
  - When adding the Die behavioral di/dt (from the CPM), check for any unwanted noise or spikes in the power rails during the step load transition

# Validating Thermal Considerations

- Thermal Analysis
  - Operating at 2000 Amps steady state, along with large dynamic step loads, can generate significant thermal heat rise in components



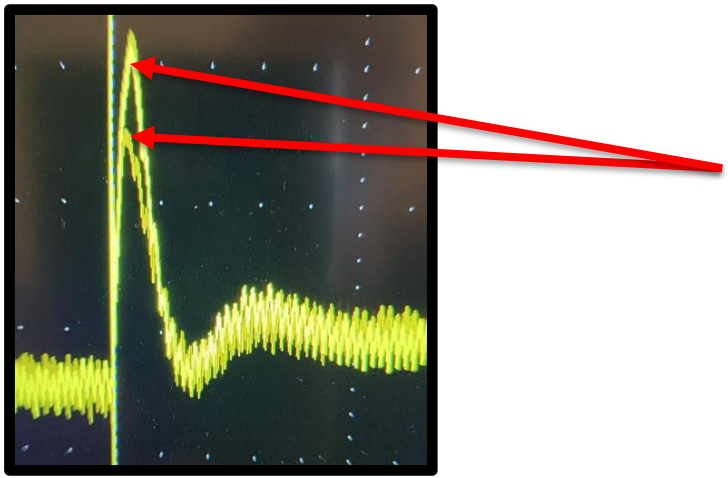




Thermal analysis for a 2000A load with no cooling on the left, and with cooling on the right. This is a symmetric design, so the hottest location is in the center with 766C on the left with no cooling, and a reasonable 37C on the right with ideal water cooling

# Large vs. Small Signal Measurement Validation

- Measurement Equipment
  - Invest in high-quality measurement equipment before trying to measure this kind of step
- Small signal vs Large signal
  - **Small signal** represent relatively constant signals and typically have small variations around a nominal operating point (DC), how impedance varies with frequency also for stability and noise margins
  - **Large signal** focuses on phenomena such as transient, step response, voltage droop

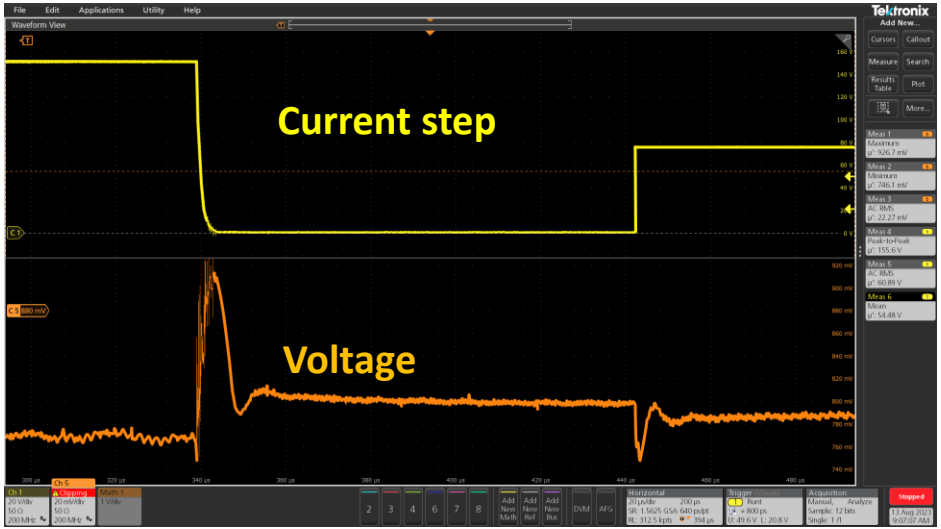
**Voltage vs. Time**

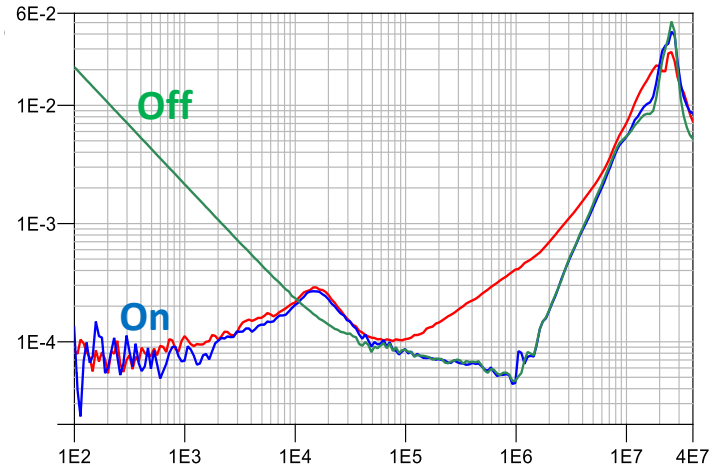


The large signal response shows 2 different responses for the same step load change.

# Time & Frequency Domain Measurement Validation

- Testing
  - Once we have done the necessary design simulations and know what to expect, it's time to test the system.
  - We will check it in both time and frequency domain, voltage drop and Current step




**2-Port Shunt-Thru**

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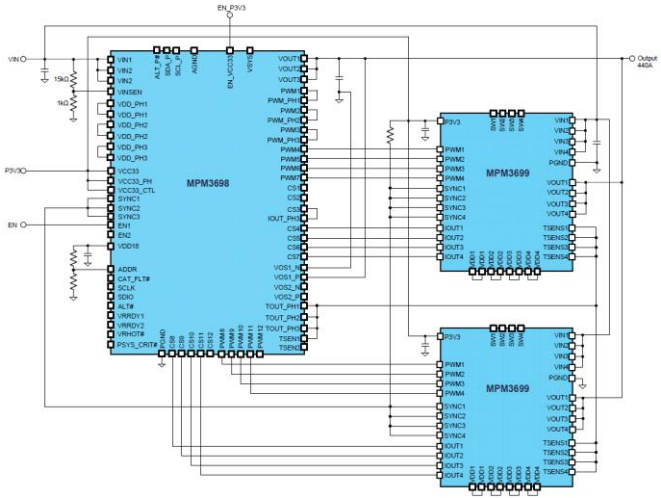
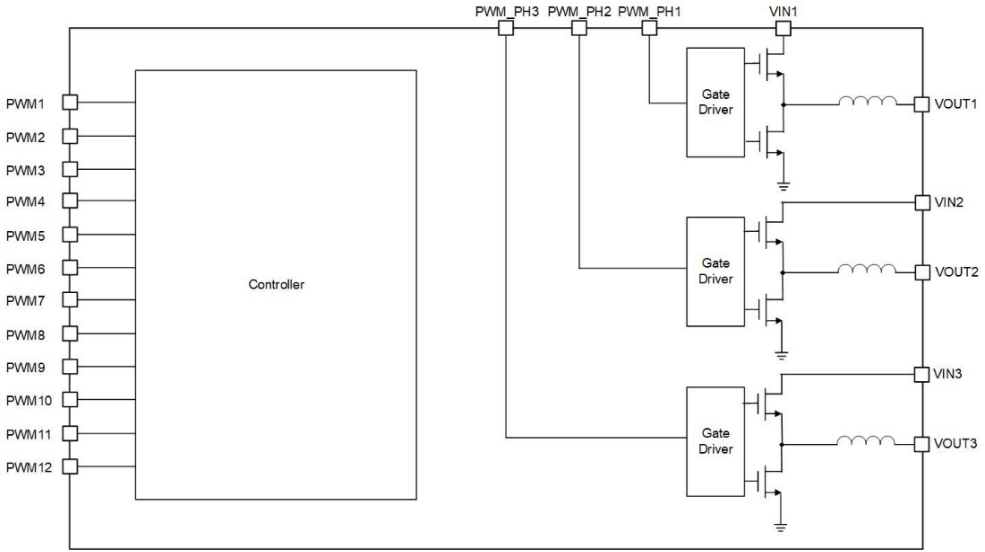
# Modeling the Source of the Power

- Accurate simulation results require a high-fidelity VRM model and the PCB effects!



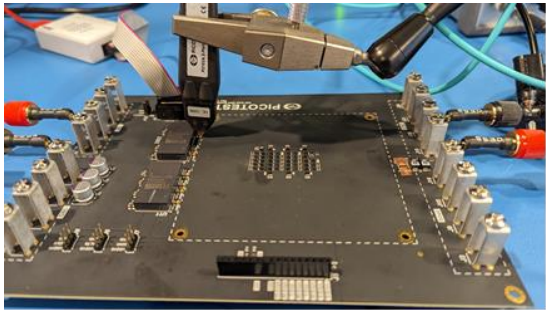

## VRM Topology



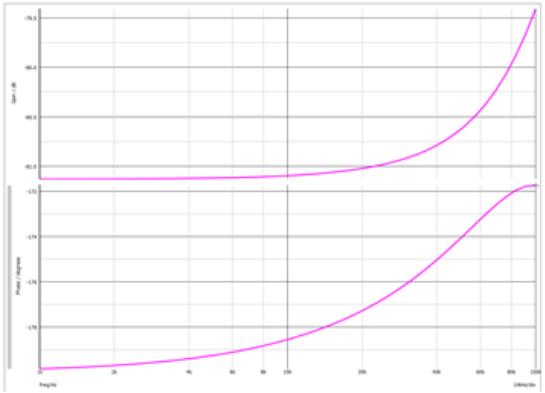
# Measurement-Based Modeling of the VRM

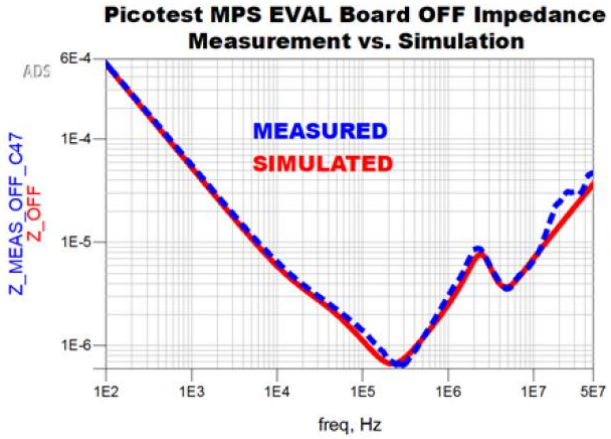
- Measurement of VRM impedance (OFF/ON)
- PSRR Model from SIMPLIS used to tune PSRR response of VRM in ADS
- The VRM model was built for MPM3698 since this can be scaled since gain parameters for MPM3698 and MPM3699 were the same

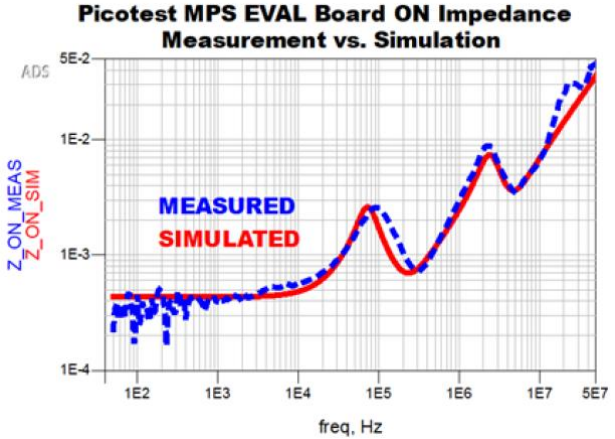
**Impedance Measurement Setup**



**PSRR from SIMPLIS**



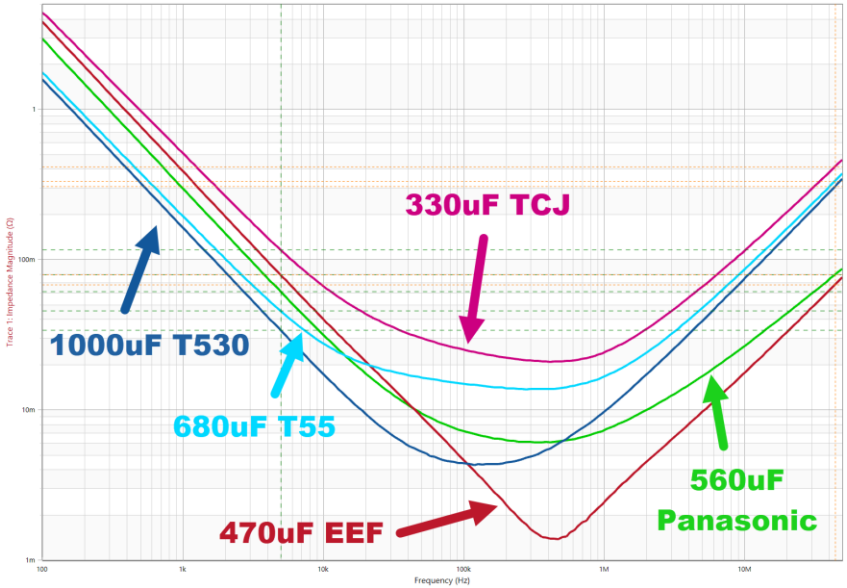


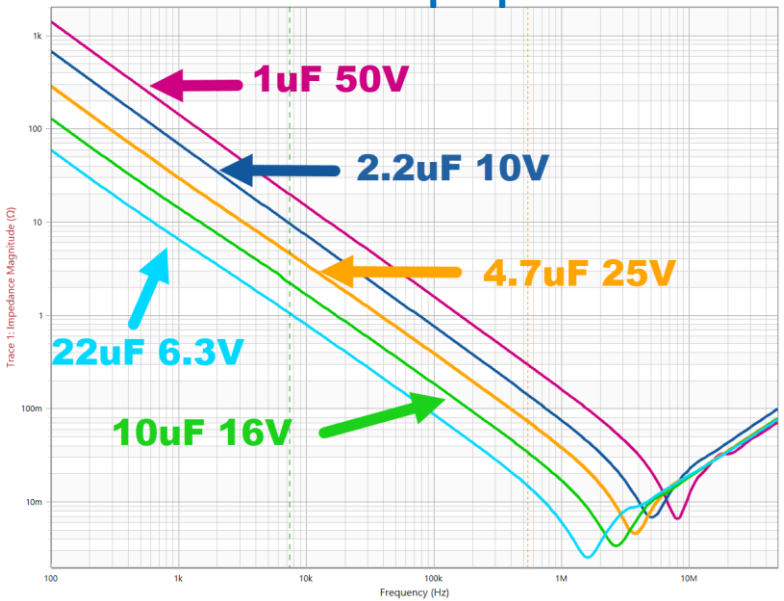
# Measurement-Based Modeling of the PDN Capacitors

- There is not an agreed-upon standard Capacitors models from vendors
- Every single capacitor used in this system was measured prior to use in PDN

## Large Cap Options



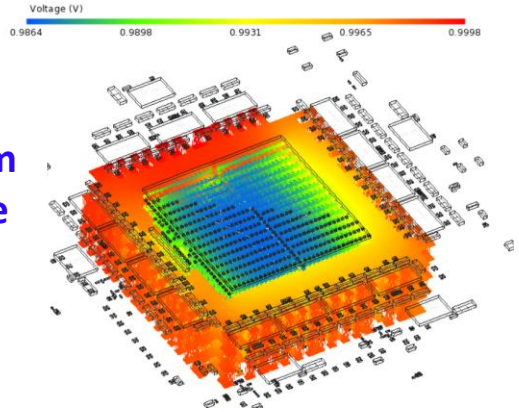

## Small Cap Options



# The Need for PCB EM Models

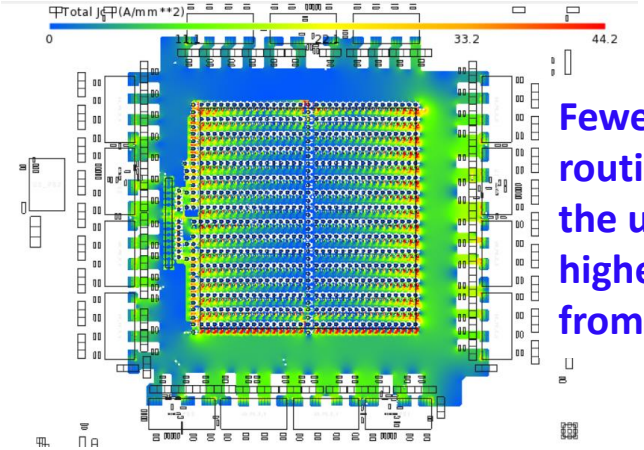
- Power delivery is AC not DC, and no matter how perfect the voltage regulator there is always some parasitic path impedance.

**Voltage IR Drop**




**Delta 10mV from outside to inside with 1000 Amps**

**Current Density**

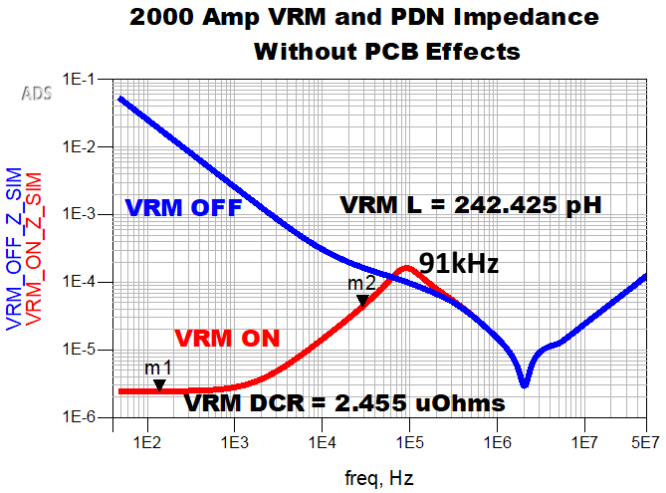



**Fewer VRMs and more routing perforations in the upper left lead to higher current flow from the lower right.**

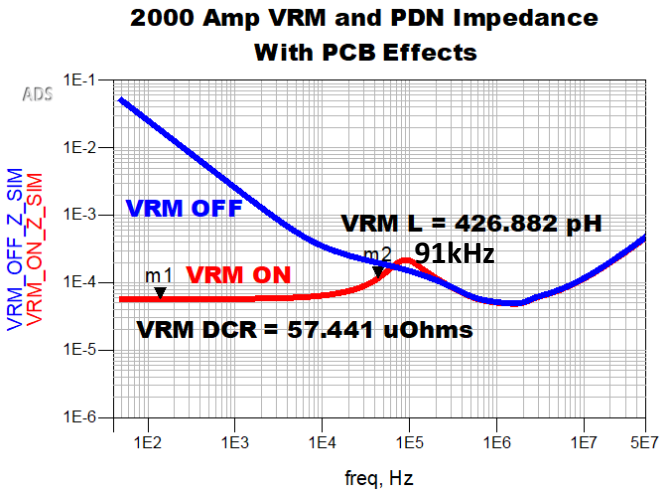
**Fast DC IR Drop EM simulations show minor symmetry differences in the PCB power distribution network and optimum placement for sense lines.**

# Digital Twin Accuracy Requires PCB EM Model

**Without PCB Effects**




**With PCB Effects**




$$C = \frac{L}{Z_o^{\,2}}$$

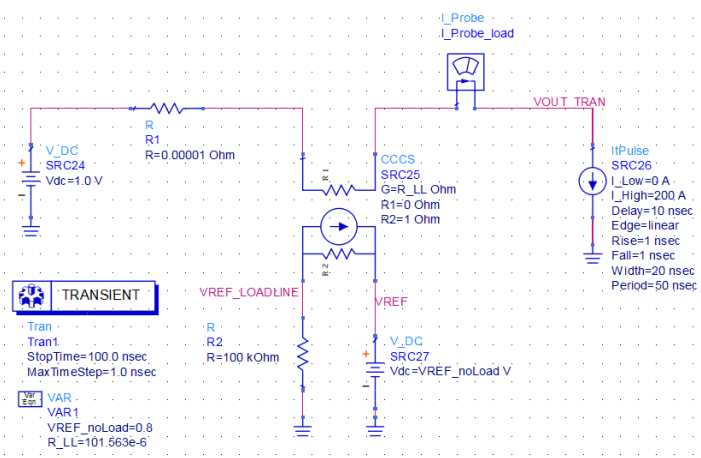
**22,000% Increase in path resistance! …And 76% increase in the inductance requires 76% more C!**

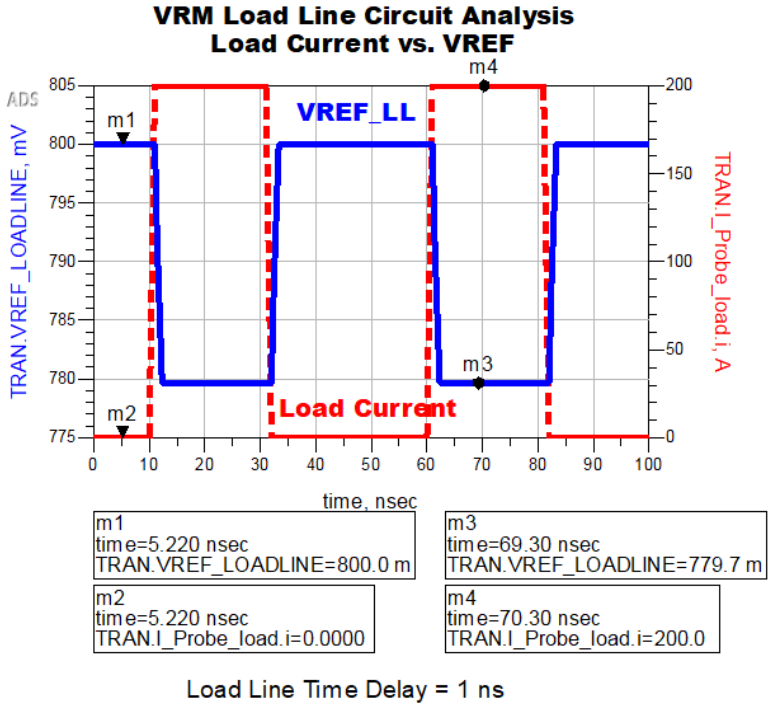
# Modeling of the VRM Load Line Sub-Model

- MPS provides gain parameters of load line within VRM.
- CCCS used to develop Load Line sub-model within VRM
- Load Line delay is adjustable

$$V_{REF\ LOAD\ LINE} = V_{REF} - I_{OUT} \cdot R_{Load\ Line}$$

*Where $R_{Load\ Line}$ is based off an EQ that is calculated based on register settings of the VRM




Load Line Time Delay = 1 ns

**As output current ↑ → $V_{REF\ LOAD\ LINE}$ ↓**

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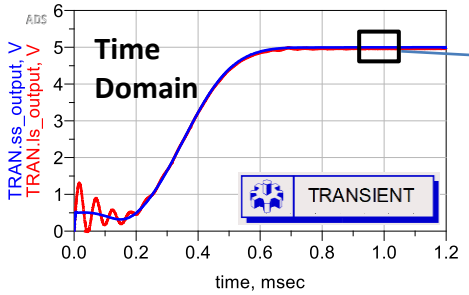
# Why use the Harmonic Balance Simulator with SSAM

- Fourier Theory says time domain waveforms are made up of frequency domain waveforms.
- Solving a circuit in the Frequency Domain can be much faster since it limits the frequencies and jumps to steady state.

**Transient** must reach steady state to measure ripple.

**50,000 time-steps!**

**Simulator Results**



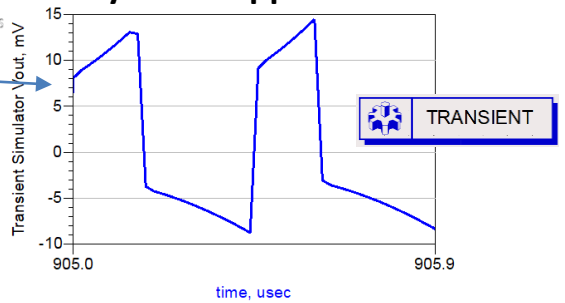

Time Domain

**Transient Sim**

Wait for Steady State

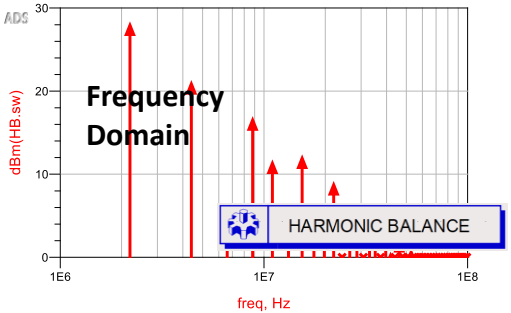
Minutes, Hours, **Days**

**Steady State Ripple vs. Time**




**Harmonic Balance** simulates harmonics of the switching frequency.

**Only 255 Frequencies for steady state ripple!**

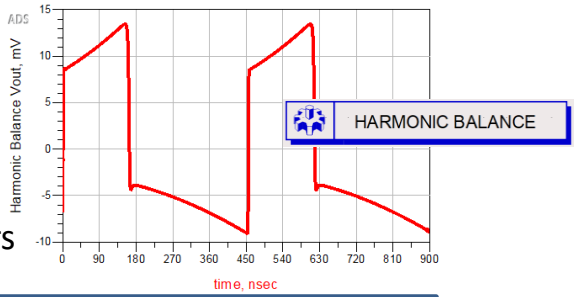



Frequency Domain

**Harmonic Balance Sim**

FFT jumps to Steady State

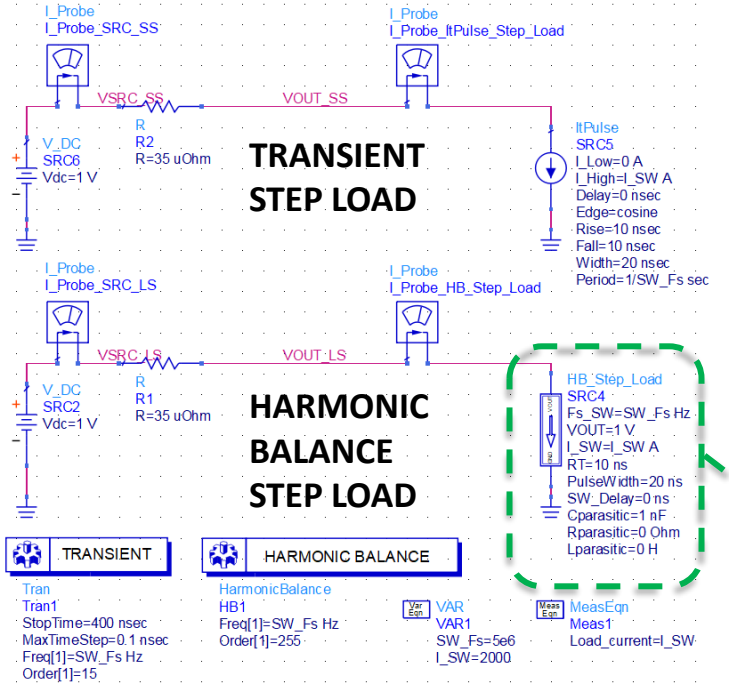
**Seconds**, Minutes, Hours

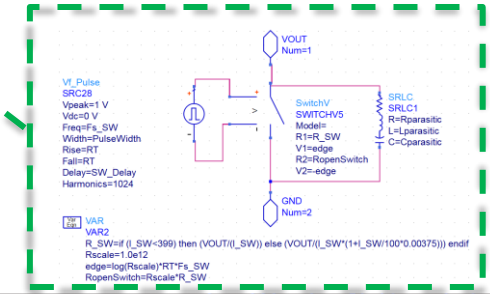


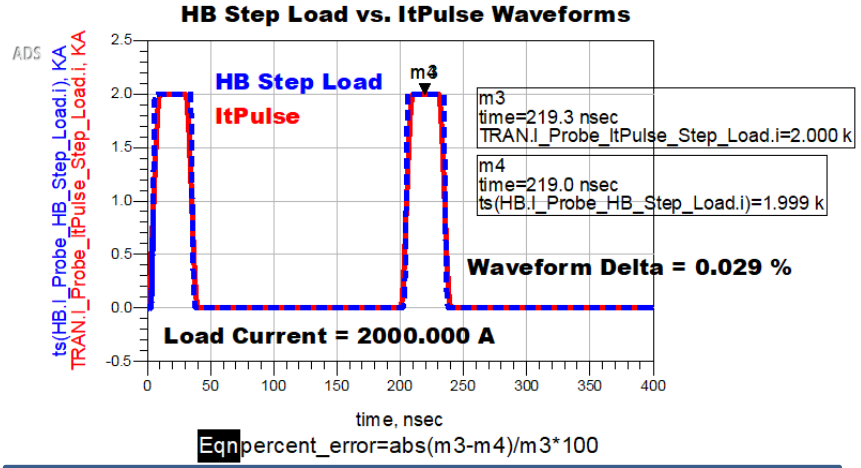

**Data shown is for one VRM, typical PCB design has dozens of VRMs**

# Harmonic Balance Simulation with the Step Load Model

- No step load model existed to support simulation with Harmonic Balance in ADS



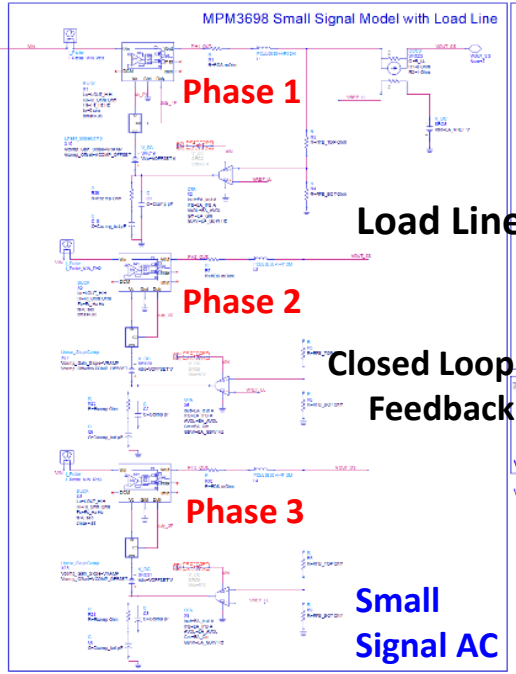



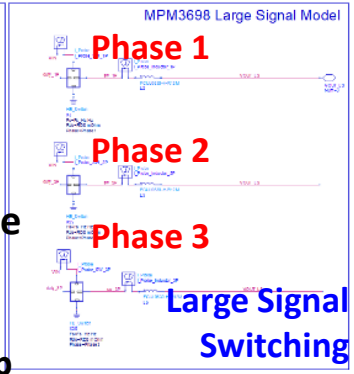




**HB step load model correlates very well to the Transient step load model**

# Creating the 55-Phase VRM Model with Load Line

## 5x MPM3698 – 3 phases

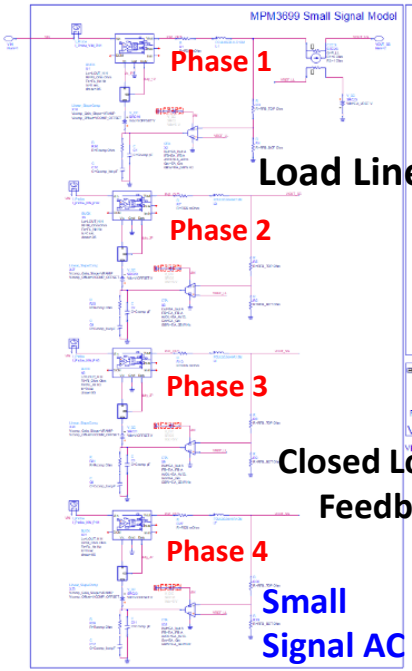


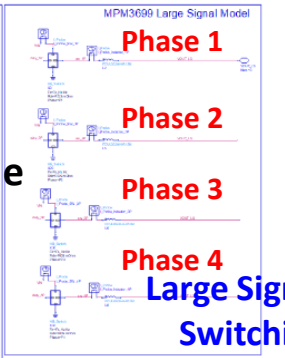





Harmonic Balance
Steady State Solution

## 10x MPM3699 – 4 phases

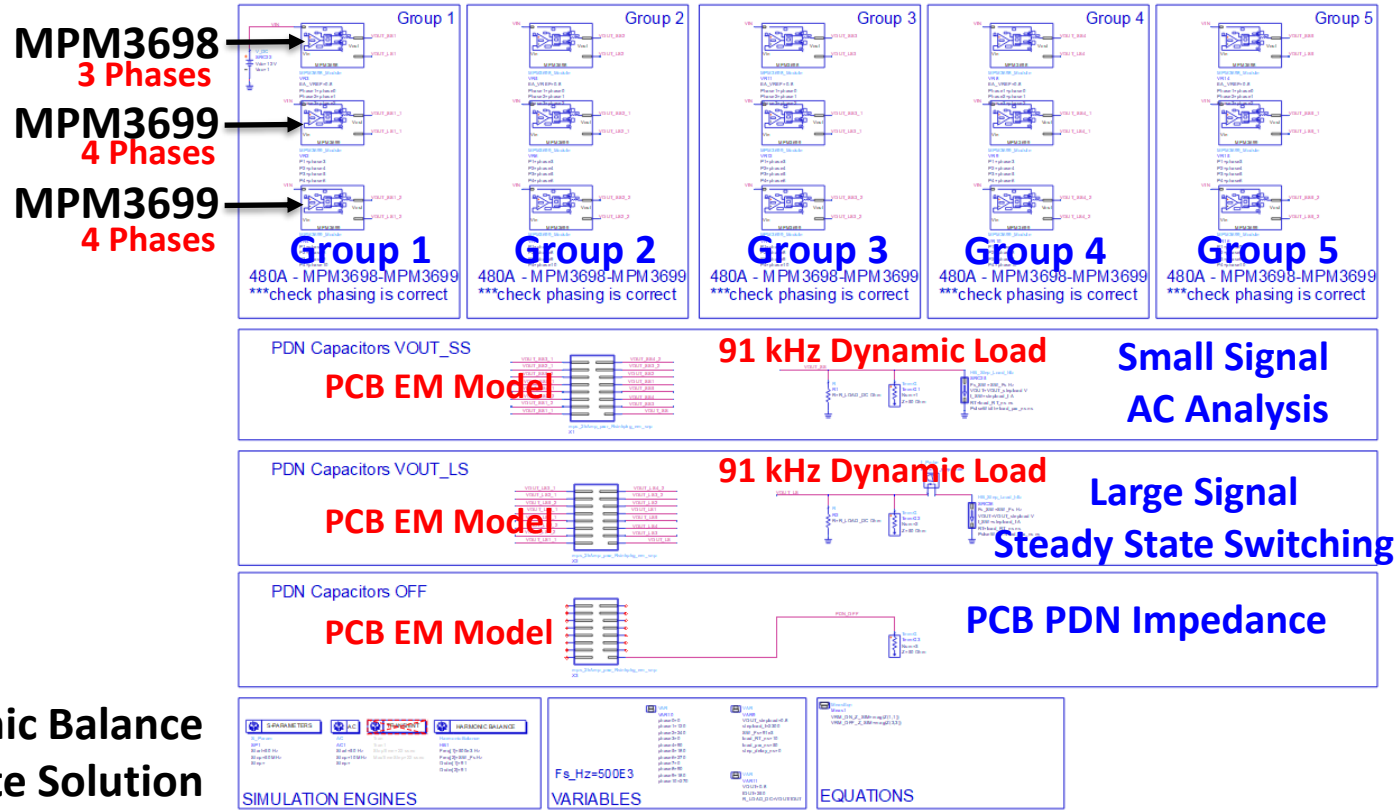




Sandler State-Space Average VRM Model was used for both the MPM3698 and MPM3699

# End-to-End 55 Phase VRM Digital Twin Model

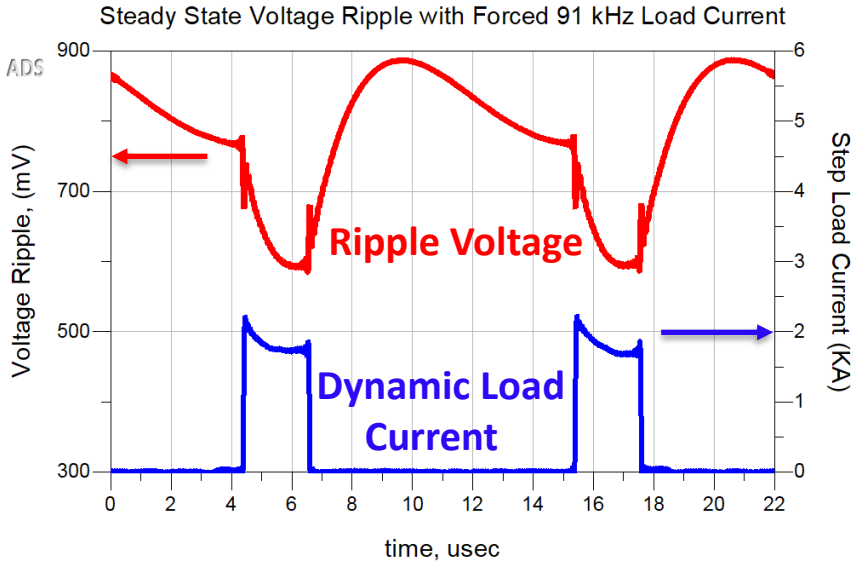


# End-to-End Digital Twin Simulations

- A complete system simulation model is created with accurate capacitor models, EM-extracted PCB effects, and a 2000A VRM model that was scaled by using 5 groups of MPM3698 and MPM3699 modules

**55 Phases at 500 kHz**
**Dynamic Load at 91 kHz**

**Steady State Harmonic Balance Results in 77s**



# Outline

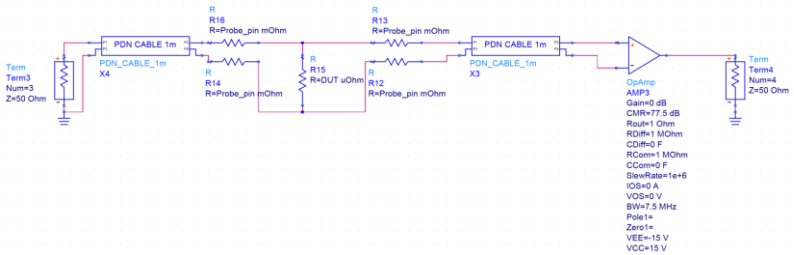
- Who and Why needs 2000 Amps?
- How do we build it
- Validation with Step Loader – How Hard is This?
- Measure-Based Modeling of the Components and PCB EM Models – Why Measure?
- End-to-end Digital Twin Simulations – Why Simulate?
- Measurement Case Study – It Works!

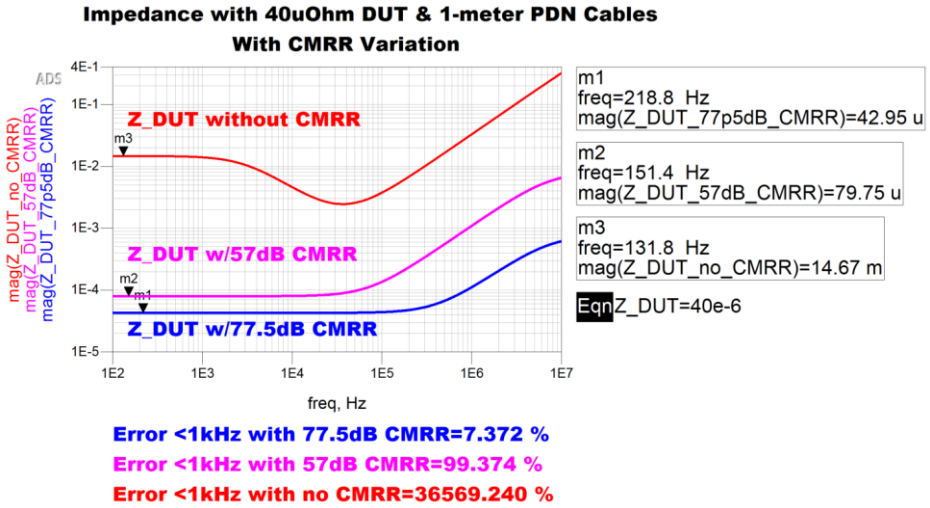
# Measurement Challenges to Measure 40 µΩ PDN

## With 2-port Probe

- Measuring a 2000 Amp PDN is **not intuitive** or even a trivial task!
- To measure 2000 A PDN (40 µΩ) a custom injector had to be created
- CMRR, RCABLE, & RPIN are the largest measurement error terms!

$$Z_{TGT} = \frac{dV}{di} = \frac{80mV}{2000A} = 40\ \mu\Omega$$

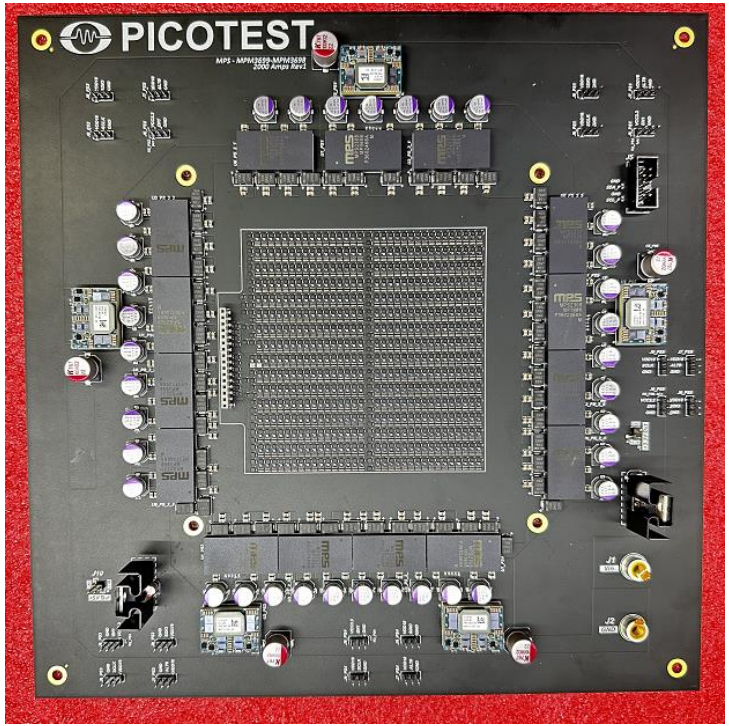


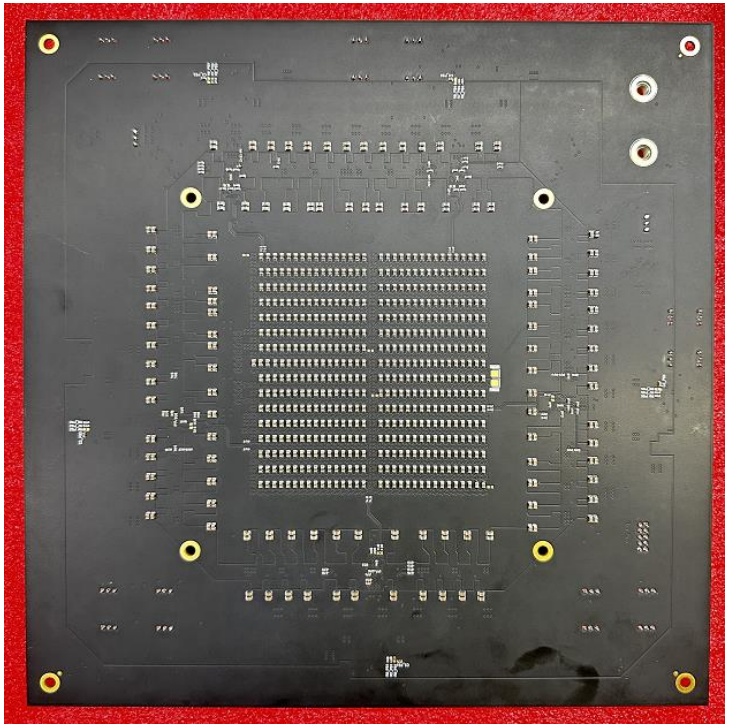

**Minimum CMRR needed to measure 40 µΩ with 2-port port is 77.5 dB for < 10% error**

# The 2000 Amp VRM and Step Load Design

- 15 MPS Modules
- 5 Groups
- 5x  48V to 12V
- 512 Load Cells
- 11 bit 50 MS/s



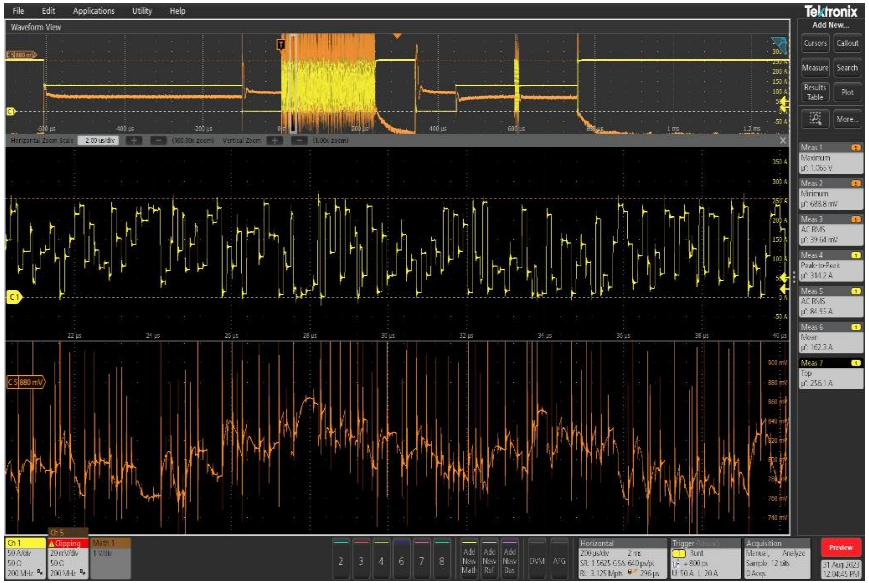

TOP



BOTTOM

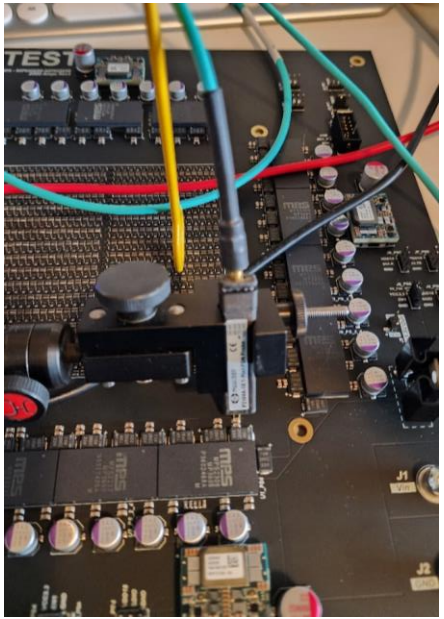
# Measurement Case Study – It Works!

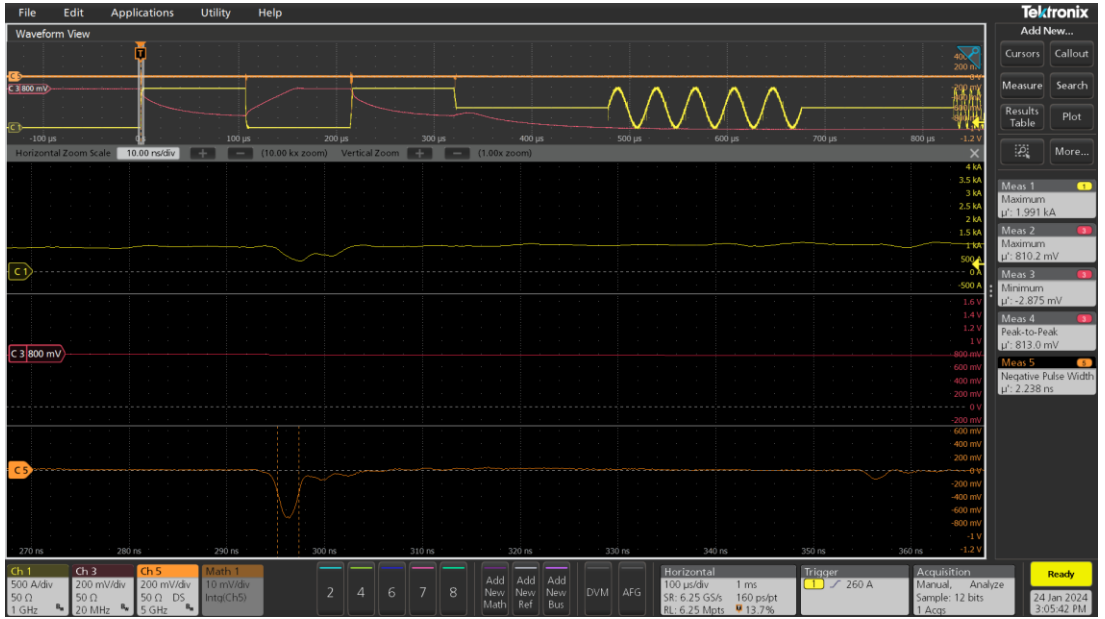
- The upper trace shows a demonstration of exponential rise and fall, linear rise and fall, high speed burst, sine and pseudo-random. The zoom window in the lower part of the screen shows the pseudorandom excitation




# Measurement Case Study – It Works!

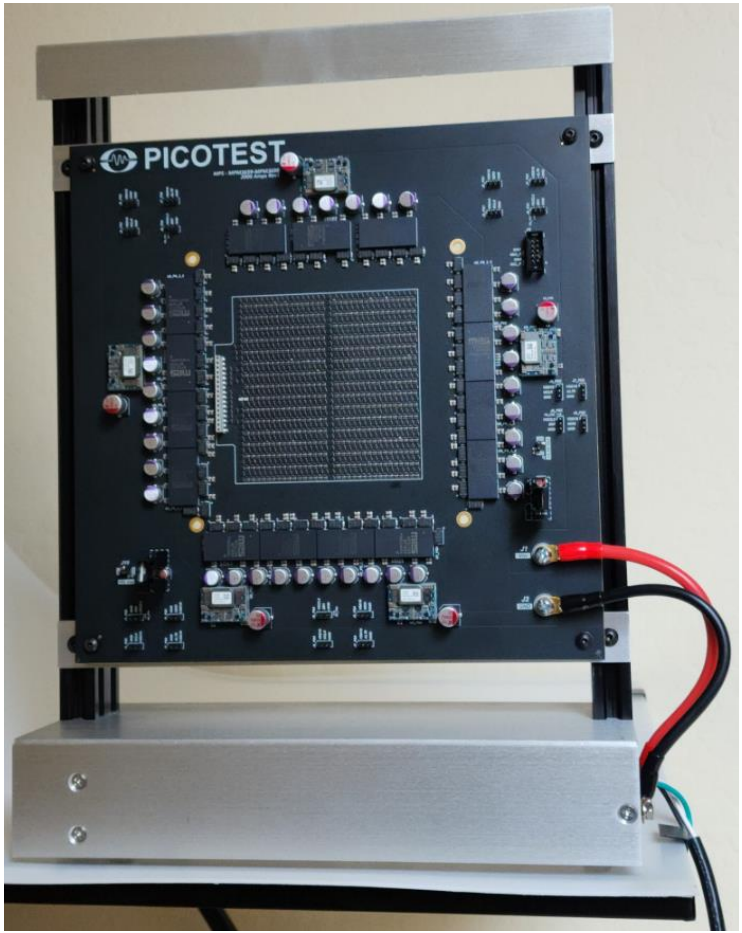
- Here is a screenshot of one of the decoupling caps using a near field probe.
- Integrating this will provide the current vs time.
- The total time is about 5ns, so the rise time is about 2.5-3ns. This depends mostly on the inductance of the loop through the load switch and decoupling capacitor.





# Conclusion and Summary

- 2000 Amp delivery is here to stay and even higher!
- Step Loader validation is the only way to get accurate large signal dynamic behavior
- Simulation accuracy requires measurement-based models for VRM SSAM and capacitors; PCB EM models
- Digital twin 55 phases, load-lines, dynamic load HB simulation in minutes
- Hardware measurements prove scalable 2000 Amp step load can be done!



# Thank you!

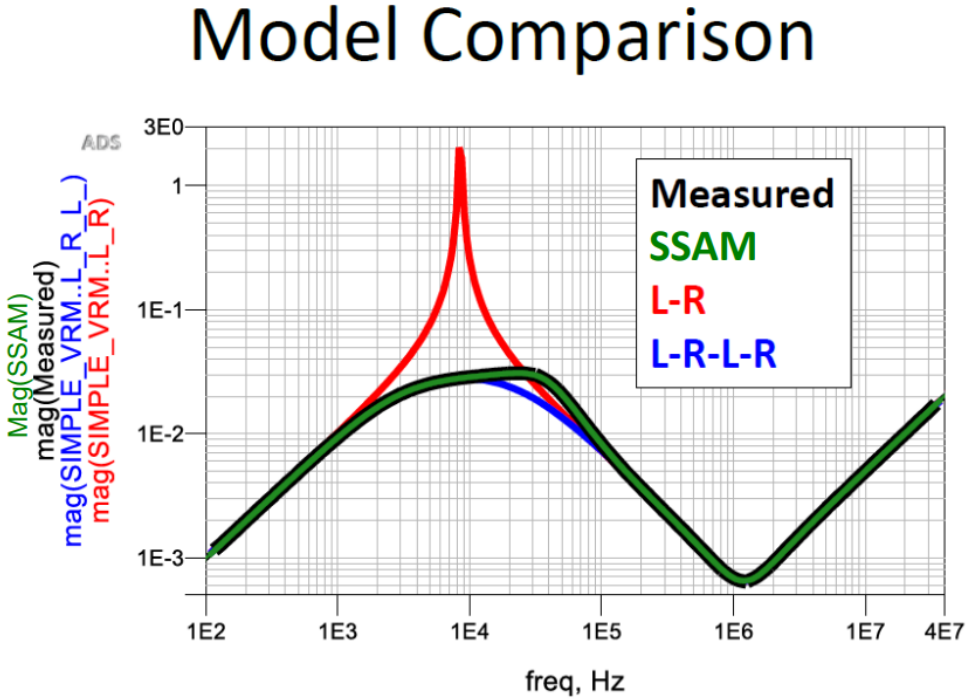
## QUESTIONS?

# References


1. Advantages of Constant-On-Time Control in DC/DC Converters - https://www.monolithicpower.com/en/advantages-of-constant-on-time-control-in-dc-dc-converters
2. Dannan, B., & Sandler, S. M. (2023, December). The Challenge of Measuring a 40 μΩ, 2000 Amp PDN With a 2-Port Probe: How Much CMRR is Needed? Extreme Measurement Blog. https://www.signalintegrityjournal.com/
3. Dannan, B., & Sandler, S. M. (2024, January). The Challenge of Measuring a 40 μΩ, 2000 Amp PDN With a 2-Port Probe: The Measurement Result. Extreme Measurement Blog. https://www.signalintegrityjournal.com/
4. S. Sandler, B. Dannan, H. Barnes, and C. Yots, “VRM Modeling and Stability Analysis for the Power Integrity Engineer”, DesignCon 2023.
5. ___

# Modeling the Source of the Power

- A poor fidelity State-Space Average Model is significantly better than a good R-L VRM model




S. Sandler, B. Dannan, H. Barnes, and C. Yots, "VRM Modeling and Stability Analysis for the Power Integrity Engineer", DesignCon 2023.