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# VRM Modeling and Stability Analysis for the Power Integrity Engineer

Steve Sandler, PICOTEST.com
steve@picotest.com

Ben Dannan, Northrop Grumman Mission Systems
benjamin.dannan@ngc.com

Heidi Barnes, Keysight Technologies
heidi_barnes@keysight.com

Christian Yots, Texas Instruments
yots@ti.com

## Abstract

In the world of power electronics, the focus is on the power supply, and the load is modeled as a simple resistor. In the world of power integrity, the focus is on the decoupling capacitors required for the digital load, and the power supply is modeled as a simple resistor in series with an inductor. In the real world, neither assumption solves the problem of simulating the power delivery ecosystem with switching power supply control loops, gigabit switching digital loads, and a PCB network of filtering and decoupling components. The challenge is how to simulate the Power Integrity ecosystem and include the feedback loop and switching noise of a switch mode power supply (SMPS) without waiting days for the simulation results.

The solution presented here uses control loop theory state space equations to create a behavioral model of an SMPS that allows for fast simulation. This Sandler State Space Average Model previously published [1] has the fidelity to include the dynamic control loop behavior for stability assessment, large signal and small signal noise ripple, and power supply rejection ratio. The model also works with the Non-Invasive Stability Measurement method to assess the control loop phase margin from simple output impedance data.

## Authors Biography

**Steve Sandler** has been involved with power system engineering for more than 40 years. Steve is the founder of PICOTEST.com, a company specializing in power integrity solutions, including measurement products, services, and training. He frequently lectures and leads workshops internationally on the topics of power, PDN, and distributed systems and is a Keysight-certified expert for EDA software.
Steve frequently writes articles and books related to the power supply and PDN performance, and his latest book, Power Integrity Using ADS, was published by Faraday Press in 2019. Steve founded AEi Systems, a well-established leader in worst-case circuit analysis and troubleshooting of high-reliability systems. (Phoenix, AZ) steve@picotest.com

**Heidi Barnes** is a Senior Application Engineer for High-Speed Digital applications in the PathWave EDA Group of Keysight Technologies. Her recent activities include the application of electromagnetic, transient, and frequency domain simulators to solve power integrity challenges. Author of over 20 papers on SI and PI and recipient of the DesignCon 2017 Engineer of the Year. Experience includes six years designing ATE test fixtures for Verigy, six years in RF/Microwave microcircuit packaging for Agilent Technologies, and ten years with NASA in the aerospace industry. Heidi graduated from the California Institute of Technology in 1986 with a bachelor's degree in electrical engineering. She has been with Keysight's EDA simulation group since 2012. (Santa Rosa, CA) heidi_barnes@keysight.com

**Benjamin Dannan** is a Technical Fellow and a Staff Digital Engineer at Northrop Grumman Mission Systems, with a multi-faceted background that includes a wide range of professional engineering and military experiences. He is a senior member of IEEE, with professional engineering experience that includes designing multiple systems and platforms to meet requirements for high-volume, high-reliability, harsh environments. He specializes in signal and power integrity, high-speed circuits, and multi-layered PCB design. He has multiple years of experience with EMC product development and certifications to support global product launches. Benjamin holds a certification in cybersecurity, has a BSEE from Purdue University, a Master of Engineering in Electrical Engineering from The Pennsylvania State University, and graduated from the USAF Undergraduate Combat Systems Officer training school with an aeronautical rating. Benjamin is a trained Electronic Warfare Officer in the USAF with deployments on the EC-130J Commando Solo in Afghanistan and Iraq, totaling 47 combat missions, and a trained USAF Cyber Operations Officer. In addition, he has co-authored multiple peer-reviewed journal publications. He received the prestigious DesignCon best paper award in 2020, given to authors leading as practitioners in semiconductor and electronic design. Lastly, Benjamin is also a Keysight Certified Expert in ADS. (Baltimore, MD) benjamin.dannan@ngc.com

**Christian Yots** is a Senior Applications Engineer at Texas Instruments in the Space Power team, focusing on DC-DC switching converters for space applications. Christian joined TI in 1993 after receiving a Bachelor of Science in Electrical Engineering (BSEE) from Auburn University. He earned a Master of Science in Electrical Engineering from the University of Texas at Arlington in 1998. His 29-year career at TI includes roles as IC process, product, test, characterization, systems, design, and applications engineer, developing ICs for many end equipment, including transceivers for cellular handsets and infrastructure, data converters for medical imaging, and power switchers for space applications. (Dallas, TX) yots@ti.com

## Introduction

In the real world of power delivery to high-speed digital loads, the power supply is not a simple series resistor and inductor, and the load is not a static resistor. Simulating the end-to-end power delivery ecosystem must include the switching power supply control loops, the gigabit switching digital loads, and the PCB network of filtering and decoupling components. The challenge is how to simulate this power delivery ecosystem with the feedback loop and switching noise of a switch mode power supply (SMPS) without waiting days for the simulation results.

The answer lies in using models with the appropriate level of fidelity for the task at hand. The series R-L model is too simple, making it difficult to assess the design of sense lines, large signal switching noise, and power supply noise rejection ratio. Full transistor-level models of all the power supply circuitry are too complicated for efficient simulation times and are often proprietary. The model with the appropriate level of fidelity for simulating the power integrity ecosystem is a behavioral model that characterizes the feedback loop and switching behavior and can be created from a few simple measurements. This paper will demonstrate how the measurement-based Sandler State-Space Average Model (SSAM) [1] provides a high level of power supply fidelity with very fast simulation times. The model uses well-published control loop theory state-space equations for switching power supplies [12] and supports AC, DC, time domain transient, or harmonic balance frequency domain simulators.

Learn how this simple SSAM model can quickly identify power rail decoupling resonances that are excited by the large signal switching noise ripple. Learn how the SSAM model can assess the trade-offs of current mode vs. voltage mode feedback to reduce noise on the power rail and improve the power supply rejection ratio (PSRR). The model also works with measurement techniques like the Sandler Non-Invasive Stability Measurement (NISM) to assess power supply stability using only the output impedance data. This stability algorithm is derived from the minor loop gain and is an accepted measurement method in the aerospace industry [14].

## Why Use a Sandler State-Space Model?

There is a significant gap in fidelity between the series R-L power supply model that is often found in power integrity simulations versus the detailed transistor-level SPICE model supplied by the vendor of the regulator. The R-L model does not provide dc-dc converter switching noise, there is no information on noise transfer PSRR, and it is a fixed model for all load levels. The vendor-provided SPICE model is often proprietary, requires long simulation times to reach a steady state, and may not have the desired accuracy for a user's application. Behavioral models like SIMPLIS are available but are not designed to run fast with electromagnetic (EM) extracted S-parameter models representing the power distribution network (PDN) and cannot support end-to-end simulation. The use of state-space average models for switched mode power supplies was started in the 1970s [12] and is an effective technique for averaging the switching behavior to get the small signal AC behavior of the switching power supply control loop

in the frequency domain. Solving for the small signal behavior enables one to use that load-dependent operational point to drive the large signal switching behavior. This is what the Sandler-developed SSAM model does and makes it possible to simulate PSRR, power rail ripple, input/output impedances, switch node pulse width modulation (PWM), regulator stability, etc., as shown in Figure 1.

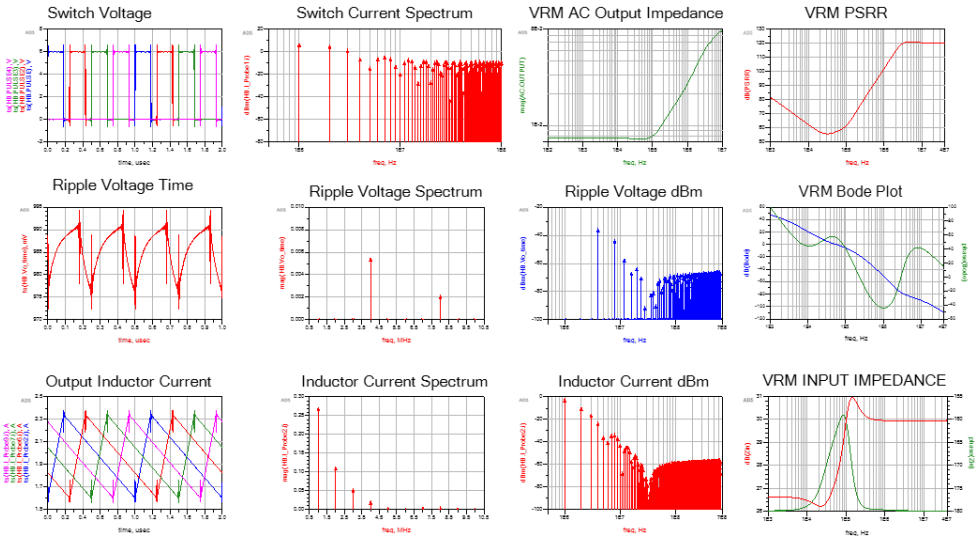



**Figure 1: A high fidelity state space average behavioral model of the switching power supply provides PSRR, power rail ripple, input/output impedances, switch node PWM, stability, etc.**

The SSAM is a behavioral model that simulates all noise sources going into and out of the switched mode power supply or voltage regulator module (VRM), as it is often called in the high-speed digital world, Figure 2. Network analysis on this 2-port system relates these noise sources to the frequency-dependent S-parameter models that characterize the VRM over frequency.

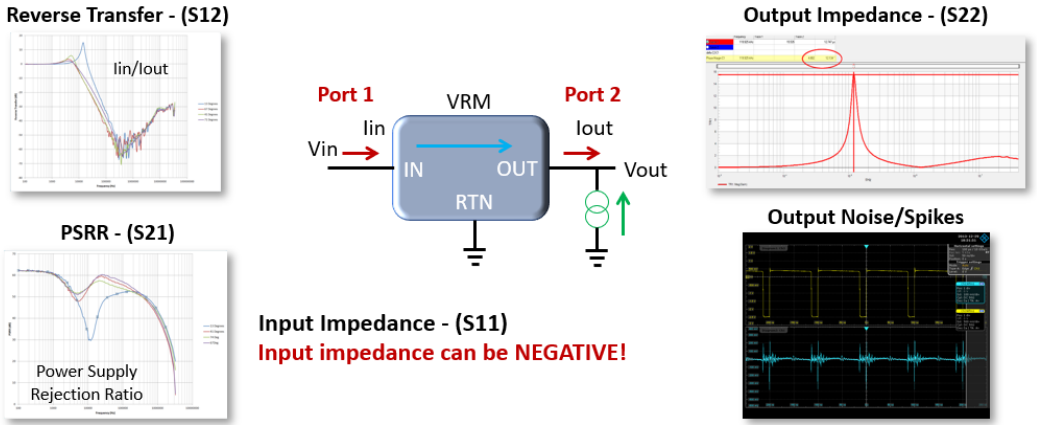



**Figure 2: A network analysis of the VRM 2 port system shows that all the noise sources can be characterized with the 2-port S-parameters.**

The model averages the power switch states to determine the behavior. Figure 3 shows the simplified circuits for the State 1 and State 2 conditions of the dc/dc converter with two switches. Minor modifications to the equations can be made for continuous

conduction mode (CCM) versus discontinuous conduction mode (DCM) and current mode vs. voltage mode, making it possible for the Sandler SSAM to support all of these modes and topologies in a universal model.

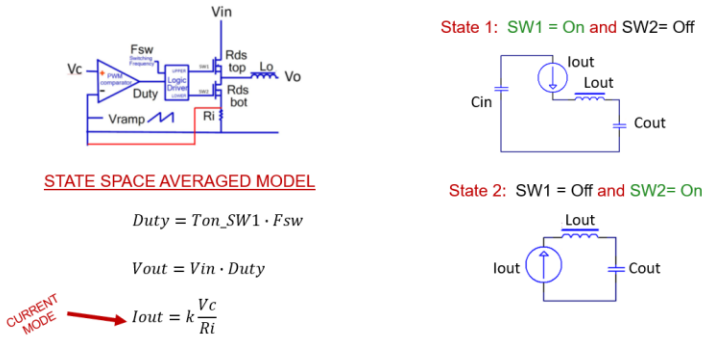



**Figure 3: State Space Average models take the average of the two states for the switches creating the PWM voltage that feeds the inductor and output capacitor.**

This SSAM accurately predicts the complete VRM performance, while simple lumped models have limited use. Figure 4 shows how the SSAM simulation results compare with measurements, while the R-L method results in a large resonance near 10 kHz. This resonance in the R-L model solution requires overestimating the bulk capacitance needed to reduce the resonance and ensure a stable load for the VRM control loop.

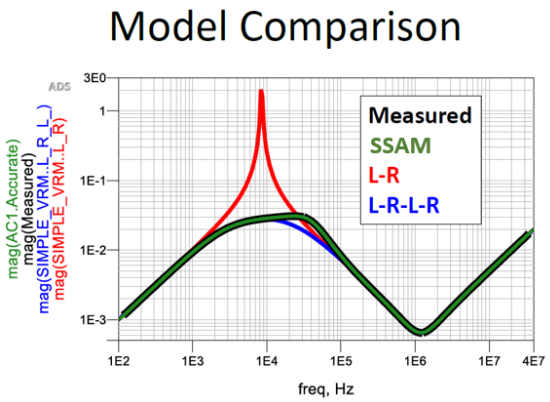



**Figure 4: Comparison of a measured VRM output impedance with the exact overlay of the accurate SSAM model vs. the oversimplified L-R model vs. a higher order L-R-L-R model.**

The L-R-L-R model gets closer to the measured behavior of the output impedance, but this is just one of the terms in our 2-port VRM system. Table 1 compares an ideal voltage source, an L-R model, a higher-order L-R-L-R model, and the high-fidelity Sandler SSAM [13]. The L-R model only models output impedance, and not very well, so it is often replaced with the higher order L-R-L-R model. However, this lumped model still only models the output impedance. It takes a higher fidelity SSAM model to provide the system behavior for the 2-port VRM. The table clearly shows the benefit of the SSAM over the other methods for accurately predicting all the noise sources and VRM behavior.

| | V Source | L-R | L-R-L-R | SSAM |
|---|---|---|---|---|
| PDN Impedance | INCORRECT RESULT | NOT WELL | REASONABLY | Y |
| Switching ripple | N | N | N | Y |
| PSRR/Transients | N | N | N | Y |
| Negative resistance | N | N | N | Y |
| Input switching current | N | N | N | Y |
| Control loop stability | N | N | N | Y |
| Turn on overshoot | N | N | N | Y |
| Remote sense | N | N | N | Y |

**Table 1: Comparison of VRM models. The ideal voltage source does not work for higher frequency behavior, the L-R is not as good as the L-R-L-R model, and only the Sandler SSAM behavioral model provides all of the VRM 2-port behavior.**

High-fidelity models provide valuable insights into the importance of different components, their optimum value, and the required tolerances to stay within the specified design margins. Figure 5 shows how parameters such as the output capacitor, input inductor, and load current can be swept with the Sandler SSAM to assess the impact on the VRM's behavior over frequency.

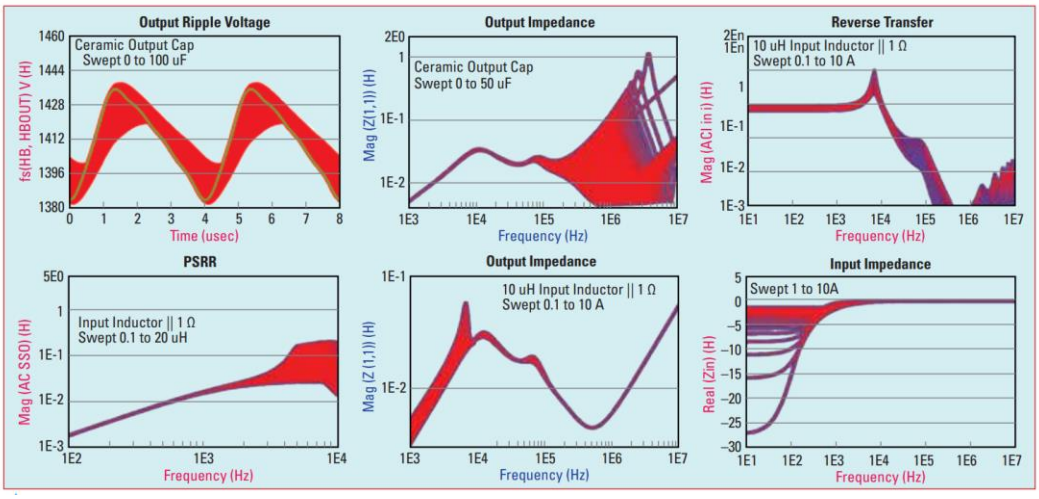



**Figure 5: Higher fidelity SSAM for the VRM makes it easy to find component sensitivities, optimize their values and assess tolerances to meet design margins.**

Even a best guess lower quality SSAM for the VRM behavior provides significantly better qualitative behavior than an R-L model for identifying critical components necessary for optimization and faster troubleshooting of power delivery failures.

The SSAM, like any model, has its limits. It assumes that one is operating the regulator at a switching frequency at least six times higher than the control loop bandwidth. Figure 6 uses audio susceptibility to compare the Sandler SSAM to the Dr. Ridley continuous time model [10], showing that in the desired bandwidth of control where the frequency is below 1/6$^{th}$ of the switching frequency, the SSAM matches well with the Ridley model. At higher frequencies, the Ridley model characterizes some of the higher-order modes. Keeping the VRM loop bandwidth less than 1/6$^{th}$ the switching frequency ensures a predictable behavior and avoids instabilities as one approaches the pulse width

modulation switching frequency. At frequencies above 1/6th the switching frequency, it is the job of the PDN decoupling capacitors to deliver power.

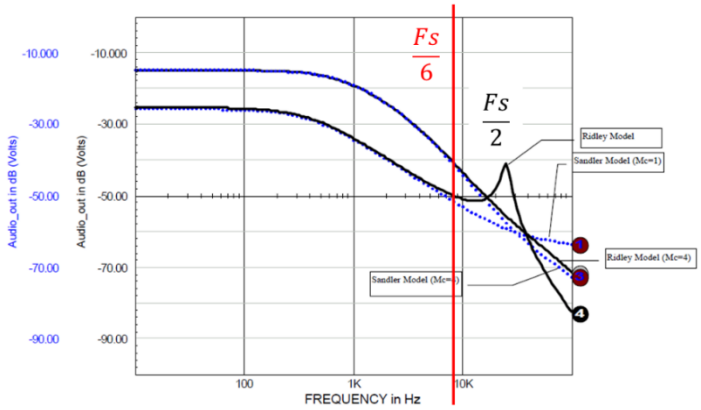



**Figure 6: Comparing the Sandler SSAM to the Ridley Model shows excellent agreement up to 1/6th of the switching frequency, which is the desired region of operation for the VRM.**

## Building a Sandler State-Space Model

The purpose of the Sandler SSAM is to capture the switching behavior of a PWM dc/dc converter and allow simulation in both the frequency and time domains. The state-space equations describe the small signal "plant" behavior. However, the plant, as depicted in Figure 7, needs to be fed a feedback signal to determine the control loop adjustments to maintain the output voltage under dynamic load conditions. Although it may look confusing to setup up the feedback loop with an error amplifier that feeds a ramp voltage to a comparator to adjust the duty cycle, in reality, one can start with the simplest of feedback models and add fidelity as needed to get a better correlation with measurement.

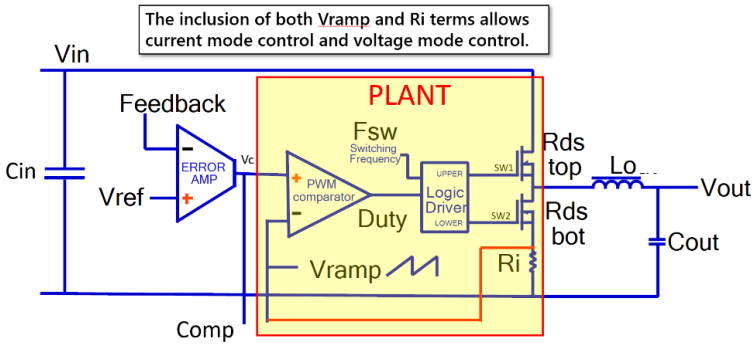



**Figure 7: Basic topology for the VRM behavioral model.**

Some fundamental topologies to consider are current mode versus voltage mode, continuous mode and discontinuous mode, and shunt versus series feedback compensation. Even if you are unsure of the topology, some of it will be self-determining; for example, in voltage mode, the Ri term is approximately zero and can be set to a very small value. The VRM switching frequency, output inductor value, output PDN, and input filtering are all set by design. Identifying other behaviors like $V_{ramp}$, Ri,

switch RDSon, and the Error Amplifier Av can be more challenging when VRM components are internal to a packaged design. This is when measurements are the only way to populate the behavioral model. Measurements are also an excellent way of confirming data sheet parameters and ensuring that the vendor-provided information is valid for the desired application. As an example, Figure 8 shows how some VRM components make it easy to measure SSAM model parameters like $V_{ramp}$.

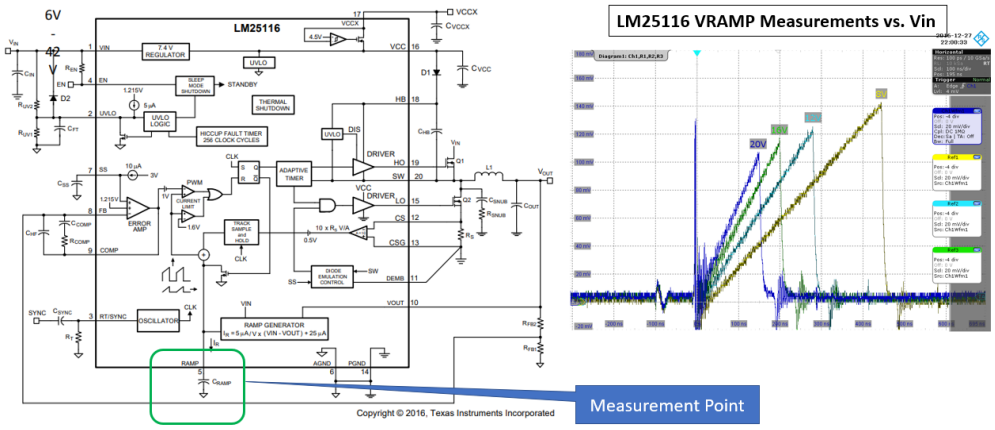
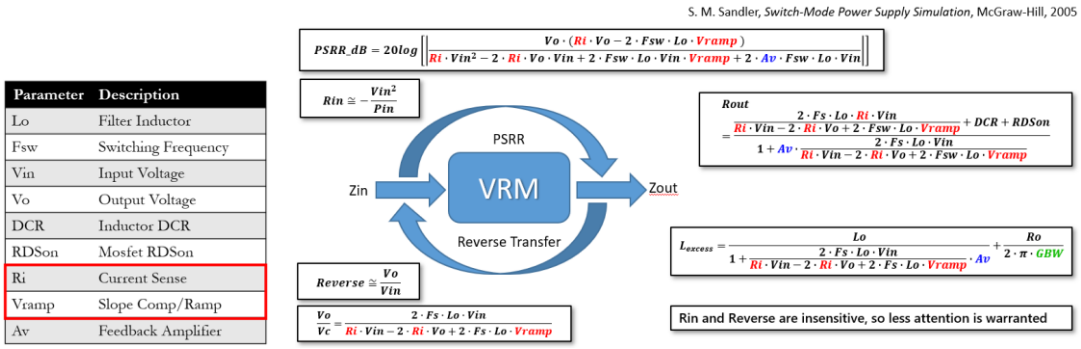



**Figure 8: A direct measurement of $V_{ramp}$ for populating the SSAM parameters is only available if the packaged VRM provides an access pin to the ramp voltage.**

## Measurements for a Sandler State-Space Model

The SSAM is a measurement-based behavioral model, so it is important to review which parameters are found in the data sheet and which are typically measured. The mathematics for the state-space model and required parameters are shown in Figure 9. While the state-space average model appears complicated, the mathematics behind it is embedded within the open-access model, and the user does not need to interact with them. The user only needs to provide a few parameters to the model.




| Parameter | Description |
|---|---|
| Lo | Filter Inductor |
| Fsw | Switching Frequency |
| Vin | Input Voltage |
| Vo | Output Voltage |
| DCR | Inductor DCR |
| RDSon | Mosfet RDSon |
| Ri | Current Sense |
| Vramp | Slope Comp/Ramp |
| Av | Feedback Amplifier |

**Figure 9: The primary state space equations that define the small signal plant behavior of the VRM. Two of the critical parameters, $V_{ramp}$ and Ri, are found with measurement.**

Most required parameters are known design parameters, such as the switching frequency, output filter inductance, and system-level requirements, such as input and output voltages. These data sheet and system-level parameters can generally be passed to the model. Although for the highest simulation to measurement accuracy, these parameters can also be measured. Figure 10 lists the required parameters for the SSAM and whether they are typically defined by system requirements or measured.

| Parameter | Description | Comments |
|---|---|---|
| Lo | Filter Inductor | We likely know this, but easily measured with a VNA |
| Fsw | Switching Frequency | We likely know this, but can easily measure it using an oscilloscope |
| Vin | Input Voltage | We should know this, since it is externally set, but can measure with a DMM |
| Vo | Output Voltage | We should know this, since it is externally set, but can measure with a DMM |
| DCR | Inductor DCR | We likely know this, but easily measured with a VNA (low impact) |
| RDSon | Mosfet RDSon | We likely know this, but easily measured with a VNA (low impact) |
| Ri | Current Sense | Often considered proprietary. This is equal to $\frac{\Delta Vcomp}{\Delta Io}$ |
| Vramp | Slope Comp/Ramp | Often considered proprietary |
| Av | Feedback Amplifier | Often external. Not always accessible, measurable with a VNA if COMP is available |
| Zcap | Output Cap Impedance | We might know this, but easily measured with a VNA* |

**Figure 10: List of required parameters for the Sandler SSAM measure-based model. Most parameters are known system-level requirements, but ones like $V_{ramp}$ are rarely in the data sheet and must be measured.**

Two parameters often not specified in the datasheet and can be challenging to obtain from the semiconductor manufacturer are the current sense resistance Ri and the slope compensation peak-to-peak ramp voltage, $V_{ramp}$. These two parameters are significant since they appear in every one of the model equations, as seen in Figure 9.

Obtaining the Ri term is simple if the device includes a COMP pin for external compensation. This is one of many reasons that it is recommended to only use devices with an external compensation pin.

Measuring the DC voltage at the COMP pin for a constant input voltage and varying load results in a graph like that shown in Figure 11. The slope of the line is the effective value of the resistance, while the zero current intercept is the internal offset voltage. This offset voltage is necessary since the internal feedback amplifier common mode range does not generally include ground, and this offset lifts the COMP pin voltage off ground.

Even if the manufacturer provides the data, it is still important to measure Ri. Take the Texas Instruments LM25116 regulator, for example. The LM25116 evaluation board from the manufacturer includes a visibly marked 10 milliohm current sense resistor on the PCB, and the current sense amplifier gain is specified as 10. This would make the effective current sense resistance 10 milliohms*10 or 100 milliohms. However, the measured data indicates 135 milliohms or 35% higher than anticipated, Figure 11. This is due to the added resistance of the PCB traces connecting this resistor to the feedback loop. The external COMP pin makes this a straightforward measurement, and it is highly recommended for increasing the model's fidelity.

You might wonder if this Ri term is necessary for a voltage mode converter. Theoretically, this would measure zero volts for a voltage mode converter, independent of load current, but this isn't always the case. It is simple to measure, so it is still worthwhile, particularly if you are not sure if the topology is voltage mode or current mode.

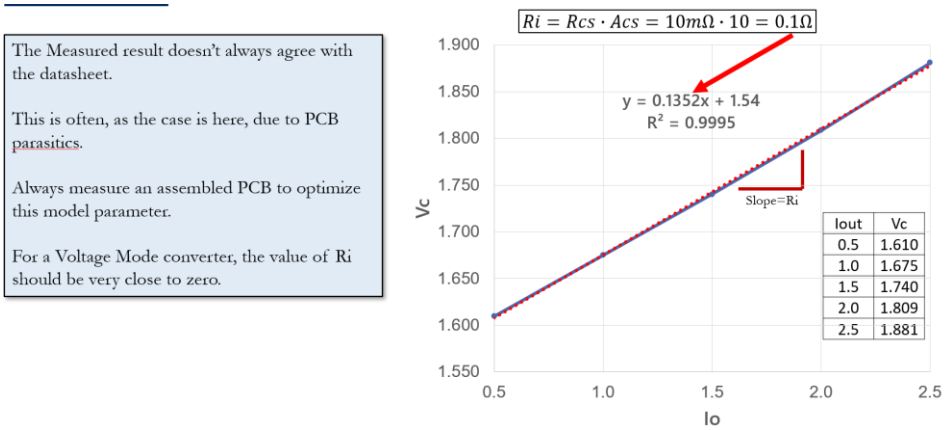



**Figure 11: Devices with an external COMP pin make it easy to measure Ri. Here we see that the LM21156 eval board has a data sheet value of Ri=0.1 Ohm, while the measured slope shows an actual value of Ri=0.135 Ohms, a 35% difference.**

The next term to be measured is $V_{ramp}$, the maximum peak-to-peak voltage of the ramp, or in most cases the peak voltage at 100% duty cycle. In some cases, though rare, the slope compensation ramp is externally available as a pin on the VRM's IC package for user adjustment. This makes it very easy to measure $V_{ramp}$ at different input voltages, as shown in the Figure 12, with an oscilloscope for the LM25116 switching regulator. If this information is directly measurable, you can likely use it confidently.

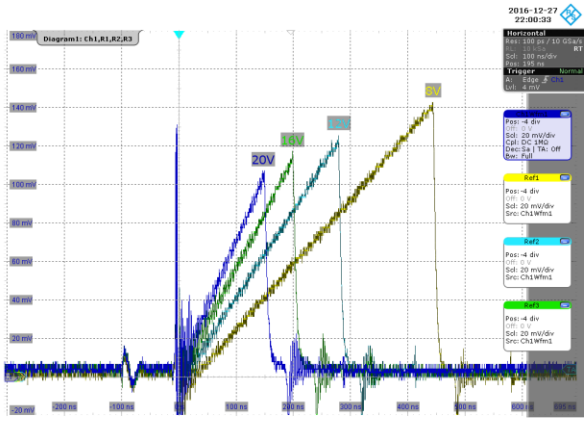



**Figure 12 - The LM25116 regulator has an external pin for adjustment of $V_{ramp}$, making it easy to directly measure $V_{ramp}$ vs. Vin on an oscilloscope.**

In most cases, where the $V_{ramp}$ is not accessible for measurement, it can be determined indirectly by measuring a VRM parameter that is a function of $V_{ramp}$. The equations shown in Figure 9 show that almost all converter characteristics are dependent on Ri and

$V_{ramp}$. In particular, the power supply rejection ratio (PSRR) of the converter is the most sensitive to $V_{ramp}$. Note that this equation also includes the control loop gain, Av, which can easily dominate the measurement. Ideally, the PSRR is measured in the open loop state by fixing the feedback voltage. Setting the feedback voltage to force open loop operation is relatively simple if the device includes a COMP pin for external compensation. Simply attach a fixed voltage at the COMP pin to operate open loop. Another good reason for selecting devices with an external COMP pin.

However, one must be careful to apply the correct voltage for the selected fixed load. Here is an example of the step-by-step procedure. Connect a Line Injector for the PSRR measurement, and then operate the VRM converter at the desired input voltage and resistive load current. Record the DC voltage at the comp pin. Connect a DC power supply with this voltage directly to the COMP pin. The converter will then operate at the desired operating point but open loop. The open loop plant gain can then be directly measured in this open loop state, using any PSRR setup such as the one shown in Figure 13 with the Picotest J2120 Line Injector.

**Warning:** *PSRR is a small signal ac measurement, DO NOT change the load current or the input voltage in this open loop condition, as the output voltage will also change, and it is possible to damage the converter.*

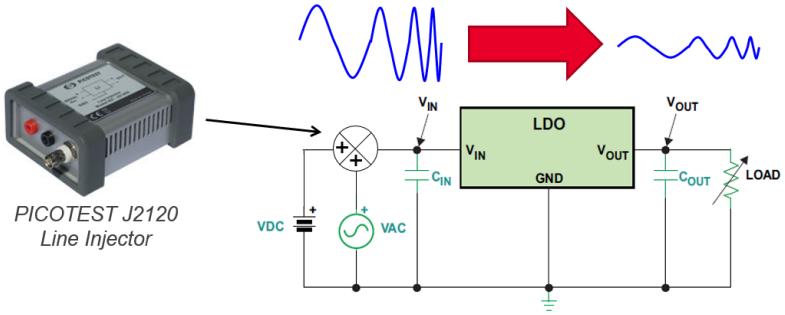



**Figure 13: Basic PSRR measurement setup with Line injector at Vin for Vac small signal noise injection for determining Vout/Vin.**

Our goal is to obtain the PSRR at low frequency, where the response is flat. We are also interested in the PSRR phase. This is because the PSRR is a second-order equation, so there are two solutions. We want to be sure to choose the correct one.

$V_{ramp}$ can then be directly calculated with the PSRR equation and the measured Ri term, or even easier, one can tune the $V_{ramp}$ parameter in the SSAM model until the PSRR results at low-frequency match with the open loop measurement. Don't forget to run the model in the open loop mode with the fixed feedback voltage by adding this to the simulation model.

The best way to demonstrate this process of populating the parameters for a high-fidelity Sandler SSAM model of a VRM is to walk through a real-world case study.

## TPS7H4003 VRM Modeling Example

In selecting an example test case to show how to build a Sandler SSAM VRM model and test its fidelity, it is important to select an industry that requires high reliability with low noise ripple. Space applications have some of the most stringent requirements for components as well as system-level design reliability.

Space applications can be grouped into two types. One is the radiation-hardened electronics that are used in harsher applications where they can experience single-event upsets (SEU). The other is the less expensive radiation-tolerant electronics that are targeting most of the new space applications that provide internet access and mobile telephony. These new applications include Amazon's Project Kuiper, SpaceX's Starlink constellation, and Iridium. These new satellite constellations operate in low-earth orbit (LEO) or about 99 to 1,200 miles up. The typical mission profile for LEO applications is, on average, around five years with total radiation exposure equal to 10 – 30 krad(SI), which means electronics packages can use the less expensive radiation-tolerant RT plastic [9]. The growing need for RT electronics for LEO applications is the reason for selecting the TPS7H4003 regulator for a VRM modeling case study.


**Figure 14 – Low earth orbit (LEO) vs. geosynchronous equatorial orbit (GEO) [6]**

The Texas Instruments TPS7H4003 is a radiation-tolerant, 7-V, 18A synchronous buck converter with integrated MOSFETs manufactured by Texas Instruments. The manufacturer provides an evaluation board shown in Figure 15 that demonstrates this device's operation and simplifies collecting the measurements needed for populating a TPS7H4003 SSAM model.


**Figure 15 – Depiction of TPS7H4003EVM Evaluation Board**

Figure 16 shows the test bench setup with the TPS7H4003EVM board for extracting the Ri data. An adjustable electronic load is used to set the output current while the input

voltage is maintained at 5V on the input. A digital voltmeter records the COMP pin voltage while the electronic load provides the load current.

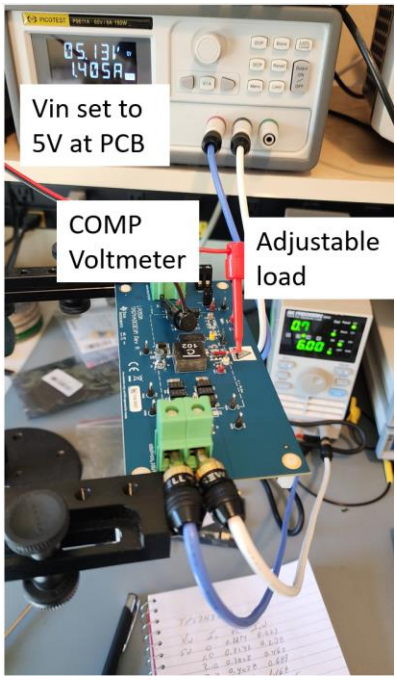



**Figure 16 – TPS7H4003 Ri measurement setup on the eval board. Ri is the slope of the voltage at the COMP pin vs. Iout.**

The manually collected data is plotted, see Figure 17, and a linear trendline is used to curve fit the data. The result indicates an Ri value of 26.6 milliohms, and the offset voltage is 327.8mV. The offset voltage is the value when the load is zero, and the DC offset includes the SSAM voltage compensation network. Note the regression coefficient of 0.9999, indicating a nearly perfect fit to the straight-line equation.

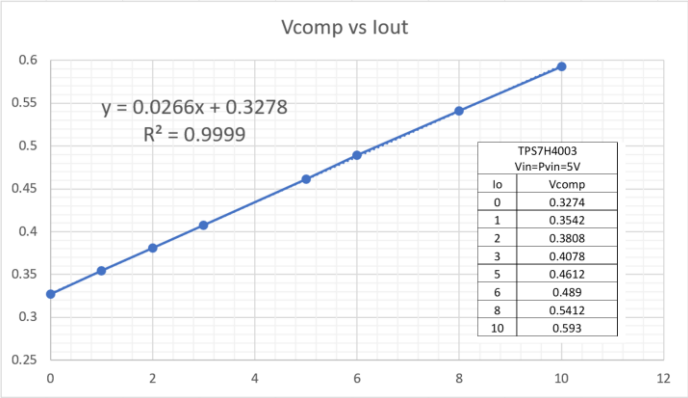



**Figure 17 – TPS7H4003 Ri measurement result – Ri is the 26.6 mohm slope for the voltage at the COMP pin vs. Iout and has a linear regression curve fit of 0.9999 for this extracted value.**

Figure 18 shows the evaluation board configured for the PSRR measurement. In this case, Vin and the load are held constant, and the COMP pin is also set to a fixed voltage

to allow for an open loop measurement of Vout/Vin with small signal frequency excitation at Vin with the J2120A Line Injector.

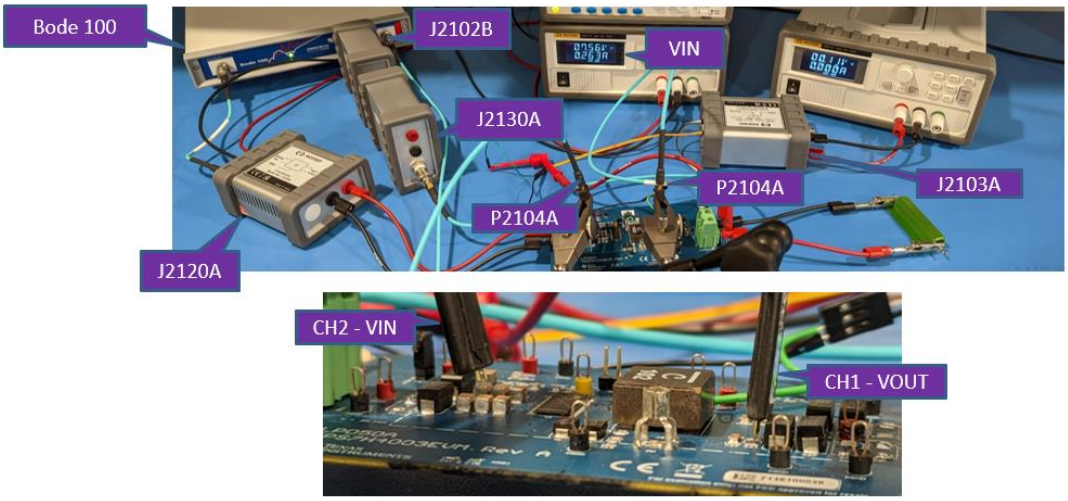



**Figure 18 – TPS7H4004 PSRR Measurement Setup with 1.6A Load and a fixed voltage at the COMP pin for performing the Open Loop measurement of Vout/Vin with small signal excitation at Vin.**

The resulting PSRR measurement, shown in Figure 19, indicates a low-frequency PSRR (Vout/Vin) of -22 dB and a phase of 175 degrees at 61 Hz for a 1 Amp load. In this case the gain data (in dB) is negative, but it is also an acceptable practice to plot the inverse (Vin/Vout) as a positive dB value for PSRR. This data is used to indirectly determine the ramp amplitude for the model by tuning the $V_{ramp}$ parameter to match simulated PSRR to the measured PSSR data for the SSAM VRM model.

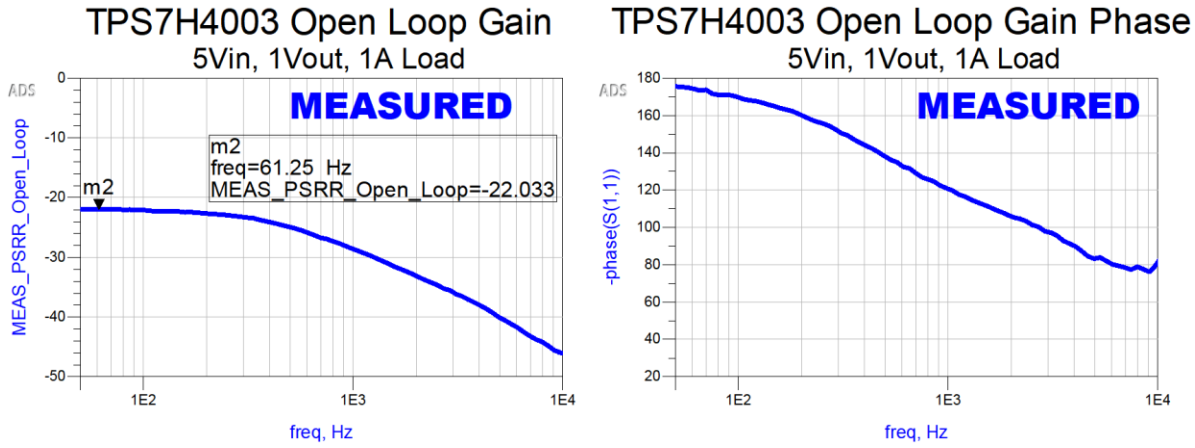



**Figure 19: TPS7H4003 Open Loop PSRR measured results shows a magnitude of -22 dB, graph on the left, and a phase of 175 degrees, graph on the right, at 61 Hz with a 1 Amp load.**

## Tuning and Verifying the TPS7H4003 SSAM

The next step is to start entering the parameters into the SSAM for the TPS7H4003. The parameters set by design are:

| | |
|---|---|
| Vin = 5 V | :Input Voltage |
| Vout = 1 V | :Output Voltage |
| Fsw = 500 kHz | :Switching Frequency |
| Lo = 1 uH | :Output Inductor |
| RDS = 17 mohms | :Upper and Lower Switch Resistance in the On State, not critical |
| Rtop = 10 kOhms | :Feedback top resistor in the resistive divider that sets output V |
| Rbot = 15.4 kOhms | :Feedback bottom resistor that sets the output V |
| Vref = 0.605 V | :Feedback internal reference voltage |
| Gm = 1800 uS | :Error Amplifier Transconductance (gm) |

The TPS7H4003 data sheet provides Ri in its inverse form, as the 40 S transconductance from the COMP pin to Iswitch, as shown in Figure 20. Inverting this gives a typical Ri value of 25 mohms, which is not far from the 26.6 mohms measured and within the specified tolerances. It is still essential to use the measured value when building the model so that it is the exact value used when measuring and simulating $V_{ramp}$. The TPS7H4003 also includes the ability to adjust $V_{ramp}$ with an external resistor on the RSC pin. The equation for calculating the RSC resistor includes the Slope Compensation (SC), which can then be used to calculate $V_{ramp}$, shown in Equation (1). The TPS7H4003 evaluation board specifies RSC=953k ohms; putting this into the data sheet equation demonstrated by Equation (1) and solving for SC results in 1.1 A/uS. Multiplying SC by the switching period for a 100% duty cycle, as shown in Equation (2), results in a 2.2A/100% duty cycle. From there, $V_{ramp}$ can be calculated by multiplying $SC_{\text{per duty cycle}}$ by Ri as shown in Equation (3), which results in a $V_{ramp}$ of 0.055V.

| | | | | | | |
|---|---|---|---|---|---|---|
| COMP to Iswitch gm[3] | COMP = 0.5 V | –55°C | 28 | 38 | 49 | S |
| | | 25°C | 29 | 40 | 50 | |
| | | 125°C | 30 | 41 | 52 | |

**Figure 20 – TPS7H4003 Datasheet COMP pin to Iswitch Gm**

$$RSC = \frac{24000}{f_{sw}} + \frac{1040}{SC} - 30 \quad (1)$$

$$SC_{per\ duty\ cycle} = SC \cdot SW_{period} = 1.1A/us \cdot 2us = 2.2A/100\%\ duty\ cycle \quad (2)$$

$$V_{ramp} = SC \cdot R_i = 2.2A \cdot 25m\Omega = 0.055V \quad (3)$$

The data sheet parameter values are entered into the model along with the measured Ri and DC COMP Offset Voltage. The data sheet calculated $V_{ramp}$ of 0.055 V was a best guess, so the next step is to run the model in an open loop configuration to match the PSRR measurement and then tune $V_{ramp}$ until simulated and measured open loop gain for the plant match at low frequency. To run the model in the open loop configuration that was used for the measurement, a DC voltage source of 686mV is attached to the COMP net and the output load is set at a fixed resistor value of 1 ohm as shown in Figure 21.

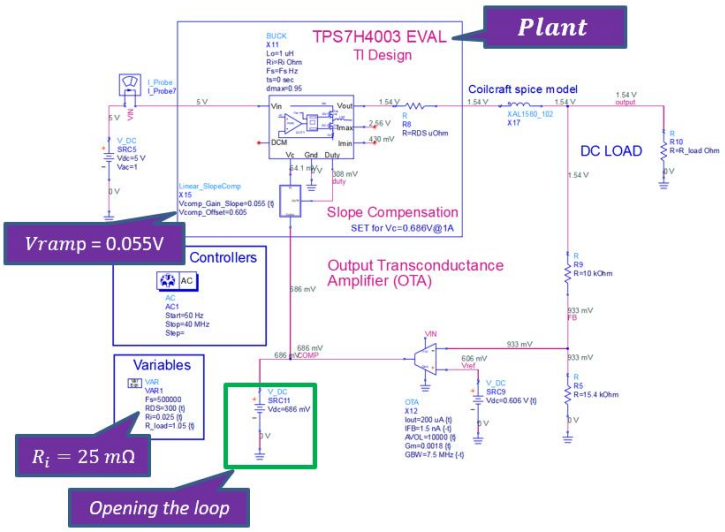



**Figure 21 – Schematic Depiction of TPS7H4003 Open Loop Gain with a fixed 0.686V at the COMP**

When entering the parameters and running the simulation for the first time, it helps to use a feature that annotates the DC voltages at all the nodes so that one can quickly check if there are any errors in values resulting in unrealistic voltage levels. If the model is operating correctly the 1 Volt AC results for 100 Hz to 10 MHz sweep can be plotted, as shown in Figure 22. The open loop gain data is plotted in dB magnitude for Vout/Vin and is one of the plant performance characteristics most sensitive to $V_{ramp}$ and Ri.

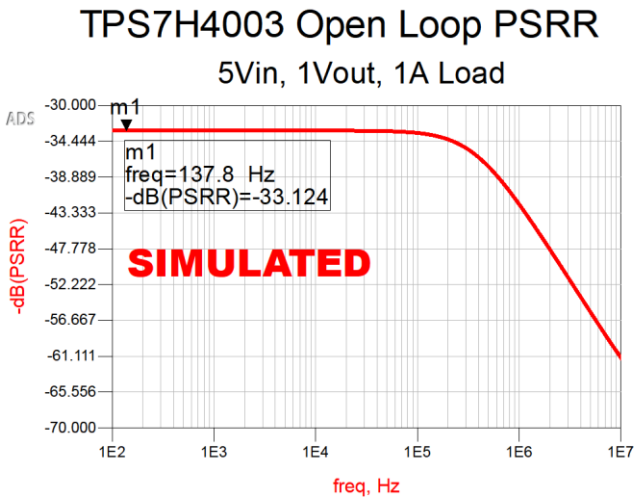



**Figure 22 – TPS7H4003 Plant Open Loop Gain Result**

The next step is to compare the simulated open loop plant gain with the measured data and tune the model's $V_{comp}$_Gain_Slope term for $V_{ramp}$. The open loop plant gain is measured on a network analyzer, so the data can be brought in as a 1-port S-parameter model to be evaluated over the same frequency range as the simulation, as shown in Figure 23.

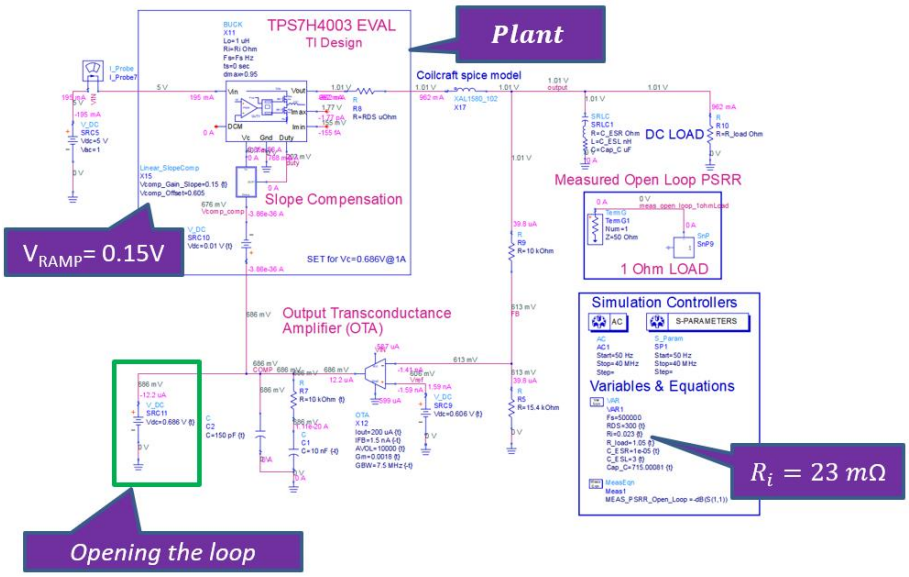



**Figure 23 – Schematic TPS7H4003 Open Loop Tuned to match Measurement**

The tuned $V_{ramp}$ value is 0.15 Volts and results in a very good simulation to measurement agreement for the open loop plant gain at the lower frequencies as shown in Figure 24. The measurement fixture and cables often limit the higher frequency accuracy of the measured data, so it is best to focus on the accuracy in the kHz and below range.

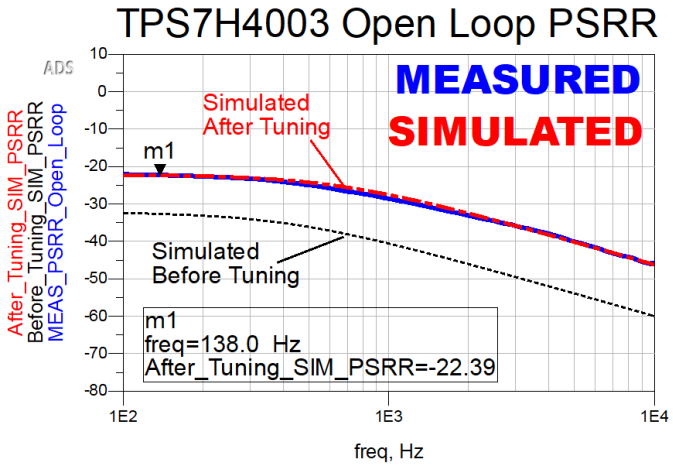



**Figure 24 – PSRR Open Loop Measurement vs. Tuned Simulation Results**

Output impedance is primarily a function of Ri and also sensitive to $V_{ramp}$, so an extra check on the model's accuracy can also be performed by comparing measured output impedance to simulated output impedance. When tuning to output impedance, it is important to ensure that one has accurate output inductor and bulk capacitor models. To first order, the PDN load that the VRM sees is the large bulk capacitor, and a series RLC model can be used to approximate this behavior.

## Test Case: Using the TPS7H4003 Model to Design for Stability

Once the model has been completed and simulation to measurement for PSRR and output impedance match reasonably well, one can explore all the different performance characteristics. One very important characteristic is to ensure that the power supply operation is stable and that there are no resonances in the system. Another key performance metric is voltage ripple on the power rail, such as the DC/DC converter switching noise. The Sandler SSAM is a two-part model, the state-space equations solve the small signal AC response to the PDN load to determine the duty cycle over time, and then in parallel, the model provides duty cycle information to drive upper and lower switch models, attached to the PDN load, to get the large signal switching noise, Figure 25.

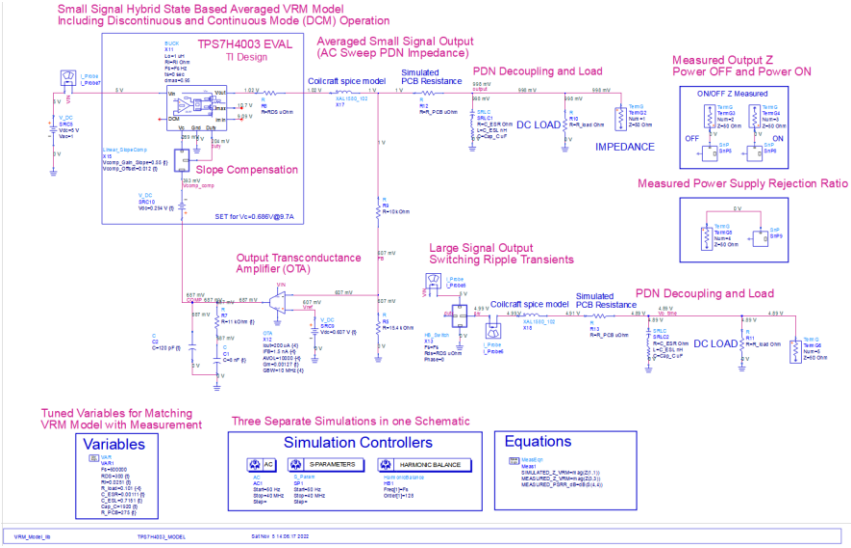



**Figure 25 – TPS7H4003 State-Space Average Model without PCB Effects**

Initially, this is simulated with a simple first-order series RLC model for the PCB PDN and a resistor load. The switch model can be simulated in the time domain, but a SPICE type transient simulation requires start up time for the circuit to settle, resulting in very long simulation times. A faster way is to use the Fourier based Harmonic Balance simulation engine which simulates the circuit at the fundamental switching frequency and enough harmonics to allow conversion to the time domain using Fourier Theory, Figure 26. This technique results in the steady state solution and can be significantly faster.

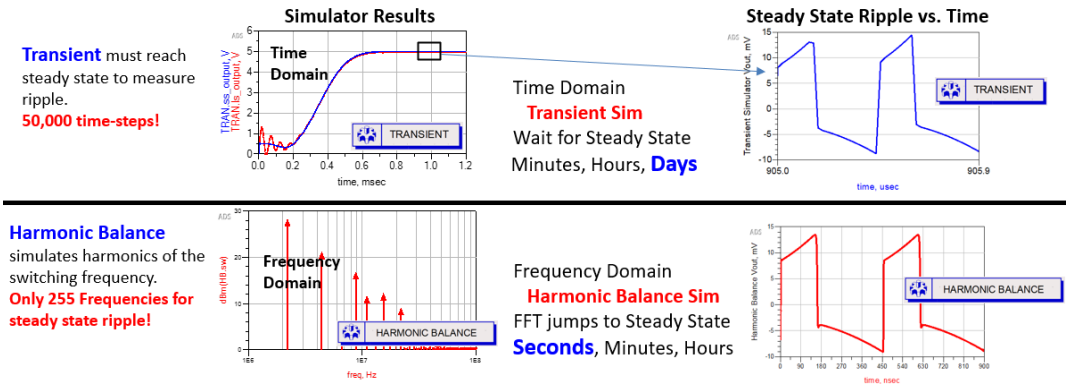



**Figure 26: Harmonic Balance in the frequency domain is a faster way of getting the time domain steady state ripple.**

The full model simulates the AC, S-parameter, and HB simulators in less than a minute to provide a full set of characteristics for the switching regulator power delivery system.

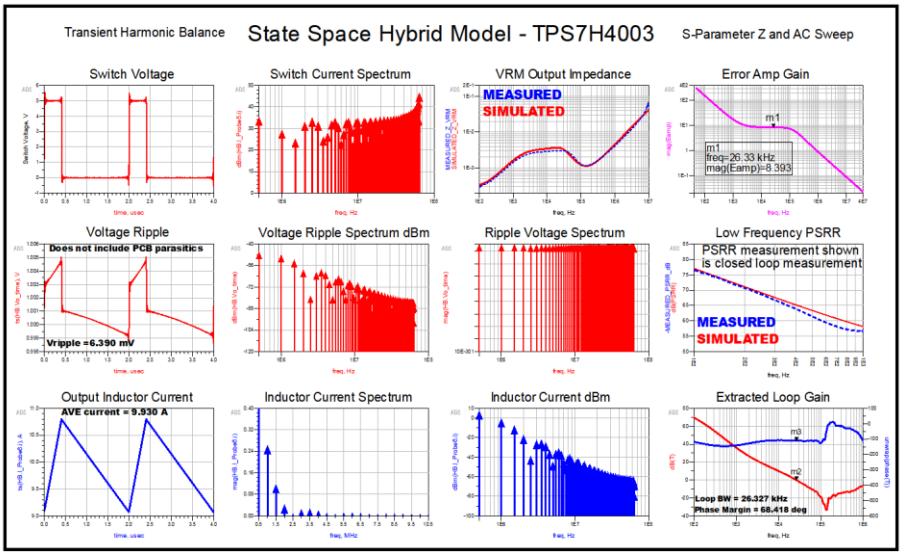



**Figure 27 - TPS7H4003 State-Space Average Model Results without PCB Effects**

The ultimate test is to compare the output voltage ripple on the power rail to measurement. Since impedance is very dependent on location, this also means that the voltage ripple is very sensitive to where it is measured. Making sure to measure and simulate at the same point is critical for correlating power rail voltage ripple simulation to measurement.

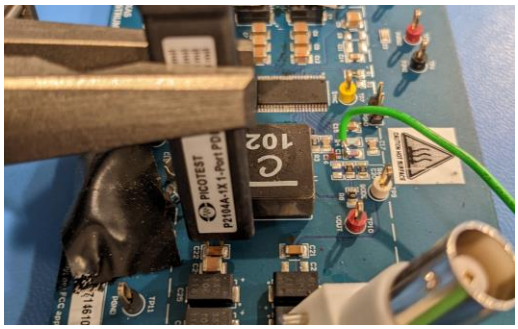



**Figure 28 – Measuring the TPS7H4003 output voltage ripple near the inductor at C22.**

Measuring at a capacitor near the output inductor, Figure 28, of the VRM results in the dc/dc converter switching noise shown in Figure 29. When comparing the voltage ripple result shown in Figure 27 to the actual measurement shown in Figure 29, an additional 1 MHz resonance is observed that is not seen during simulation.

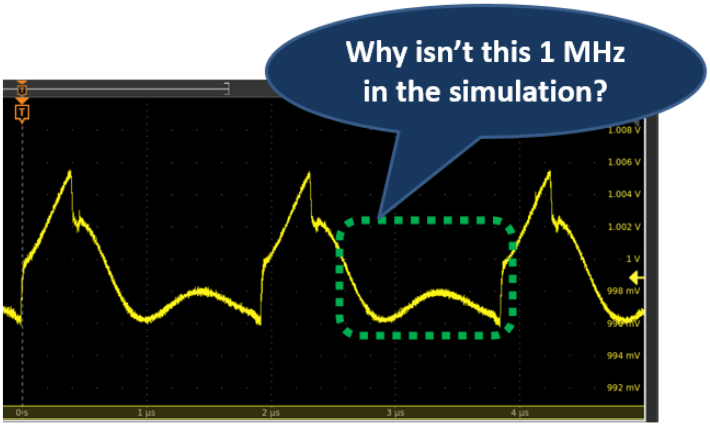



**Figure 29 – Measured voltage ripple on the TPS7H4003 EVAL PCB with load.**

As a next step to determine where the 1 MHz resonance seen in measurement is coming from a higher fidelity PCB model is added. The PCB switch and Vout nodes were both extracted using PIPro from 0 Hz to 1 GHz. A depiction of the PCB extracted Vout node is shown in Figure 30. After both EM extracted models were checked for causality and passivity, they were added into the SSAM Figure 31.

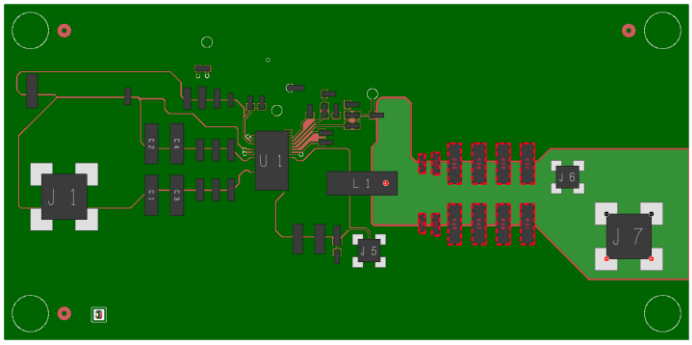



**Figure 30 – EM Extraction Artwork for TPS7H4003 EVAL PCB**

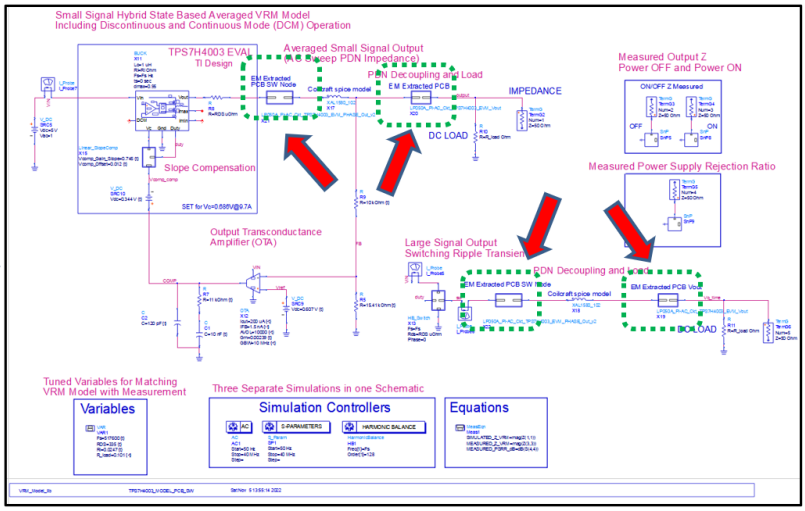



**Figure 31 - TPS7H4003 State-Space Average Model with EM extracted PCB effects.**

By including the PCB effects into the SSAM the voltage ripple response, shown in Figure 32, now looks identical to the measurement shown in Figure 29. This emphasizes the importance of including the PCB effects with the VRM design to ensure the model is correct.

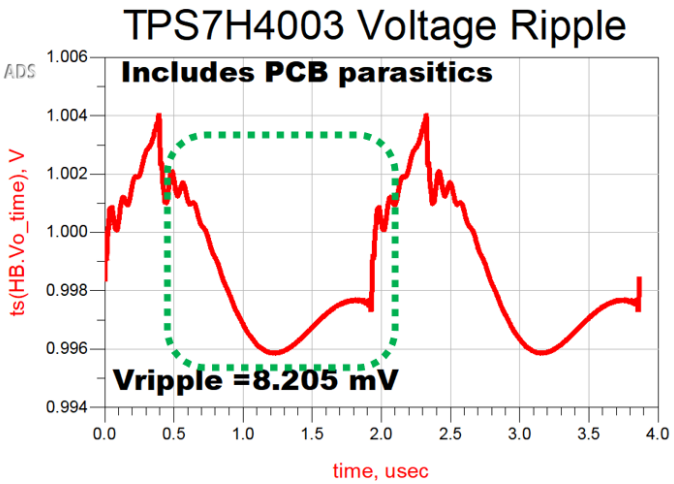



**Figure 32 – The TPS7H4003 SSAM simulated output voltage ripple with 9.8A load and including the EM extracted PCB model from the layout artwork now shows the 1 MHz resonance.**

The question now remains as to what is causing the 1 MHz resonance in the output voltage ripple? To identify the answer to that question, the first step is to re-visit the output impedance measurement. The 2-port measurement setup for the VRM output impedance is shown by Figure 33 and Figure 34.

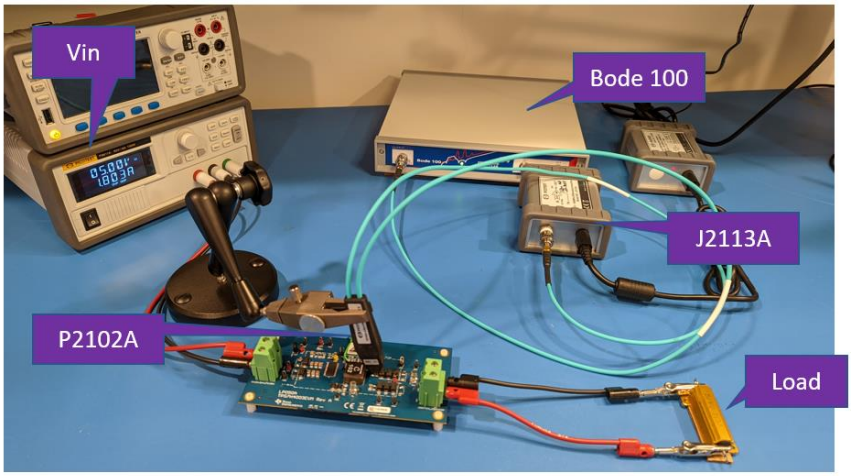



**Figure 33 – 2-Port Shunt output impedance measurement setup using a Bode 100 network analyzer.**

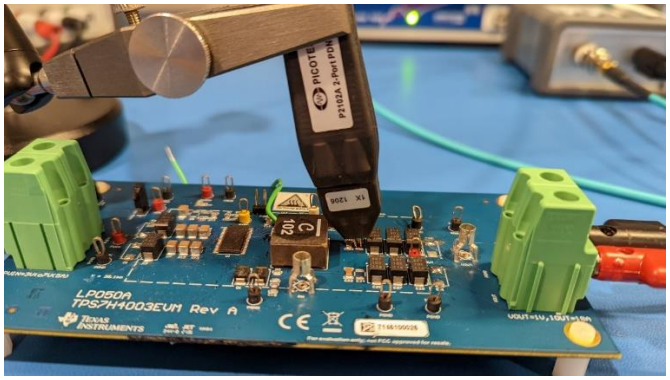



**Figure 34 – TPS7H4003 output impedance measurement at C23.**

When reviewing the output impedance measurement shown by Figure 35, a 1 MHz resonance is observed as indicated by marker m9. To further understand what the root cause of this 1 MHz resonance is, that is also seen in the impedance, a power plane resonance was extracted on the PCB artwork in PIPro with a 1 MHz excitation frequency as shown by Figure 36.

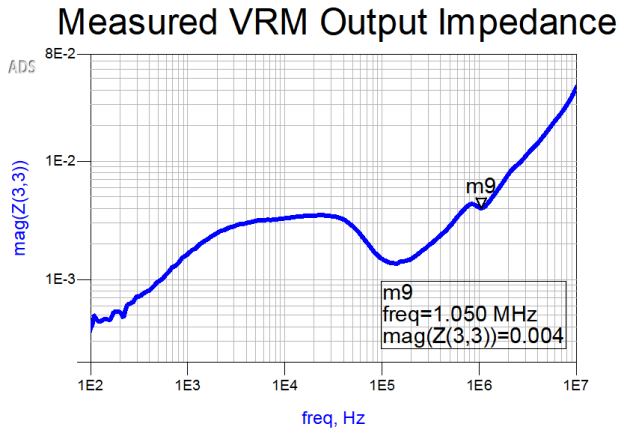



**Figure 35 – TPS7H4003 output impedance vs. frequency measurement with a 9.8A load.**

Further analysis of the power plane resonance shows multiple capacitors are resonating at 1 MHz on the PCB. The EM simulation includes both 22uF capacitors, and interestingly the eval board PCB has the upper C23 capacitor removed indicating that maybe this 22uF capacitor was previously found to be a problem. One can also consider that the 330uF capacitors are too large to resonate at 1 MHz. The 0.1uF capacitors at C21 and C22 are too small to resonate at 1 MHz. Through process of elimination, that leaves the remaining 22uF capacitor installed at the bottom C24 location. The impedance of the vendor spice model for the 22uF capacitor is plotted and shown by Figure 37, where a strong correlation is made that shows this capacitor is the root cause of the 1 MHz resonance.

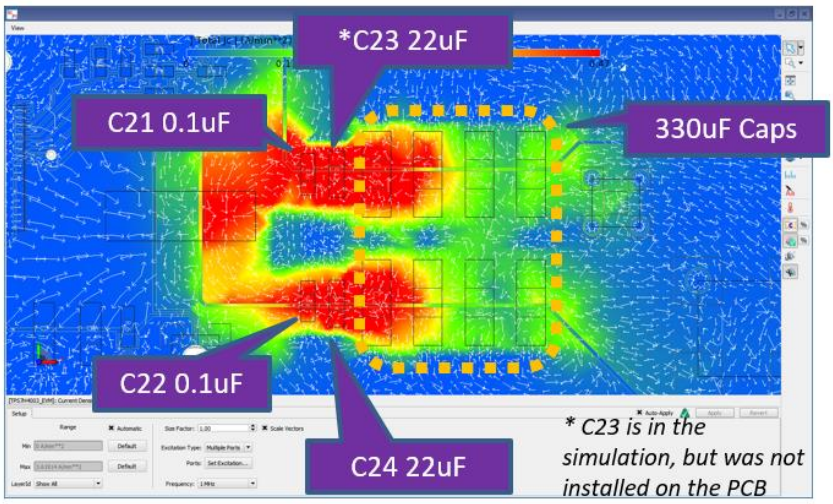



**Figure 36 - EM simulation of the power plane resonances for the TPS7H4003 EVAL show a high current density around the 22uF capacitors when excited at 1 MHz.**

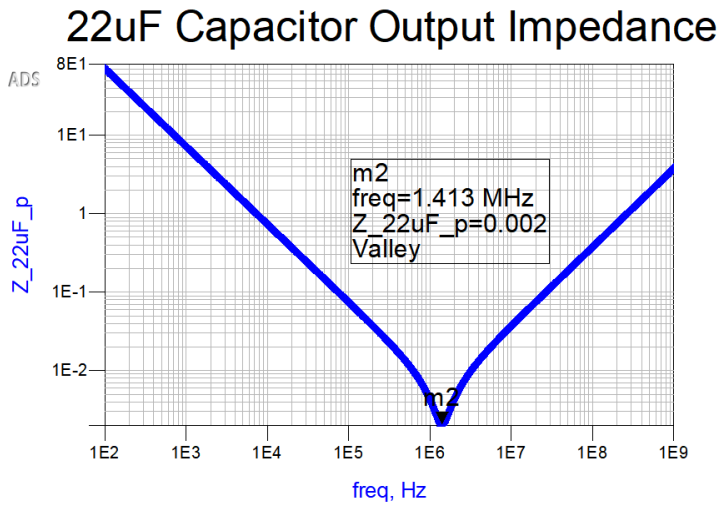



**Figure 37 – Impedance Plot of 22uF Capacitor**

To prove the 1 MHz resonance was truly identified, C24 was removed from the SSAM as indicated by Figure 38. After removing C24 from the SSAM model depicted by Figure 31, the results shown by Figure 39, show this resonance is removed completely. This proves the resonance was occurring on the PCB with the C24 capacitor.

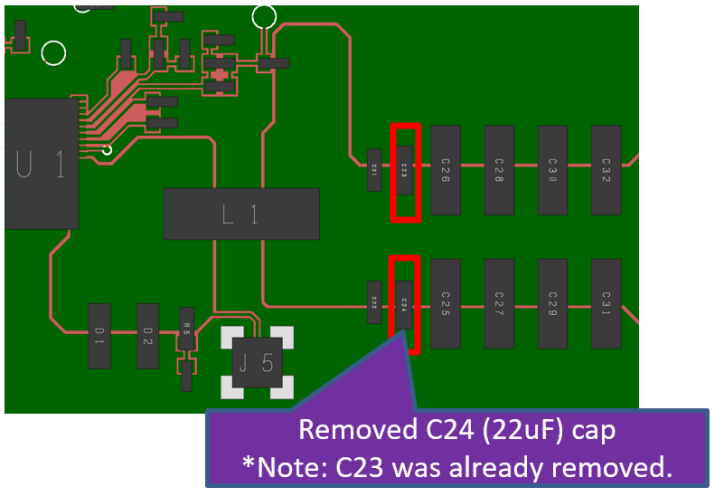



**Figure 38 – Location of the 22uF C24 capacitor that is causing the 1 MHz resonance.**

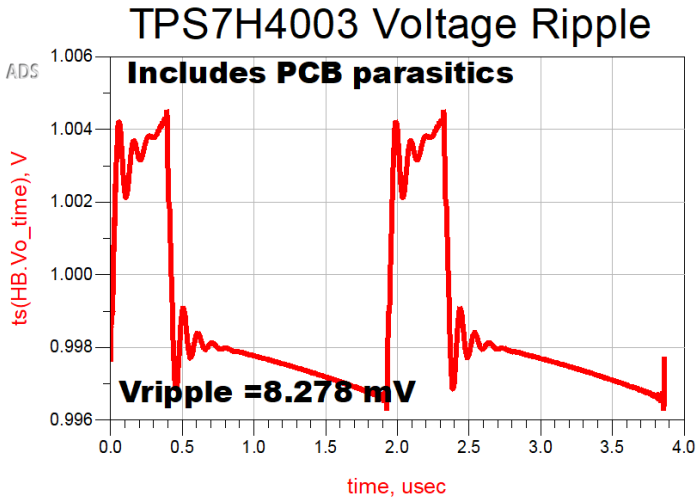



**Figure 39 – The TPS7H4004 SSAM simulated voltage ripple with the 22uF C24 removed no longer has the 1 MHz resonance.**

Now that the design is optimized, the last step is to tune the model. With reference to equations (4) and (5) as well as Figure 40, the overall voltage ripple shape can be tuned to match measurement.

$$Ripple\ Ramp \cong \Delta I_L \cdot ESR \tag{4}$$

$$Ripple\ Height \cong \frac{V_{in} \cdot ESL}{L_O} \tag{5}$$

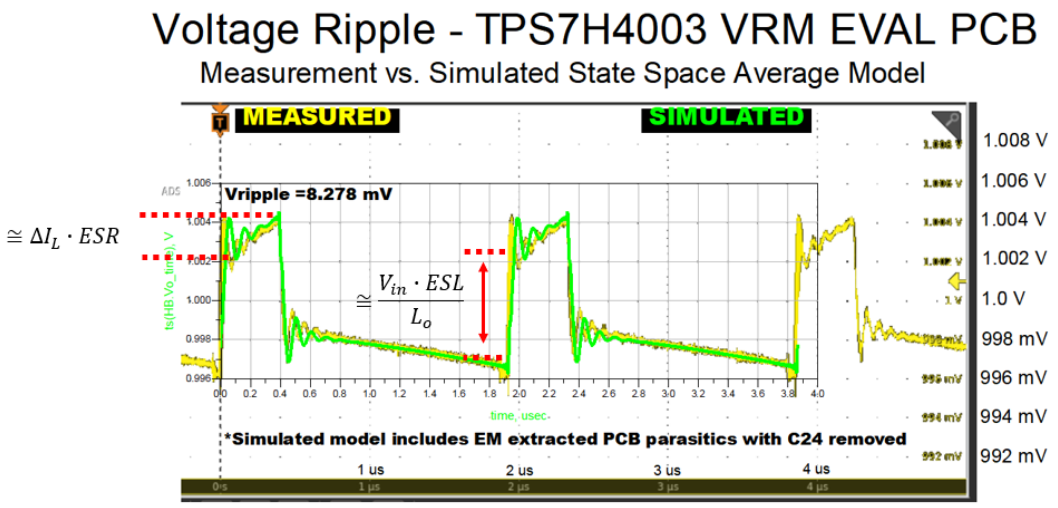



**Figure 40 – TPS7H4003 Simulation versus Measurement**

To answer the question "how much should designers care about including the PCB effects with the VRM model?" First, a fitted VRM passive spice model is created. The schematic for the fitted VRM passive spice model is shown by Figure 41. The output impedance result of the fitted VRM passive spice model when compared to measured is depicted by Figure 42. Which shows great correlation to the impedance measurement.

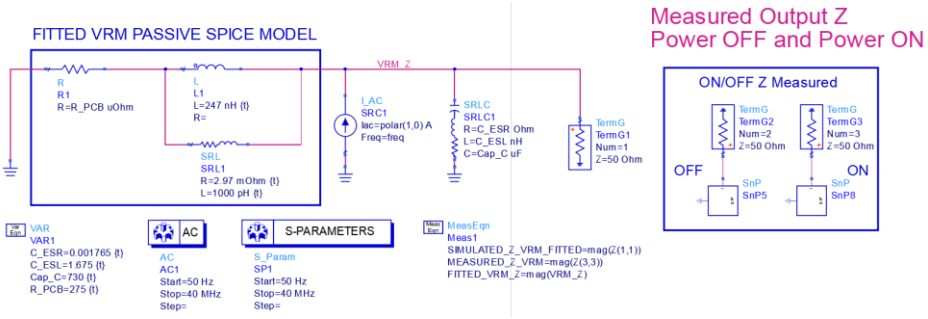



**Figure 41 – Schematic depiction of an impedance curve fitted passive SPICE VRM Model.**

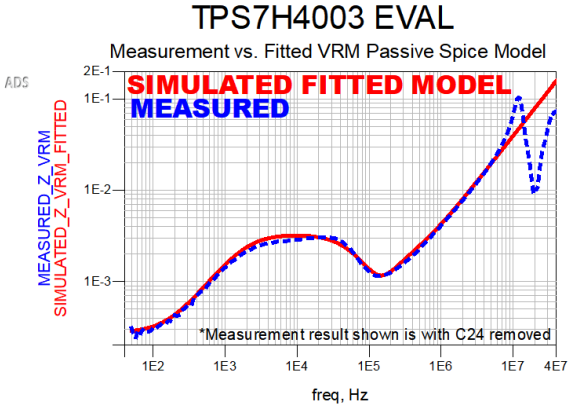



**Figure 42 – Impedance curve fitted passive SPICE VRM model vs. measured impedance.**

As further analysis, a comparison of the impedance between the fitted VRM passive spice model and the SSAM is shown by Figure 43 shows great impedance correlation between

these models. Figure 44 shows the schematic depiction the 10A, 100ns rise time step load applied to both VRM models.

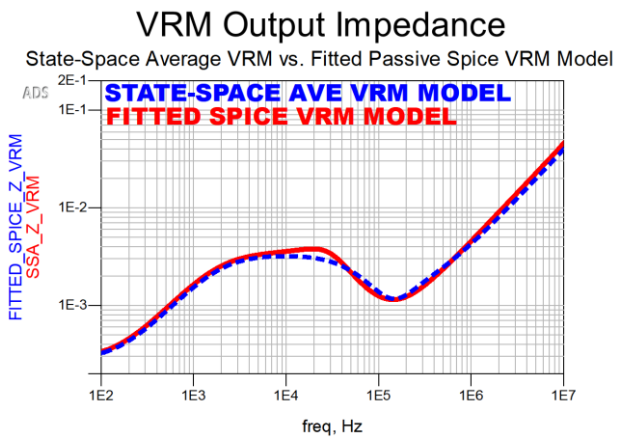



**Figure 43 – Fitted passive SPICE VRM model vs. State-Space Average Model impedance result**

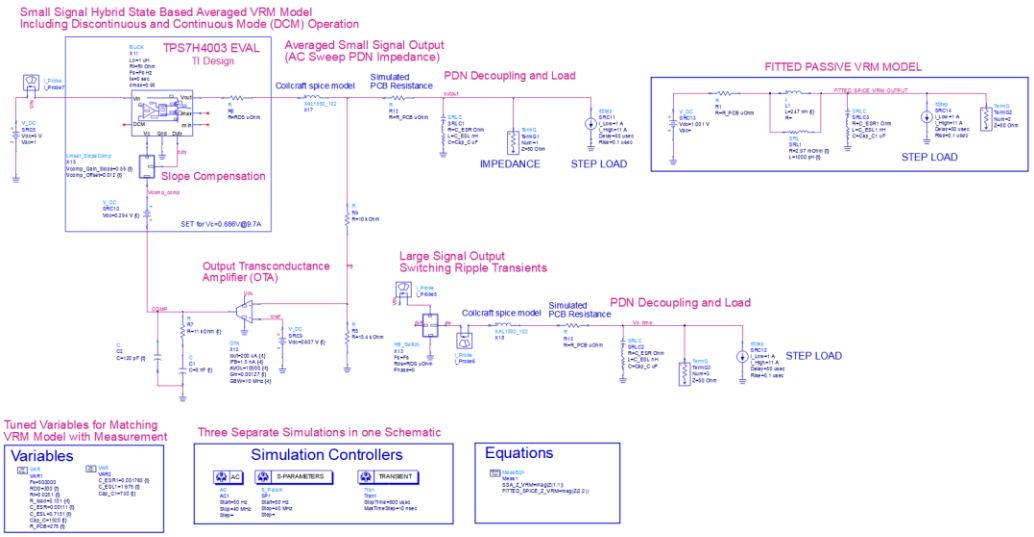



**Figure 44 - Step response model for SSAM VRM Model and fitted SPICE passive VRM model without PCB effects.**

The results from the step load without the PCB effects, are depicted by Figure 45. The SSAM model shows an initial step response of 152.4mV, whereas the fitted VRM SPICE model shows a smaller step response of 135.58mV. The delta between the step response from these two VRM models is 16.8 mV, which is an 11% delta with the SPICE model underestimating the ripple magnitude. When looking at the step response from 50.15us to 50.5us, a large difference in oscillation is observed between the two models. The largest difference in oscillation is observed at around 50.2 us at 35.467 mV, which is an 86% delta with the SSAM showing the larger magnitude voltage ripple even without the PCB effects.

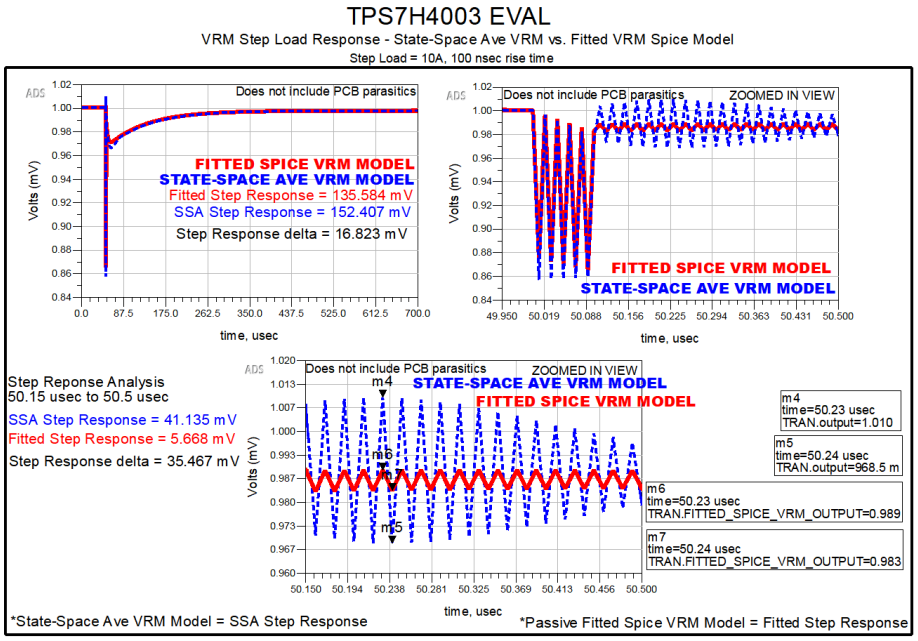



**Figure 45 – Step Response Results – SPICE model vs. SSAM VRM model without PCB effects.**

Figure 46 depicts the exact same model as Figure 44, except now the PCB effects have been added to the model.

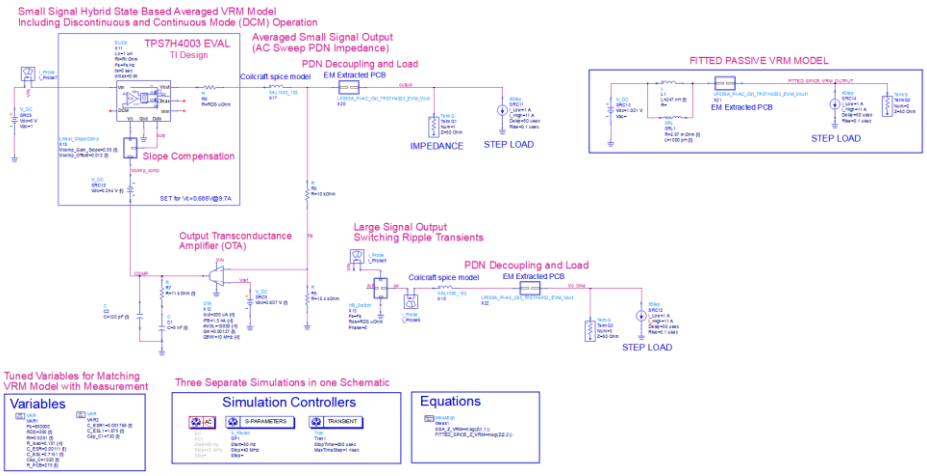



**Figure 46 – Step response model for the SSAM VRM model and the fitted SPICE passive VRM model with PCB effects.**

The results depicted in Figure 47 from the step load with the PCB effects show an increase in voltage ripple for both the SSAM and the fitted SPICE model. The SSAM model shows an initial step response of 258.017mV, whereas the fitted VRM SPICE model shows a smaller step response of 151.883mV. The delta between the step response from these two models with the PCB effects is 106.134mV which is a 41% delta with the fitted SPICE model underestimating the voltage ripple. When looking at the step response from 50.95us to 50.24us, a large difference in oscillation magnitude and phase is now observed between the two models. The largest difference in oscillation is observed

at around 50.13us to 50.19us with a delta of 48.176mV, which is a 79% difference in the step response from the SSAM model with the PCB effects as compared to the fitted SPICE model.

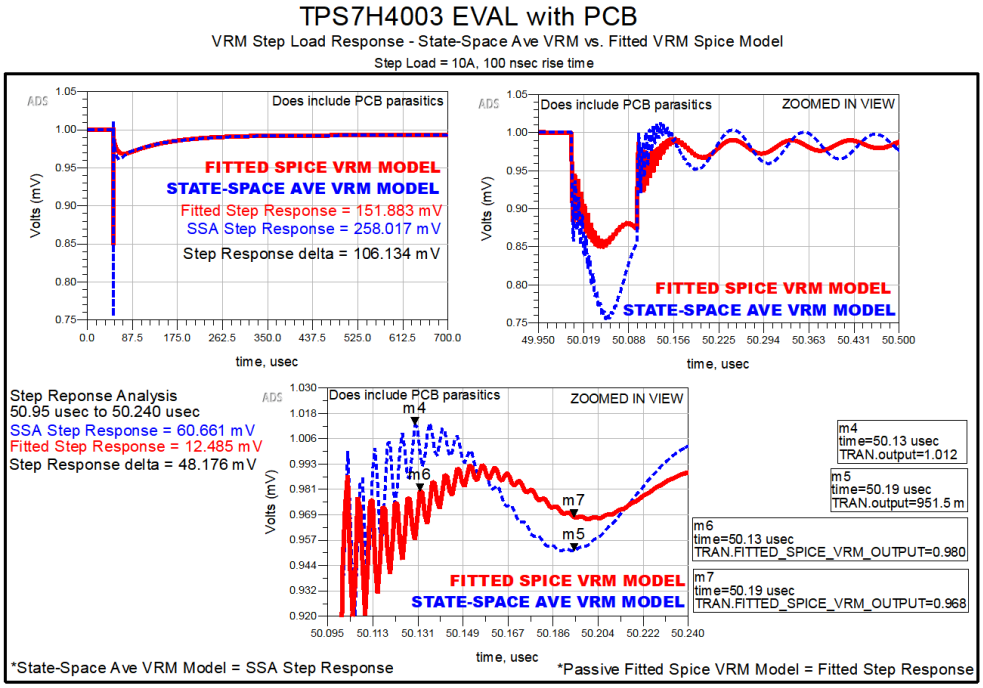



**Figure 47 - Step Response Results – Fitted SPICE model vs. SSAM VRM model without PCB effects.**

Further analysis was done to explore the differences seen in the noise spectrum between these two VRM models both without and with the PCB effects. The results of the step response noise spectrum without the PCB effects are shown by Figure 48. Whereas the results with the PCB effects are shown in Figure 49. In addition, these results are summarized in Table 2. With reference to Figure 48, at 9 MHz the SSAM depicts a peak of -71.07dB, whereas the fitted VRM SPICE model depicts no peaks. In Figure 48, marker m9 was placed at 11.19 MHz to correspond with same frequency point of the VRM SPICE model results shown in Figure 49. In Figure 48, the difference between the SSAM and fitted SPICE VRM model results without the PCB is 43.652dB or a 61% delta with the SSAM predicting a higher noise peak.

When including the PCB effects, with reference to Figure 49, at 9 MHz the SSAM depicts a peak of -55.33dB, whereas the fitted VRM spice model depicts a similar phase peak but shifted to 11.19 MHz with -102dB. This is a difference of 46.677dB or an 84% difference from the SSAM. By looking at the noise spectrum a correlation to the phase shift seen in the time domain is clearer.

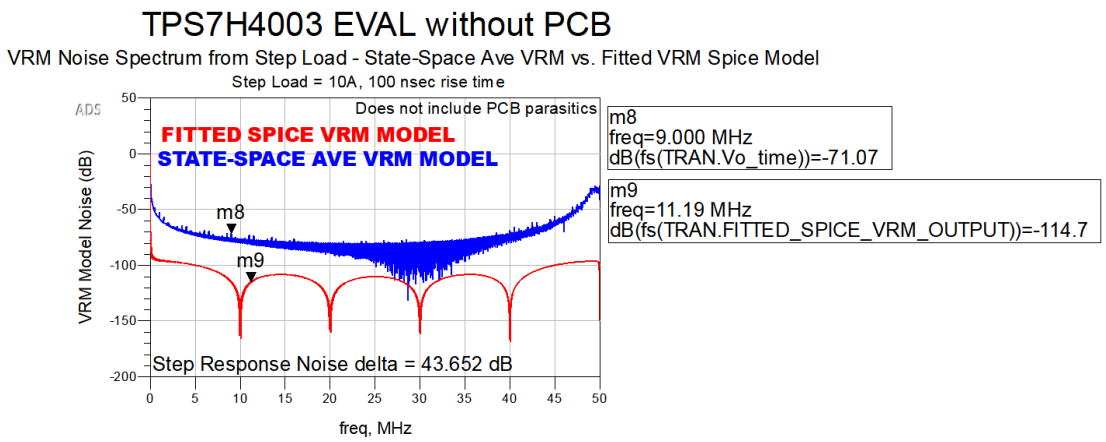



**Figure 48 – The VRM noise spectrum from a step load for the SSAM vs. the fitted VRM SPICE model while simulating without PCB effects.**

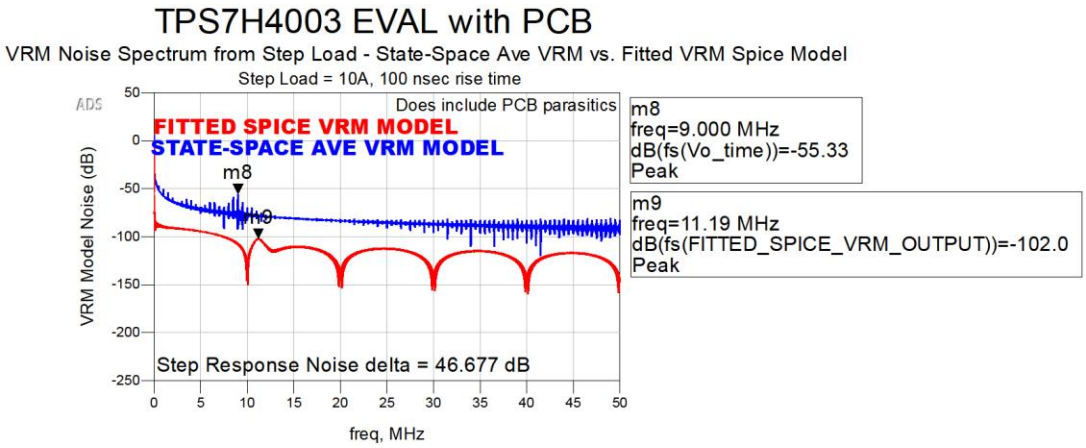



**Figure 49 – The VRM noise spectrum from a step load for the SSAM vs. the fitted VRM SPICE model while simulating with PCB effects.**

| VRM Model | Noise Spectrum without PCB Effects | Noise Spectrum with PCB Effects | Noise Spectrum Delta when adding PCB Effects |
|---|---|---|---|
| Fitted SPICE Model | -114.7 dB | -102 dB | 12.7 dB at 11.19 MHz |
| SSAM | -71.07 dB | -55.33 dB | 15.74 dB at 9 MHz |
| VRM Model Noise Spectrum Delta | **43.652 dB** | **46.677 dB** | |

**Table 2 – Summary of VRM Noise Spectrum Results with a 10A, 100nsec risetime step load applied to the SSAM and the fitted VRM SPICE model without and with PCB effects.**

The result of this effort to compare the SSAM VRM model and the fitted SPICE passive VRM model is to make it clear that these models are very different. Even with the close agreement for the impedance magnitude versus frequency, seen in Figure 43, it is apparent that these two models are significantly different in the time and frequency domains. Table 2 shows that the difference between the models increases significantly, by at least 13dB, when the higher-fidelity PCB effects are included in the simulation. The fitted passive SPICE model underestimates the potential peak-to-peak ripple for this TPS7H4003 VRM modeling test case, with or without the PCB effects.

## Expanding to Multi-Phase SSAM with PCB EM Models

The Sandler SSAM has been successfully demonstrated on the single-phase TPS7H4003 EVAL. Still, it is worth mentioning that nothing prevents the model from being used in multi-phase designs. The model is replicated for the number of stages and the outputs tied together for the small signal AC frequency response. The large signal part of the model is also replicated for the number of stages, and then an additional input is used to set the different phase that each stage will have. The results are shown in Figure 50, demonstrating how it is possible to get the multi-phase noise ripple using an end-to-end power integrity ecosystem simulation with the SSAM VRM model.

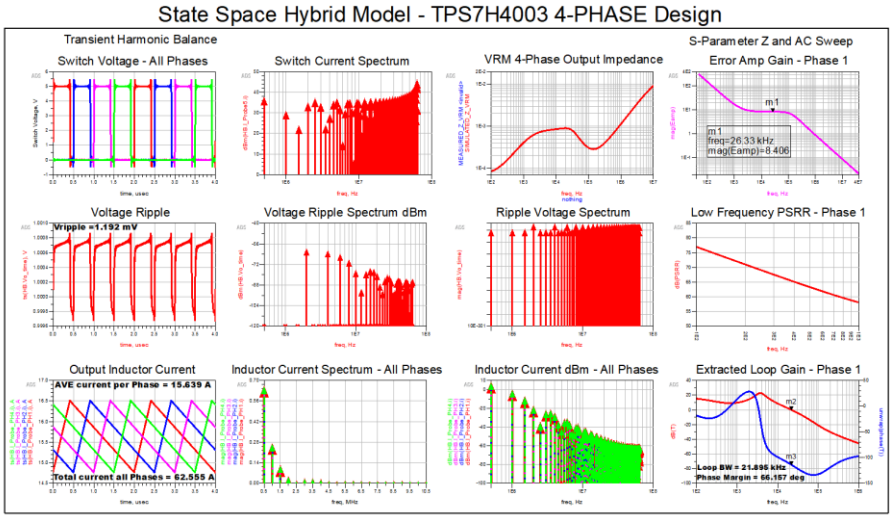



**Figure 50 – TPS7H4003 4-Phase design simulated with the SSAM behavioral model and PCB effects.**

## Summary

In summary, a simple R-L VRM model does not have the fidelity needed for solving the power integrity challenges that engineers face today. Even with a higher order impedance, curve-fitted, passive SPICE VRM model, it was shown that there is still a significant difference when compared to the higher fidelity Sandler state-space average VRM model in both the time and frequency domains. This paper showed that it is simple to give the SSAM behavioral model a try. Most of the parameters for populating the model are set by design, and only a few, like $V_{ramp}$ and Ri, require measurement. The complex equations are programmed into the simulator, making it easy to tune a parameter value that cannot be directly measured by matching the model's output with easy-to-access measured parameters like PSRR and output impedance. Even an imperfect SSAM model for simulation is significantly better than any L-R or L-R-L-R VRM model and will show all the VRM noise, not just impedance-based transients.

The SSAM, with its ability to quickly simulate both small signal AC response and large signal switching noise, makes it ideal for optimizing the end-to-end power integrity ecosystem. In the TPS7H4003 example, shown here, it was demonstrated that PCB effects are also critical, and by including a higher fidelity EM model of the PCB, with the

SSAM VRM model, the simulation was able to predict the 1 MHz resonance seen in measurement and identify the decoupling capacitor that was causing the problem. The Sandler SSAM is not proprietary and is an excellent example of how to build your own high-fidelity VRM behavioral model. A model that will even work with the latest challenges in designing high current, low voltage multi-phase power delivery networks for high-speed digital loads.

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